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LINEAR IC's and APPLICATION'S

4th Sem EC/TC/IT/BME/ML

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OPERATIONAL AMPLIFIER FUNDAMENTALS

❖ Definition of operational amplifier (OP-AMP)

Op-Amp is a directly coupled high gain IC amplifier with two high impedance I/P termiinals and one low output impedance. The op-amp consists of a differential amplifier input stage and an emitter follower output stage.

❖ Op-Amp Symbol :

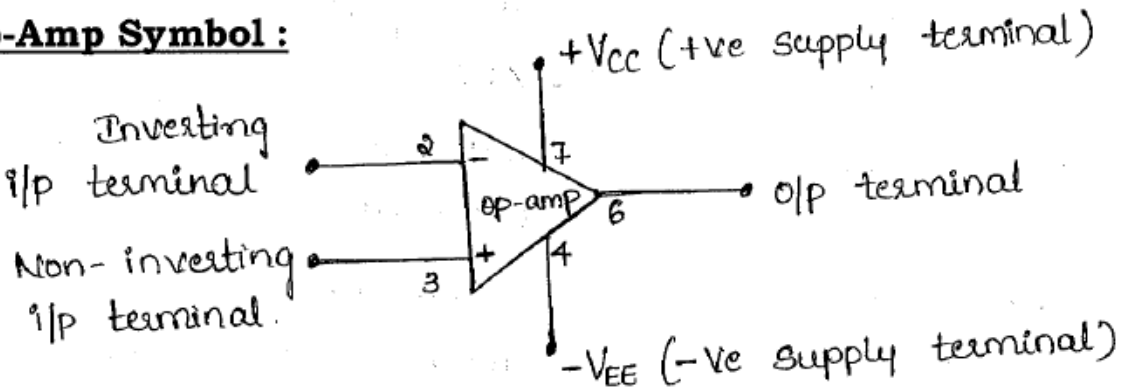

fig 1 @ : symbol.

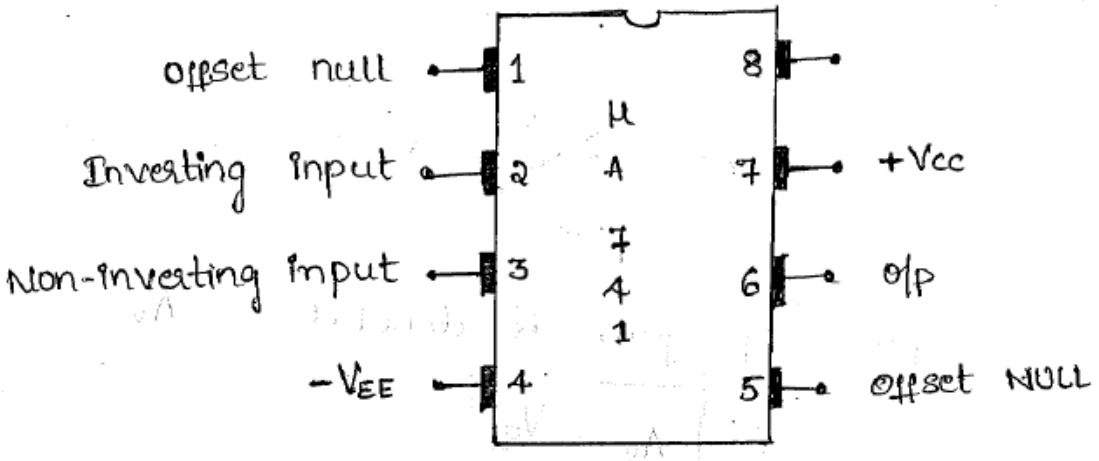

fig 1 ⓑ : Op-Amp IC

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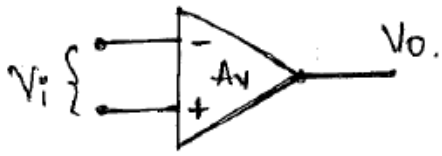
fig 1. @ shows the symbol of op-amp. It consists of 5-terminals as shown above.

NOTE :-

The letter prefix code identifies the manufacturer as shown in table below:

Letter prefix	Manufacturer
AD	Analog devices.
CA	RCA.
LM	National semiconductor corporation.
MC	Motorola.
SN	Texas instruments.
HA	Fair child corporation.

OPEN-LOOP AMPLIFIER :-



open-loop gain is denoted by Av.

i.e $$A_V = \frac{V_o}{V_i}$$

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MODES OF OPERATION OF OP-AMP :-

1) Inverting Mode :-

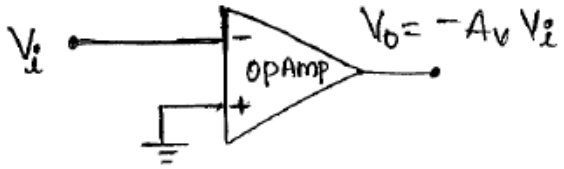
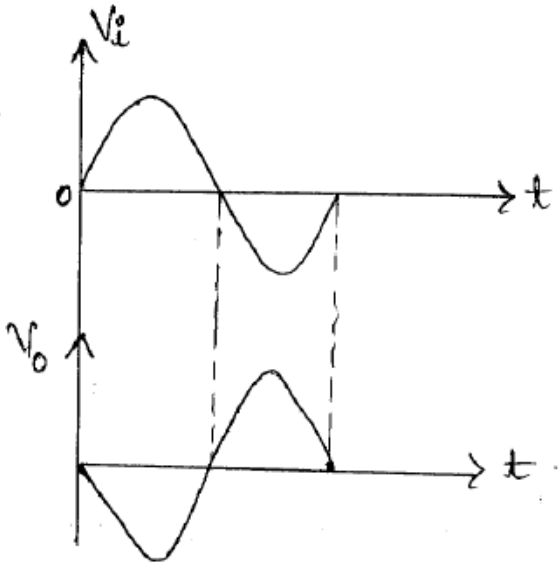


fig : INV Mode.



In INV mode, the I/p voltage V_i is applied to the INV I/p terminal & the Non-INV I/p terminal is grounded. The o/p signal of the INV amplifier is 180° out of phase with the applied I/p signal.

Thus o/p voltage $\boxed{V_o = -A_v V_i}$

2) Non-Inverting Mode :-

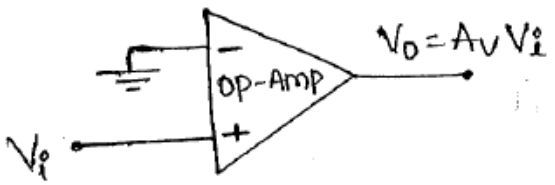
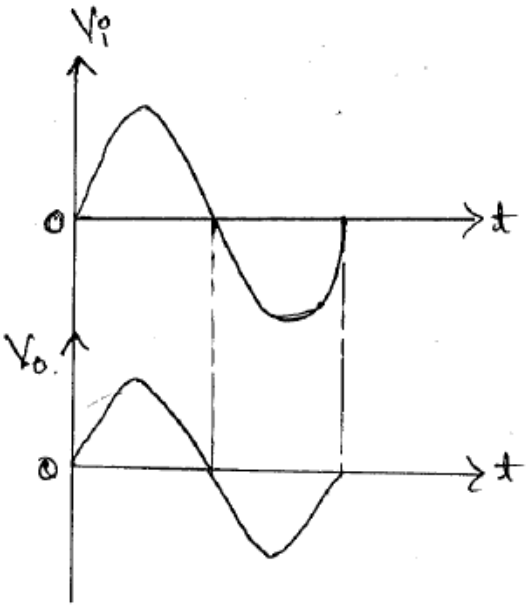


fig : Non-INV mode.



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In Non-INV mode, the I/p voltage is applied to the Non-INV I/p terminal and the INV I/p terminal is grounded. The o/p signal of the Non-INV amplifier is in-phase with the applied I/p signal.

Thus o/p voltage $V_o = A_V V_i$

Differential Mode :-

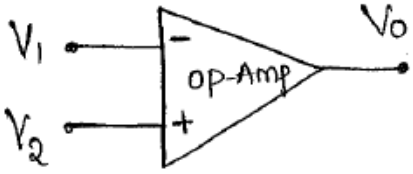

fig : Differential Mode.

$\because A_V = \frac{V_o}{V_i}$.

where $V_i = (V_2 - V_1)$

$V_o = A_V V_i$.

$V_o = A_V (V_2 - V_1)$.

In differential mode, the voltages V_1 & V_2 are applied to the inverting and Non-inverting I/p terminals respectively.

The o/p voltage is proportional to the difference between V_2 & V_1 & hence the name differential mode.

BLOCK DIAGRAM OF OP-AMP :

* Explain the block-diagram of an operational amplifier with the help of a diagram indicating the various building blocks

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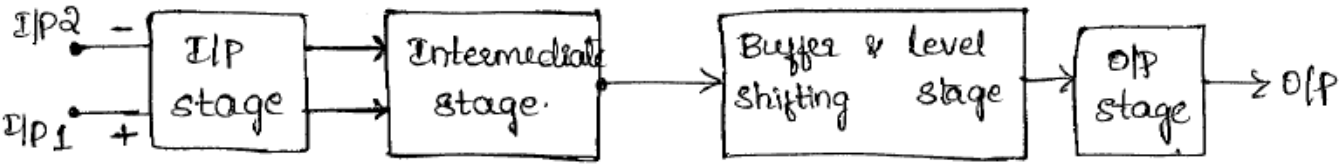

fig ①: Internal block schematic of op-amp.

An op-amp is basically a difference amplifier having very high gain, directly coupled amplifier with high I/P impedance & low-o/p impedance.

fig ① shows the block diagram of Ic op-Amp.

The op-Amp basically consists of 4-stages as shocon in fig ①.

i) I/p stage :-

The I/P stage requires two I/p Terminals with high I/p impedance & low o/p impedance. These requirements are achieved by using dual-I/p, balanced o/p differential amplifier.

The function of a differential amplifier is to amplify the difference between the two I/p signals.

This stage provides a major part of the voltage gain.

ii) Intermediate stage :-

The o/p of the I/P stage is directly fed to the Intermediate stage. This is another differential amplifier with dual I/p, unbalanced o/p (i.e. single ended o/p).

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(The I/P stage alone cannot provide such a high gain).

The main function of the intermediate stage is to provide an additional voltage gain required. practically, the intermediate stage is a chain of cascaded amplifiers called Multistage amplifiers.

iii) Level-shifting stage :-

Since the I/P stage amplifier & the intermediate stage amplifiers are directly coupled the dc voltage at the o/p of the intermediate stage tends to rise above the ground, which is not desirable.

To bring down this dc voltage to zero, a level shifter is employed. This is usually an emitter follower. which also acts as a buffer with very large I/P resistance & loco o/p resistance.

iv) O/P stage :-

The o/p stage consists of a complementary push-pull amplifier, which helps to increase the o/p voltage swing & the current supplying capacity of the op-Amp.

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Ideal characteristics of an op-Amp :-.

An ideal op-Amp exhibits the following characteristics :-.

1) The voltage gain is infinite ($A_V = \infty$)
2) The I/p impedance is infinite
3) The O/p impedance is zero.
4) The bandwidth is infinite
5) There is no change in the characteristic features with changes of temperature.
6) When equal voltages are applied at the two I/p terminals, the O/p is zero.

BASIC OPERATIONAL AMPLIFIER CIRCUIT :-.

* With a neat circuit diagram explain basic operational amplifier circuit.

June-09, 6M

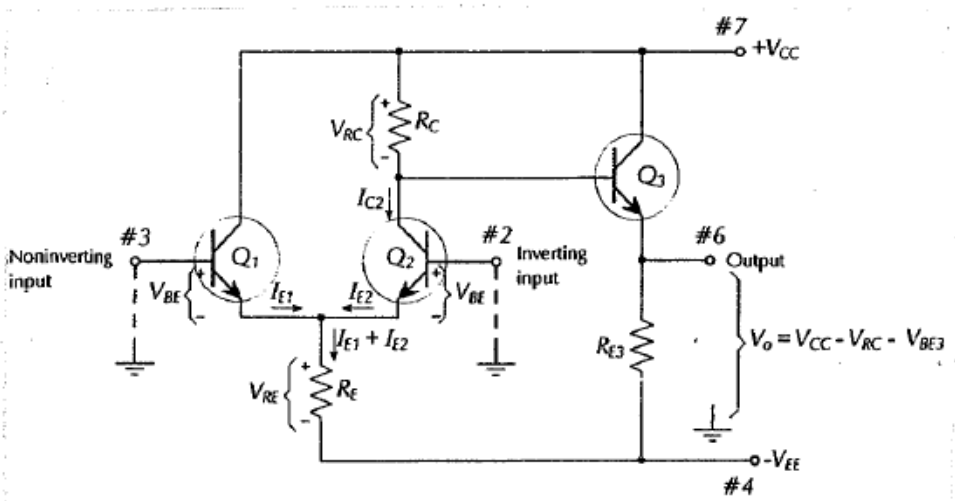

Figure 1 The basic circuit of an operational amplifier has a differential amplifier input stage and an emitter follower output.

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fig ①: Basic circuit of an operational amplifier has a differential amplifier I/P stage & an emitter follower o/p.

The basic circuit of an op-amp is shown in fig ①.

* It is provided with $+V_{CC}$ & $-V_{EE}$ supply voltages and the two i/p terminals are grounded. Transistors Q_1 & Q_2 forms a <u>differential amplifier</u>.

* When a difference I/p voltage is applied to the bases of Q_1 & Q_2, it produces a voltage change at the collector of Q_2. Transistor Q_3 acts as an emitter follower to provide a low o/p impedance.

The dc o/p voltage at pin 6 is (applying KVL from V_{CC}, R_C, Q_3 base & o/p we get)

$$V_{CC} - I_{C2}R_C - V_{BE3} - V_0 = 0$$

$$\boxed{V_0 = V_{CC} - I_{C2}R_C - V_{BE3}.}$$

* Assuming that Q_1 & Q_2 are matched (Identical) transistors, which provides equal V_{BE} Levels & current gains.

With both transistors bases at ground level, the emitter currents I_{E1} & I_{E2} are equal & flow through common emitter resistor 'R_E'

∴ The total emitter current is given by

$$I_{E1} + I_{E2} = \frac{V_{RE}}{R_E}$$

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* Applying KVL from base of Q_2 to $-V_{EE}$ supply.

$$-V_{BE} - (I_{E1} + I_{E2}) R_E + V_{EE} = 0.$$

$$(I_{E1} + I_{E2}) R_E = V_{EE} - V_{BE}.$$

$$\boxed{(I_{E1} + I_{E2}) = \frac{V_{EE} - V_{BE}}{R_E}}$$

NOTE :- i) $I_{E1} = I_{E2}$.

ii) $V_{BE1} = V_{BE2} = V_{BE3}$.

iii) operating point values $\rightarrow I_{CQ}$ & V_{CEQ}.

Here * $\boxed{I_E \approx I_C \approx I_{CQ}.}$

* the collector voltage of Q_2 is given by

$$V_C = V_{CC} - I_C R_C$$

WKT $V_{CE} = V_C - V_E$

& $V_{BE} = V_B - V_E$

as $V_B = 0$.

$$V_{BE} = -V_E$$

$$\boxed{V_E = -V_{BE}}$$

$$V_{CE} = V_C - V_E$$

$$= V_{CC} - I_C R_C - (-V_{BE})$$

$$\boxed{V_{CE} = V_{CC} + V_{BE} - I_C R_C}$$

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FORMULAE

1) operating point value (i) $I_{CQ} = I_E$

(ii) $V_{CEQ} = V_{CC} + V_{BE} - I_C R_C$

2) $V_0 = V_{CC} - I_{C2} R_C - V_{BE}$

3) $I_{E1} + I_{E2} = \dfrac{V_{EE} - V_{BE}}{R_E}$

Problems :

1. calculate the o/p voltage for basic op-amp.
Given $V_{CC} = +10\,V$, $V_{EE} = -10\,V$, $R_E = 4.7\,K\Omega$,
$R_C = 6.8\,K\Omega$ & all transistors have $V_{BE} = 0.7\,V$.

Soln :-

Given :- $V_{CC} = 10\,V$, $V_{EE} = -10\,V$, $R_E = 4.7\,K\Omega$,
$R_C = 6.8\,K\Omega$, $V_{BE} = 0.7\,V$.

WKT $I_{E1} + I_{E2} = \dfrac{V_{EE} - V_{BE}}{R_E} = \dfrac{10\,V - 0.7\,V}{4.7\,K\Omega}$

$$\boxed{I_{E1} + I_{E2} = 2\,mA}$$

& $I_{C2} \approx I_{E2} \approx 1\,mA$.

* o/p voltage V_0 is given by.

$$V_0 = V_{CC} - (I_{C2} R_C) - V_{BE}$$
$$= 10\,V - (1\,mA \times 6.8\,K\Omega) - 0.7\,V$$

$$\boxed{V_0 = 2.5\,V}$$

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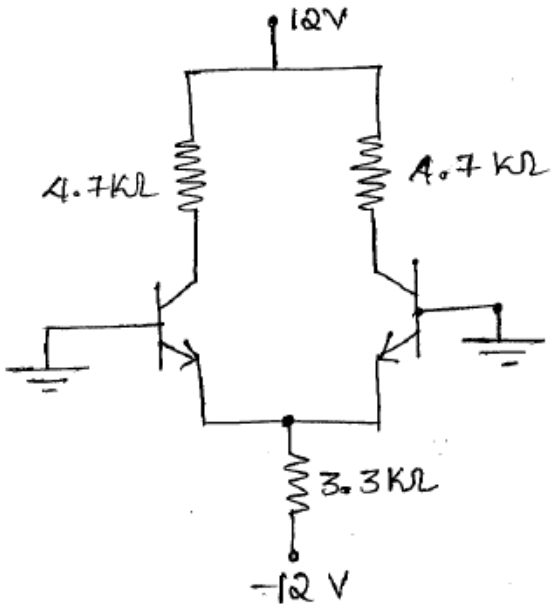
2) calculate the dc operating point values & the o/p voltage for the circuit shown in the fig ①. Assume $V_{BE} = 0.7\ V$ for both the transistors.



Given :- $V_{CC} = +12V$, $-V_{EE} = -12V$, $R_C = 4.7\ K\Omega$,

$V_{BE} = 0.7V$.

Sol:- $$I_{E1} + I_{E2} = \frac{V_{EE} - V_{BE}}{R_E}$$

$$I_{E1} + I_{E2} = 3.42\ mA$$

$$\boxed{I_{E1} + I_{E2} = 1.71\ mA}$$

$$\boxed{I_E \approx I_{CQ} = 1.71\ mA}$$

* $V_{CEQ} = V_{CC} + V_{BE} - I_C R_C = 12V + 0.7\ V - (1.71\ mA \times 4.7\ K\Omega)$

$$\boxed{V_{CEQ} = 4.6536\ V}$$

* o/p voltage.

$$V_0 = V_{CC} - (I_C R_C) - V_{BE}$$

$$= 12\ V - (1.71\ mA \times 4.7\ K\Omega) - 0.7\ V$$

$$\boxed{V_0 = 3.9536\ V}$$

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OP-AMP PARAMETERS :-

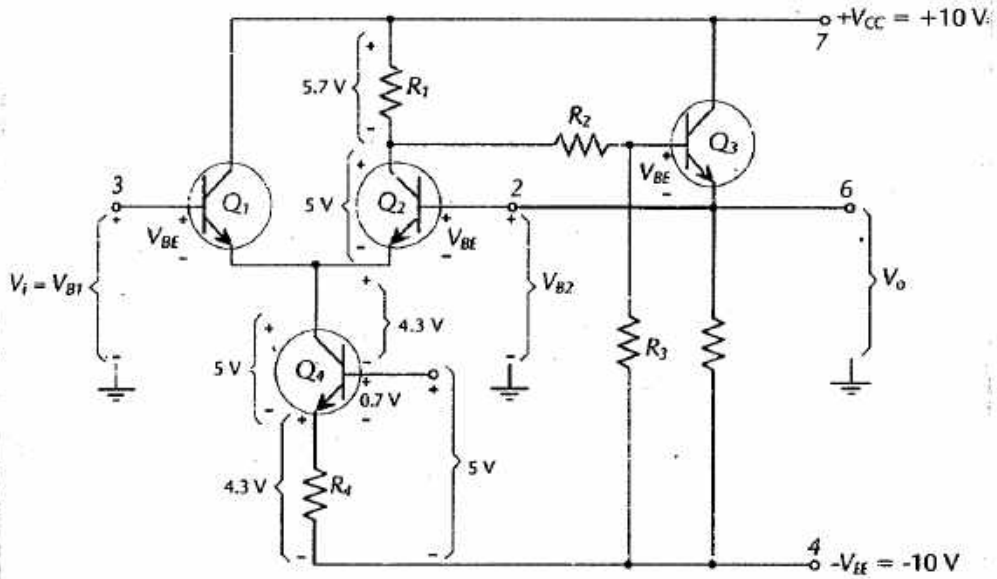

Figure (1) There are limits to the input and output voltage ranges of an operational amplifier. In the basic op-amp circuit these limits occur when any of the transistors approach saturation or cutoff.

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COMMON MODE REJECTION :-

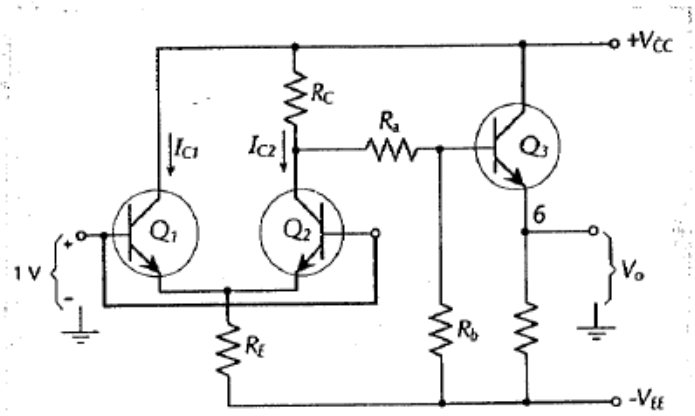

fig ①: Basic circuit of an op-Amp with the two I/P's short circuited and a common input voltage V_i applied to them.

The two input terminals are shorted together & a dc voltage of 1V is applied to it. This is known as a common mode I/p.

Since there is no differential input, & both input terminals are at the same potential. So ideally the o/p should be zero.

Since base voltages of Q_1 & Q_2 are raised by 1V, the voltage drop across R_E also increases by 1V. This increases I_{C1} & I_{C2}. Thus voltage drop across Rc also increases, which results in a change in the o/p.

Similarly, if a -1V common mode I/p is applied, I_{C2} falls & again a change is produced at o/p

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* Thus common-mode voltage gain 'A_{cm}' is defined as the ratio of change in o/p voltage to change in common mode I/p voltage.

i.e. $$A_{cm} = \frac{V_{o(cm)}}{V_{i(cm)}}$$

* The ability of the op-amp in rejecting common mode I/p's is defined as common mode rejection ratio (CMRR).

* CMRR is defined as the ratio of the open-loop gain 'M' to the common mode gain A_{cm}.

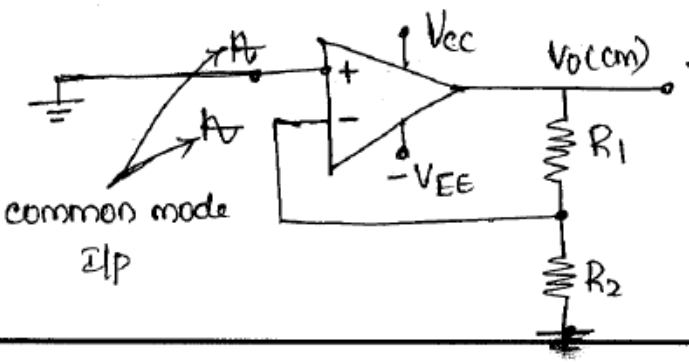
i.e. $$CMRR = \frac{M}{A_{cm}}$$

The CMRR is usually expressed in decibels.

i.e. $$(CMRR)_{dB} = 20 \log_{10}\left(\frac{M}{A_{cm}}\right) dB.$$

Typical value of CMRR for 741 IC is 90dB.

* The effect of common mode gain can be modified with feedback. consider the non-INV amplifier circuit as shown in fig. (2).



$$\left[V_d = IR_2 \quad I = \frac{V_{o(cm)}}{R_1 + R_2}\right]$$

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WKT $A_{cm} = \frac{V_{o(cm)}}{V_{i(cm)}}$.

$$V_{o(cm)} = A_{cm} \cdot V_{i(cm)} \quad \rightarrow (1)$$

The differential I/p voltage required to cancel $V_{o(cm)}$ is,

$$V_d = \frac{V_{o(cm)}}{M} \quad \rightarrow (2)$$

Sub. eq (1) in eq (2), we get

$$V_d = \frac{A_{cm} \times V_{i(cm)}}{M} \quad \rightarrow (3)$$

from fig (2), the feedback vtg 'V_2' across R_2 is

$V_d = IR_2$.

$$V_d = \frac{V_{o(cm)}}{R_1 + R_2} \cdot R_2 \quad \rightarrow (4)$$

where.

$$I = \frac{V_{o(cm)}}{R_1 + R_2}$$

Equating eq (3) & (4)

$$\frac{V_{o(cm)}}{R_1 + R_2} \cdot R_2 = \frac{A_{cm} \times V_{i(cm)}}{M}$$

$$V_{o(cm)} = \frac{A_{cm} V_{i(cm)}}{M} \cdot \frac{R_1 + R_2}{R_2}$$

$$V_{o(cm)} = \frac{A_{cm} V_{i(cm)}}{M} \cdot A_V$$

where $A_V = \frac{R_1 + R_2}{R_2}$.

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CMRR → FORMULAE

1) Mode gain $A_{cm} = \frac{V_{o(cm)}}{V_{i(cm)}}$.

2) Differential I/P $V_d = \frac{V_{o(cm)}}{M}$.

3) $V_{o(cm)} = A_{cm} \cdot V_{i(cm)}$

4) $CMRR = \frac{M}{A_{cm}}$.

$(CMRR)_{dB} = 20 \log_{10}\left(\frac{M}{A_{cm}}\right) dB$.

5) $V_{o(cm)} = \frac{V_{i(cm)}}{CMRR} \cdot A_V$

6) $V_{i(cm)} = \frac{V_{o(cm)} \cdot CMRR}{A_V}$.

CMRR PROBLEMS.

1) A 741 op-amp is used in a non-inverting amplifier with a voltage gain of 50. calculate the typical o/p voltage that would result from a common mode I/P with a peak level of 100mV.

Given: $A_V = 50$, $V_{i(cm)} = 100m$.

From the 741 datasheet: Typical CMRR = 90dB.

Sol:- WKT, $(CMRR)_{dB} = 20 \log_{10} (CMRR)$.

$(CMRR) = \text{antilog} \frac{(CMRR)_{dB}}{20}$.

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$$CMRR = 31623$$

WKT

$$V_{o(cm)} = \frac{V_{i(cm)}}{CMRR} \times A_V$$

$$= \frac{100\ mV}{31623} \times 50$$

$$V_{o(cm)} = 158\ \mu V$$

---

2) Define CMRR of an op-amp. An LM 308 op-amp circuit with a closed loop gain of 33 has a common-mode I/P of 1.5V. calculate the maximum o/p voltage this might produce. The minimum CMRR for LM308 is 80dB.

June-08, 4M

CMRR is defined as the ratio of the open-loop gain 'M' to the common mode gain Acm.

$$CMRR = \frac{M}{A_{cm}}$$

(1M)

In terms of dB, $(CMRR)_{dB} = 20 \log_{10}\left(\frac{M}{A_{cm}}\right)$

Given: $(CMRR)_{dB} = 80\ dB$, $A_V = 33$, $V_{i(cm)} = 1.5V$

Sol:-

$$(CMRR)_{dB} = 20 \log_{10}(CMRR)$$

$$80\ dB = 20 \log_{10}(CMRR)$$

$$CMRR = \text{antilog}\left(\frac{80}{20}\right)$$

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$$\boxed{CMRR = 10000}$$

WKT $V_{o(cm)} = \frac{V_{i(cm)}}{CMRR} \cdot A_V = \frac{1.5V}{10000} \times 33$

$$\boxed{V_{o(cm)} = 5mV}$$

3) When a 741 op-amp having a typical CMRR of 90 dB, is used in a non-inverting amplifier with a voltage gain of 100, the o/p voltage was measured to be 15.8mV with some common-mode I/P. Determine the common mode I/P voltage.

Given: $A_V = 100$, $V_{o(cm)} = 15.8\ mV$, $V_{i(cm)} = ?$

Sol: WKT for $\mu A - 741$, $(CMRR) = 90dB$

$$(CMRR) = \text{Antilog}\left(\frac{90}{20}\right)$$

$$\boxed{CMRR = 31622.78}$$

WKT. $V_{i(cm)} = \frac{V_{o(cm)} \cdot CMRR}{A_V}$

$$= \frac{15.8\ mV \times 31622.78}{100}$$

$$\boxed{V_{i(cm)} = 5V}$$

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Power Supply Rejection Ratio (PSRR) :-

In basic op-amp circuit, a variation in $-V_{EE}$ have the same effect as an I/p voltage change. Thus variations in V_{CC} & V_{EE} do produces some changes at o/p.

The PSRR is the ability of the op-amp to reject variations in the power supply voltages.

Ideally, the o/p voltage should not vary with variations in the power supply voltage.

$$PSRR = \frac{V_o \text{ (ripple)}}{V_s \text{ (ripple)}}$$

* If a variation of 1V in V_{CC} or V_{EE} causes the o/p to change by 1V, then PSRR is 1V per volt i.e. (1V/V)
* If the o/p changes by 10mV when one of the supply voltage changes by 1V, then PSRR is 10mV/V.

For HA-741, the PSRR is typically 30μV/V.
For the LM-108, the PSRR is expressed in decibels.

---

1) A 741 op-amp uses a ±15V supply with a 2mV, 120Hz ripple voltage superimposed. calculate the amplitude of the o/p voltage produced by the power supply ripple.

Given:- $V_s \text{(ripple)} = 2mV.$

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Sol:- WKT for op-amp 741, PSRR = 30 μV/V.

WKT $PSRR = \frac{V_o(\text{ripple})}{V_s(\text{ripple})}$.

$V_o(\text{ripple}) = PSRR \times V_s(\text{ripple})$

$= 30\,\mu V/V \times 2mV$

$\boxed{V_o(\text{ripple}) = 60nV}$

---

2) An LM 108 op-amp has a typical PSSR of -80dB. working with ±15V supply having 3mV ac ripple. Calculate the maximum level of the o/p vtg ripple.

Given:- $(PSRR)_{dB} = -80dB$, $V_s(\text{ripple}) = 3mV$, $V_o(\text{ripple}) = ?$

Sol:-

$(PSRR)_{dB} = 20 \log_{10}(PSRR)$

$(-80) = 20 \log_{10} PSRR$.

$(PSRR) = \text{Antilog}\left(\frac{-80}{20}\right)$

$\boxed{PSRR = 10^{-4}}$

WKT. $PSRR = \frac{V_o(\text{ripple})}{V_s(\text{ripple})}$

$V_o(\text{ripple}) = PSRR \times V_s(\text{ripple})$.

$= 10^{-4} \times 3mV$

$\boxed{V_o(\text{ripple}) = 0.3\,\mu V}$

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* A 741 op-amp having a PSRR of 30 μV/V, has a minimum o/p signal level of 100 mV. O/p ripple voltage produced by the ripple on the supply voltages is not to exceed 0.1 % of the minimum o/p signal level. Determine the maximum permissible supply voltage ripple.

Given :-

PSSR = 30 μV / V,

Minimum o/p signal = 100 mV

∴ V_o (ripple) = 0.1 % of minimum o/p signal

$$= \frac{0.1}{100} \times 100\,mV$$

$$\boxed{V_o \text{ (ripple)} = 0.1\,mV}$$

$$V_s \text{ (ripple)} = \frac{V_o \text{ (ripple)}}{PSSR}$$

$$= \frac{0.1\,mV}{30\,\mu V/V}$$

$$\therefore \boxed{V_s \text{ (ripple)} = 3.33\,V}$$

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2) The resistors $R_1 = R_2 = 18\,K\Omega$ have tolerance of $\pm 5\%$. Calculate the maximum I/p offset voltage due to resistor tolerance at 25°C,

i) When LM 108 is used having I/p bias current 2 nA maximum.

ii) When the op-amp is an LM 308 with I/p bias current of 7 nA maximum.

Given :- $R_1 = R_2 = 18\,K\Omega$, tolerance $= \pm 5\%$, $I_B = 2\,nA$.

Sol :- Because of the $\pm 5\%$ resistor tolerance.

$$R_2 = 18\,K\Omega - 5\% = 17.1\,K\Omega$$

$$R_1 = 18\,K\Omega + 5\% = 18.9\,K\Omega$$

i) When LM 108 is used with $I_B = 2\,nA$ maximum, the maximum I/p offset voltage is given by

$$V_i\,(offset) = I_B R_1 - I_B R_2$$

$$= I_B [R_1 - R_2]$$

$$= 2 \times 10^{-9} [18.9\,K\Omega - 17.1\,K\Omega]$$

$$\boxed{V_i\,(offset) = 3.6\,mV}$$

ii) When LM 308 is used with $I_B = 7\,nA$ maximum, the maximum I/p offset voltage is given by

$$V_i\,(offset) = I_B [R_1 - R_2]$$

$$= 7 \times 10^{-9} [18.9\,K\Omega - 17.1\,K\Omega].$$

$$\boxed{V_i\,(offset) = 12.6\,\mu V}$$

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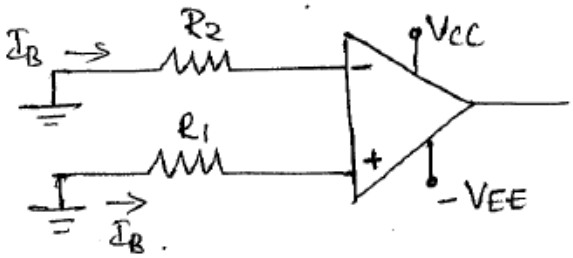
3) In fig ①, a 741 op-amp is used with resistances $R_1 = R_2 = 27\,K\Omega$ each having a tolerance of $\pm 20\%$. calculate the maximum I/p offset voltage due to

i) the 741 specified I/p offset voltage.

ii) the 741 input offset current

iii) the resistor tolerance.

Given that V_i (offset) = 6 mV maximum, I_i (offset) = 200nA maximum & I/p bias current $I_B = 500\,nA$ maximum.



Given :- $R_1 = R_2 = 27\,K\Omega$

Tolerance = $\pm 20\%$

V_i (offset) = 6 mV,

I_i (offset) = 200nA

I_B = 500nA maximum.

Sol :-

i) the maximum I/p offset voltage = 6 mV max

ii) $V_i(\text{offset}) = I_i(\text{offset}) \times (R_1 \text{ or } R_2)$

$= 200\,nA \times 27\,K\Omega$

$\therefore V_i(\text{offset}) = 5.4\,mV$

iii) Given $I_{B(max)} = 500\,nA$

Due to $\pm 20\%$ tolerance of resistors

$R_2 = 27\,K\Omega - 20\% = 21.6\,K\Omega$

$R_1 = 27\,K\Omega + 20\% = 32.4\,K\Omega$

V_i (offset) $= I_B (R_1 - R_2)$

$= 500\,nA\,(32.4\,K\Omega - 21.6\,K\Omega)$

V_i (offset) = 5.4 mV

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4) In the circuit of fig ①, a LM 108 op-amp is used with resistances $R_1 = R_2 = 18\,K\Omega$. calculate the maximum I/p voltage due to i) the op-amp specified I/p offset voltage and ii) the I/p offset current.

Given that $V_i(offset) = 3mV$ maximum & $I_i(offset) = 0.2\,nA$ at 25°C for LM 108.

Given :- $R_1 = R_2 = 18\,K\Omega$, $V_i(offset) = 3mV$, $I_i(offset) = 0.2\,nA$

Sol :- i) the maximum I/p offset voltage = 3mV maximum

ii) $V_i(offset) = I_i(offset) \times (R_1 \text{ or } R_2)$

$= 0.2 \times 10^{-9} \times 18\,K\Omega$

$V_i(offset) = 3.6\,\mu V$

---

5) What is meant by offset in an op-amp, how does it effect the performance of the op-amp? If an op-amp has an bias current of 200nA & two equal resistances of 20KΩ are connected between inverting terminal & ground as well as non-inverting terminal & ground respectively what will be the I/p offset vltg for a tolerance of ±20% in resistor values? what will be o/p voltage under open loop gain of 10^5?

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Sol :-

When the two-transistors of the I/p stage are not perfectly matched then the two base currents are different i.e. $I_{B1} \neq I_{B2}$ & there is some difference between their base-emitter voltages $V_{BE1} \neq V_{BE2}$. Due to this, there is presence of unwanted voltages & currents which are called offset voltages & currents.

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I/p offset voltage (V_{IOS}) :-

The differential voltage that must be applied between the two input terminals of an op-amp, to make the o/p voltage zero is called Input offset voltage and denoted as V_{IOS}.

I/p offset current (I_{IOS}) :-

The algebraic difference between the current flowing into the two input terminals of the op-amp is called input offset current and denoted as I_{IOS}.

$$I_{IOS} = |I_{B1} - I_{B2}|$$

O/p offset voltage (V_{OS}) :-

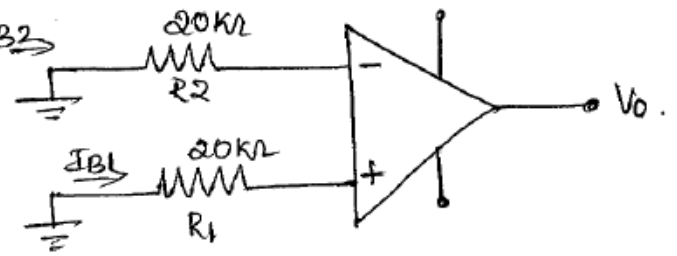
The presence of dc voltage at the o/p terminals when both the I/p terminals are grounded is called output offset voltage.

4- Marks

Given :- $I_B = 200nA$, $R_1 = R_2 = 20K\Omega$,

Tolerance $= \pm 20\%$ $A_V = 10^5$.

Sol :-



4- Marks

$R_1 = 20K\Omega + 20\% = 24\ K\Omega$

$R_2 = 20K\Omega - 20\% = 16\ K\Omega$

$V_i(\text{offset}) = I_B[R_1 - R_2] = 200nA\ [24K\Omega - 16K\Omega]$

$$V_i(\text{offset}) = 1.6\ mV$$

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$V_{out} = V_{i(offset)} \times A_V = 1.6\ mV \times 10^5$

$V_{out} = 160$

I/p & o/p Impedances :-

Input impedance :-

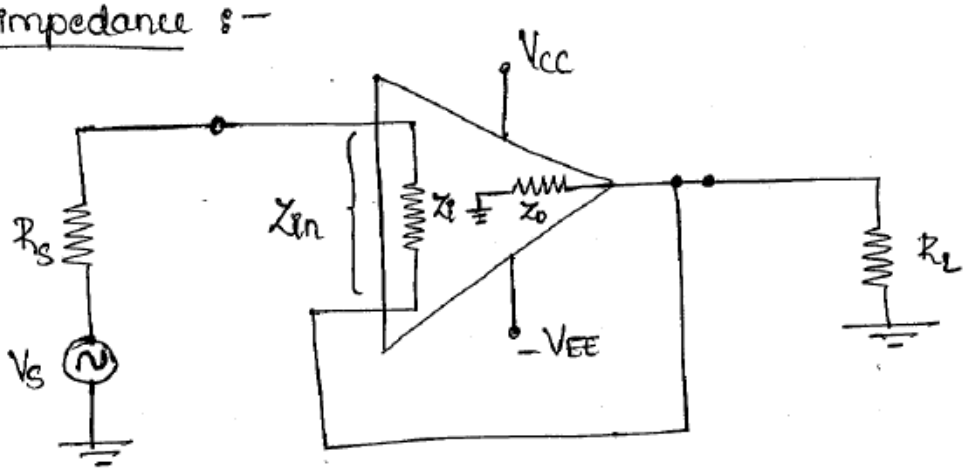

fig ① :.

In most op-amp applications, some form of negative feedback is normally provided by the externally connected components.

From negative feedback, the I/p impedance of the op-amp I/p terminal becomes

$$Z_{in} = (1 + M\beta) Z_i$$

Where, Z_i = the op-amp I/p impedance without negative feedback.

M = op-amp open-loop gain.

β = feedback factor = 1 for a ∮ Voltage follower.

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The impedance of signal sources connected at the input of an op-amp circuited should be very much smaller than the amplifier input impedance to avoid a loss of signal across 'Rs'.

Output impedance :-

The typical o/p resistance specified for the 741 op-amp is 75Ω. Any stray capacitance in parallel with this is certain to have a much larger reactance than 75Ω.

* The output impedance of the op-amp is affected by negative feedback.

$$Z_{out} = \frac{Z_o}{1 + M\beta}$$

Where,

Z_o = op-amp o/p impedance without negative feedback.

M = op-amp open-loop gain

β = feedback factor.

Load impedance connected at the o/p of an op-amp should be much larger than the circuit o/p impedance. This is to avoid any significant loss of o/p as a voltage drop across Z_{out}.

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NOTE :-

From 741 op-amp datasheet.

1) $R_i(min) = Z_i = 0.3\,M\Omega$

2) $M(min) = 50,000$

3) $Z_o = 75\Omega$

4) Typical value of $M = 200000 = 2 \times 10^5$

5) For voltage follower, $\boxed{\beta = 1}$

6) For INV amplifier & Non-INV amplifier, $\boxed{\beta = \frac{1}{A_V}}$

FORMULAE

1) Input impedance $Z_{in} = (1 + M\beta)Z_i$

2) output impedance $Z_{out} = \frac{Z_o}{1 + M\beta}$

3) For voltage follower $\boxed{\beta = 1}$

4) For INV & Non INV amplifier $\beta = \frac{1}{A_V}$

5) $A_V = \frac{R_1 + R_2}{R_2}$ & $\frac{1}{A_V} = \frac{R_2}{R_1 + R_2}$.

PROBLEMS

1) calculate the minimum Input impedance of a 741 op-amp employed as a voltage follower.

Sol :- WKT for 741 the minimum value of Z_i is

$Z_i(min) = 0.3\,M\Omega$ & $M(min) = 50,000$

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for voltage follower $\beta = 1$

$$Z_{in} = (1 + M\beta)\, Z_{i(min)}$$

$$= (1 + 50000 \times 1)\ 0.3\,M\Omega$$

$$\boxed{Z_{in} = 15000\ M\Omega}$$

---

2) calculate the typical o/p impedance of a 741 op-amp connected to function as a voltage follower

Sol:- WKT for 741 op-amp, the typical value of

$Z_o = 75\Omega$ & $M = 200000$

for voltage follower $\boxed{\beta = 1}$

$$Z_{out} = \frac{Z_o}{1 + M\beta} = \frac{75\Omega}{(1 + 200000 \times 1)}$$

$$\boxed{Z_{out} = 0.004\ \Omega}$$

---

3) From data sheet of LM 108, the minimum value of input resistance is 30MΩ and large signal voltage gain (open-loop) is 50,000. Determine the minimum input impedance of an LM 108 op-amp when it is used as i) voltage follower ii) a non-inverting amplifier with a voltage gain of 60.

Given :- $Z_i = 30M\Omega$, $M = 50,000$

i) For voltage follower $\boxed{\beta = 1}$

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$$Z_{in} = (1+M\beta) Z_i = (1+50000 \times 1)\, 30M\Omega$$

$$\boxed{Z_{in} = 1.5 \times 10^{12}\,\Omega}$$

ii) when used as a non-INV amplifier with a voltage gain of 60, we have $\beta = \frac{1}{A_V} = \frac{1}{60}$

$$Z_{in} = (1+M\beta) Z_i = \left(1 + 50000 \times \frac{1}{60}\right) 30 \times 10^6.$$

$$\boxed{Z_{in} = 2.5 \times 10^{10}\,\Omega}$$

---

4) From the data sheet of LM 308, having input resistance of 10MΩ minimum & open-loop gain of 15,000 minimum. Determine the minimum I/p impedance of an LM 308 op-amp when it is used as
i) Voltage follower ii) a non-INV amplifier with a voltage gain of 60.

Given :- $Z_i = 10M\Omega$, $M = 15000$, $A_V = 60$.

Sol :-

i) When used as voltage follower, $\boxed{\beta = 1}$

$$Z_{in} = (1+M\beta) Z_i = (1 + 15000 \times 1)\, 10 \times 10^6$$

$$\boxed{Z_{in} = 1.5 \times 10^{11}\,\Omega}$$

ii) When used as a non-INV amplifier with a voltage gain of 60 ie. $\beta = \frac{1}{A_V} = \frac{1}{60}$

$$Z_{in} = (1+M\beta) Z_i = \left(1 + M \frac{1}{A_V}\right) Z_i$$

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$$Z_{in} = \left(1 + 15{,}000 \times \frac{1}{60}\right)$$

$$\boxed{Z_{in} = 2.5 \times 10^{9}\,\Omega}$$

---

5) Determine the typical o/p resistance for a 715 op-amp (with typical o/p resistance of 75 Ω & open-loop large signal gain of 30,000)

i) When used as a voltage follower and

ii) When used as a non-INV amplifier with a gain of 100.

Given: $Z_o = 75\,\Omega$, $M = 30{,}000$, $A_V = 100$

i) When used as a voltage follower $\boxed{\beta = 1}$

$$Z_{out} = \frac{Z_o}{1 + M\beta} = \frac{75\,\Omega}{(1 + 30000 \times 1)} = \underline{2.5 \times 10^{-3}\,\Omega}$$

ii) When used as non-INV amplifier with a gain of 100,

$$\boxed{\beta = \frac{1}{A_V} = \frac{1}{100}}$$

$$Z_{out} = \frac{Z_o}{(1 + M\beta)}$$

$$= \frac{Z_o}{\left(1 + M \cdot \frac{1}{A_V}\right)} = \frac{75\,\Omega}{\left(1 + 30000 \cdot \frac{1}{100}\right)}$$

$$\boxed{Z_{out} = 0.25\,\Omega}$$

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6) Determine the typical I/p & O/p impedances of a non-INV amplifier with a voltage gain of 40,

i) Using a 741 op-amp (having typical $Z_i = 2M\Omega$, $Z_o = 75\Omega$, $M = 2\times10^5$)

ii) Using a 715 op-amp (having typical $Z_i = 1M\Omega$, $Z_o = 75\Omega$, $M = 30,000$)

Given :- $A_V = 40$.

Sol :-

i) For 741 op-amp :

Given $Z_i = 2M\Omega$, $Z_o = 75\Omega$, $M = 2\times10^5$

For Non-INV amplifier $\beta = \frac{1}{A_V} = \frac{1}{40}$

I/p impedance is

$$Z_{in} = (1+M\beta)\,Z_i = \left(1+2\times10^5\left(\frac{1}{40}\right)\right) 2M\Omega.$$

$$\boxed{Z_{in} = 10\times10^9\,\Omega}$$

O/p impedance is.

$$Z_{out} = \frac{Z_o}{(1+M\beta)} = \frac{75\Omega}{\left[1+2\times10^5\left(\frac{1}{40}\right)\right]}$$

$$\boxed{Z_{out} = 15\times10^{-3}\,\Omega}$$

ii) For 715 op-amp :

Given : $Z_i = 1M\Omega$, $Z_o = 75\Omega$, $M = 30000$, $\beta = \frac{1}{A_V} = \frac{1}{40}$

I/p impedance is

$$Z_{in} = (1+M\beta)\,Z_i = \left(1+30000\left(\frac{1}{40}\right)\right) 1M\Omega$$

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$$Z_{in} = 7.5 \times 10^8\ \Omega$$

o/p impedance is.

$$Z_{out} = \frac{Z_o}{1+M\beta} = \frac{75\ \Omega}{\left[1 + 30000\left(\frac{1}{40}\right)\right]}$$

$$Z_{out} = 0.1\ \Omega$$

---

7) calculate the typical I/p & O/p resistance of a non-inverting amplifier with a voltage gain of 25, i) Using a 741 op-amp ii) Using a 715 op-amp.

for 741 : $Z_i = 2M\Omega$, $M = 2\times10^5$, $Z_o = 75\Omega$

for 715 : $Z_i = 1M\Omega$, $M = 3\times10^4$, $Z_o = 75\Omega$.

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Given :- $A_V = 25$

Sol :-

i) Using a 741 op-amp.

Given : $Z_i = 2M\Omega$, $M = 2\times10^5$, $Z_o = 75\Omega$

For Non-INV amplifier $\beta = \frac{1}{A_V} = \frac{1}{25}$

Input impedance is

$$Z_{in} = (1+M\beta)Z_i = \left[1 + 2\times10^5\left(\frac{1}{25}\right)\right]2M\Omega$$

$$Z_{in} = 1.6\times10^9\ \Omega \leftarrow \text{2Mark}$$

output impedance is

$$Z_{out} = \frac{Z_o}{1+M\beta} = \frac{75\Omega}{\left[1 + 2\times10^5\left(\frac{1}{25}\right)\right]}$$

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$Z_{out} = 9.4\ m\Omega$ ← 1 Mark

ii) Using a 715 op-amp :-

Given : $Z_i = 1M\Omega$, $M = 3\times10^4$, $Z_o = 75\Omega$, $\beta = \frac{1}{A_V} = \frac{1}{25}$

Input impedance is

$$Z_{in} = (1+M\beta)Z_i = \left[1 + 3\times10^4 \cdot \left(\frac{1}{25}\right)\right] \times 1M\Omega$$

$Z_{in} = 1.2 \times 10^9\ \Omega$ ← 2 marks

output impedance is

$$Z_{out} = \frac{Z_o}{[1+M\beta]} = \frac{75\Omega}{\left[1 + 3\times10^4\left(\frac{1}{25}\right)\right]}$$

$Z_{out} = 63\ m\Omega$ ← 1 mark

8) prove that the open loop I/p & O/p impedance of an op-amp under closed loop condition change due to feedback. Determine these impedances for an non-INV amplifier with a closed loop gain of 200. the op-amp has differential I/p impedance of $2\times10^6\ \Omega$ & O/p impedance 50Ω. The open loop gain of op-amp $A_{V0} = 10^6$

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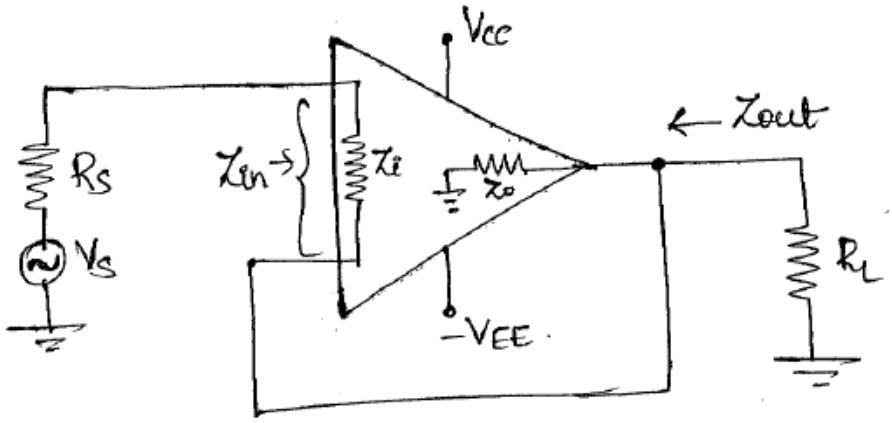
Proof :-



If Z_i & Z_o are the openloop impedance, then closed loop impedance is given by

$$Z_{in} = [1+M\beta]\, Z_i \quad \Omega$$

$$Z_{out} = \frac{Z_o}{1+M\beta}$$

← 2 Marks

Given :- $A_V = 200$, $Z_i = 2\times10^6\,\Omega$, $Z_o = 50\,\Omega$, $A_{VO} = M = 10^6$

for non-INV amplifier $\beta = \frac{1}{A_V} = \frac{1}{200}$

$$Z_{in} = [1+M\beta]\, Z_i$$

$$= \left[1 + 10^6 \times \frac{1}{200}\right] 2\times10^6$$

$$\boxed{Z_{in} = 10^{10}\,\Omega}$$ ← 1-Mark

$$Z_{out} = \frac{Z_o}{1+M\beta} = \frac{50\,\Omega}{\left[1 + 10^6 \times \frac{1}{200}\right]}$$

$$\boxed{Z_{out} = 9.9\,m\Omega}$$ ← 1 Mark

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Slew Rate :-

The slew rate 'S' of an op-amp is the maximum rate at which the output voltage can change.

When the slew rate is too slow for the I/p, distortion results.

To understand the concept of slew rate, let us consider an op-amp voltage follower circuit as shown in fig below :

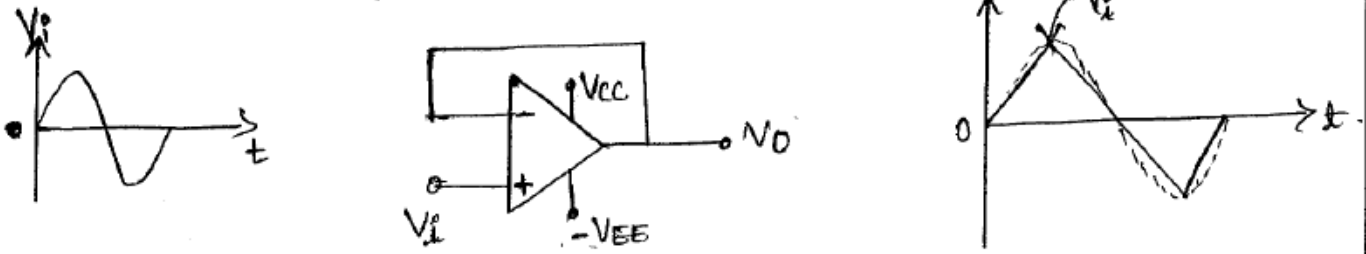

fig ① : Illustrates slew rate being too slow compared to fast rising I/p voltage.

fig ② illustrates a sine wave I/p to a voltage follower producing a triangular o/p waveform.

The triangular wave results because the op-amp simply cannot move fast enough to follow the sine wave I/p.

i.e, $$\text{Slew rate} = \frac{\Delta V}{\Delta t}$$

* The typical slew rate of the 741 op-amp is 0.5 V/μsec.
* If 'S' represents the slew rate and ΔV_0 is the change in the o/p voltage, then the minimum time required

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for satisfactory operation of op-amp is given by

$$\Delta t = \frac{\Delta V_0}{S}$$

FORMULAE

1) Slew rate 'S' $= \frac{\Delta V}{\Delta t}$

2) $\Delta t = \frac{\Delta V_0}{S}$

PROBLEMS

1) Determine the typical time required for a 741 op-amp having a 10V o/p change.

Sol:- $t = \frac{\Delta V_0}{S}$.

WKT for 741 opamp

$S = 0.5\ V/\mu sec.$

Given: $\Delta V_0 = 10V$

$\therefore \Delta t = \frac{10V}{0.5\ V/\mu sec}$

$\Delta t = 20 \mu sec$

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2) Determine the typical time required for a 741 op-amp o/p to shift from its negative extreme to the positive extreme. The op-amp uses ±12V supply & has a typical slew rate of 0.5V/μsec.

Given :- $\Delta V_0 = +12V - (-12V)$

$\boxed{\Delta V_0 = 24V}$

for 741 op-amp : $\boxed{S = 0.5V/\mu sec}$

* $t = \frac{\Delta V_0}{S} = \frac{24V}{0.5V/\mu sec}$

$\therefore \boxed{t = 48\ \mu sec}$

---

3) An op-amp with slew rate of 0.5V/μsec is used in an application. find the minimum time required for the circuit to change the o/p by 7V.

Given :- $S = 0.5\ V/\mu s$, $\Delta V_0 = 7V$

Sol :- WKT $\Delta t = \frac{\Delta V_0}{S} = \frac{7V}{0.5V/\mu s}$.

$\boxed{\Delta t = 14\ \mu sec}$

---

4) In response to a square wave I/p, the o/p of an op-amp changed from −3V to +3V over a time interval of 0.25 μsec. Determine the slew rate of the op-amp.

Given :- $\Delta t = 0.25\ \mu sec$.

$\Delta V_0 = 3 - (-3) = 6V$

$S = \frac{\Delta V_0}{\Delta t} = \frac{6}{0.25\ \mu sec}$.

$\boxed{S = 24V/\mu sec}$

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4) How fast can the o/p of an op-amp change by 10V if its slew rate is 1V/μsec?

Given :- $\Delta V_o = 10V$, $S = 1V/\mu s$.

Sol :- $\Delta t = \frac{\Delta V_o}{S} = \frac{10\ V}{1V/\mu sec}$.

$\boxed{\Delta t = 10\mu sec}$

I/p bias current :-

It is defined as the average value of the individual currents flowing into the INV(-) & Non-INV(-) I/p terminals of the op-amp.

$\therefore \boxed{I_B = \frac{I_B + I_{B2}}{2}}$

For 741 :

Typical value is 80nA

Maximum value is 500nA

---

1) If the base currents for the emitter coupled transistors of a differential amplifier are 18 μA & 22 μA, determine i) I/p bias current ii) I/p offset current for an op-amp.

Given :- $I_{B1} = 18\mu A$, $I_{B2} = 22\mu A$

i) I/p bias current.

$I_B = \frac{I_{B1} + I_{B2}}{2} = \frac{18\ \mu A + 22\mu A}{2} = \underline{20\mu A}$.

ii) I/p offset current

$I_{os} = |I_{B1} - I_{B2}| = |18\ \mu A - 22\mu A| = \underline{4\mu A}$.

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Frequency limitations :-

Sketch & explain a typical gain versus, frequency graph for an op-amp. Jan-10, 4M

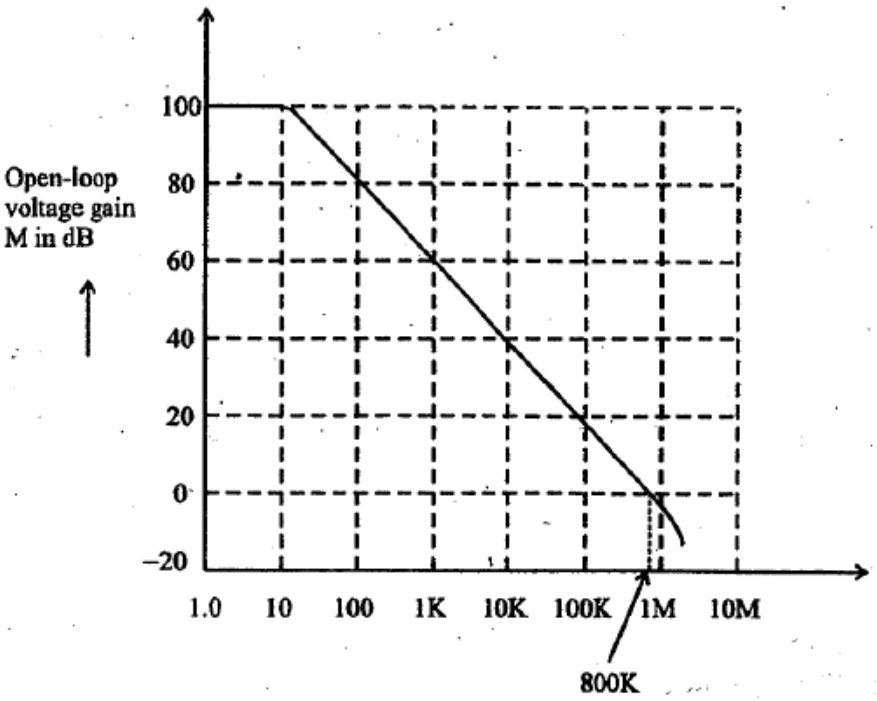

fig ① :- plot of open-loop gain M versus signal frequency 'f' for a 741 op-amp.

Fig ① : shows the graph of the open-loop gain (M) plotted versus frequency 'f' for a 741 op-amp.

The frequency is plotted to a logarithmic base & that 'M' falls linearly as 'f' increases logarithmically.

* It is seen that M is 100dB when the signal frequency is 1Hz. At 10Hz the gain has fallen below 100dB and M continues to fall as the signal frequency increases.

At $f = 100$ Hz, $M \approx 80$ dB.

At $f = 1$ KHz, $M \approx 60$ dB.

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* 'M' falls by 20dB when 'f' increases from 100Hz to 1KHz. The ten times increase in frequency is termed a decade.

So, the rate of fall of the gain is said to be 20dB per decade.

* fig ① shows that the 'M' falls to zero at approximately 800KHz

When a gain of around 80dB is required for a particular application, then the 741 op-amp is to be operated upto a frequency of 100Hz only.

When a gain of 20dB is sufficient, then the highest frequency of operation is only 90KHz.

To get larger gains at much higher frequencies, other op-amps must be used.

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OP-Amp as DC Amplifiers :-

The op-amps must be correctly biased if they are to function properly. The I/p's of most op-amps are the base terminals of the transistors in a differential amplifier.

Base currents must flow into these terminals for the transistors to be operational. consequently, the I/p terminals must be directly connected to suitable dc bias voltage source.

Bias current paths :- (DC Biasing)

* In most of the op-amp applications, the dc bias voltage to be applied to the op-amp I/p terminals will be the average value of the positive & negative supply voltages.

i.e. $\left(\frac{V_{CC}}{2} \text{ or } \frac{-V_{EE}}{2}\right)$

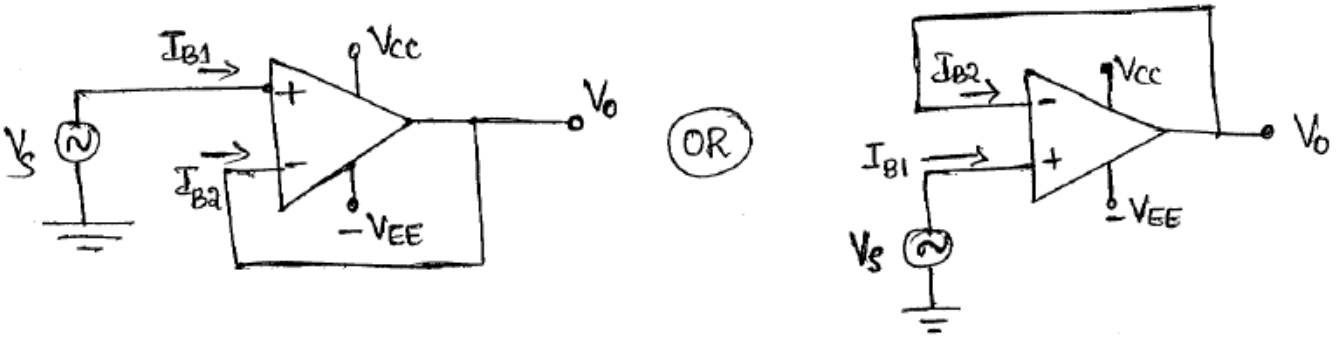

fig 1 : Directly coupled vltg follower.

* One of the two I/p terminals is usually connected to the op-amp o/p to facilitate negative feedback. The other I/p might be biased directly to ground via a signal source as shown in fig ①.

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Base current I_{B1} flows into the op-amp via the signal source while I_{B2} flows from the o/p terminal as shown in fig ①.

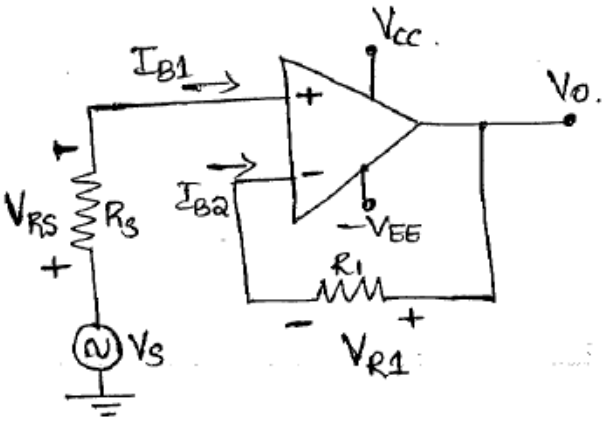

fig ②: R_1 included to match R_S

OR

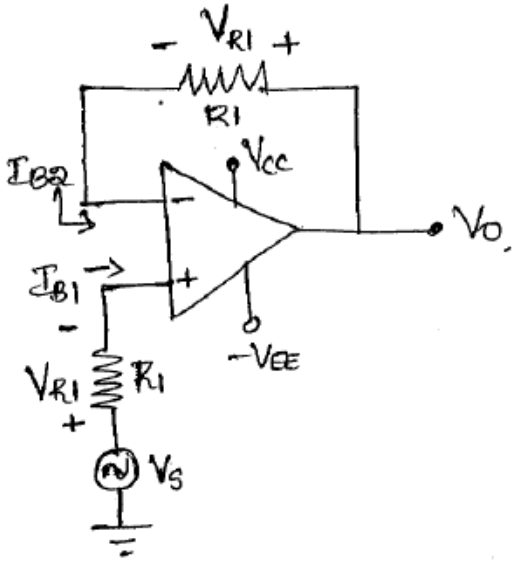

fig ③: R_1 included to match R_S.

fig ② shows a resistor 'R_1' is included in series with the inverting terminal to match signal source resistance 'R_S' in series with the non-inverting terminal.

* The op-amp I/p currents produces voltage drops

  i.e $V_{RS} = I_{B1} R_S$ &

  $V_{R1} = I_{B2} R_1$

* <u>R_S & R_1</u> should be selected as <u>equal resistors</u>. so that the resistor voltage drop are approximately equal. Any difference in these voltage drops will have the same effect as an <u>I/p offset voltage</u>.

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Maximum bias resistor values :-

In fig ②, If very small values of resistances R_S & R_1 are selected then voltage drop across them will be small. on the other hand if R_S & R_1 are very large, the voltage drop $V_{R1} = I_{B1}R_S$ & $V_{R2} = I_{B2}R_1$ might be several volts.

* For good bias stability, the maximum voltage drop across these resistors should be much smaller than the typical forward bias 'V_{BE}' drops across op-amp I/p transistors.

Usually, the voltage drop across these resistors must be made at least ten times smaller than V_{BE}.

i.e. $$I_{B(max)} \cdot R_{(max)} = \frac{V_{BE}}{10} = \frac{0.7V}{10} = 0.07V$$

For 741 op-amp $\boxed{I_{B(max)} = 500nA}$

$$I_{B(max)} \cdot R_{(max)} = 0.07V$$

$$R_{(max)} = \frac{0.07V}{I_{B(max)}} = \frac{0.07V}{500nA}$$

$$\therefore \boxed{R_{(max)} = 140k\Omega}$$

In general, $$\boxed{R_{(max)} = \frac{0.1\,V_{BE}}{I_{B(max)}}}$$

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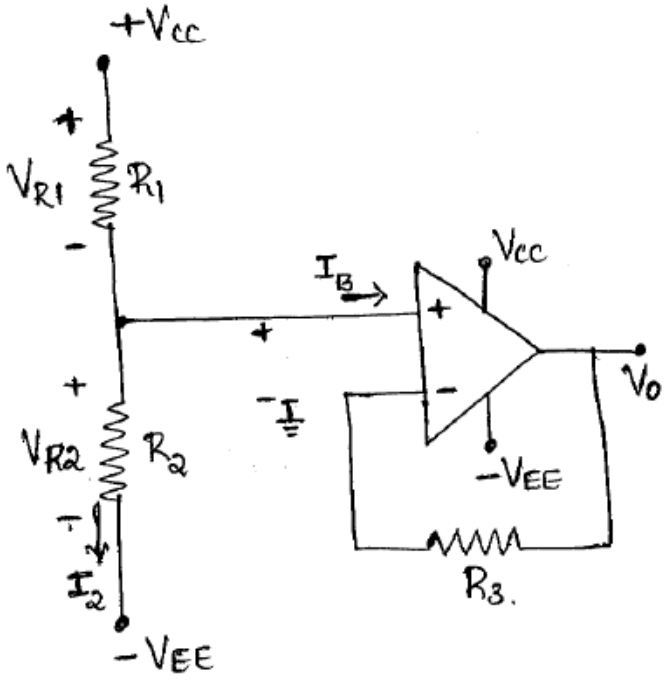
Potential divider bias :- (voltage follower potential divider bias)



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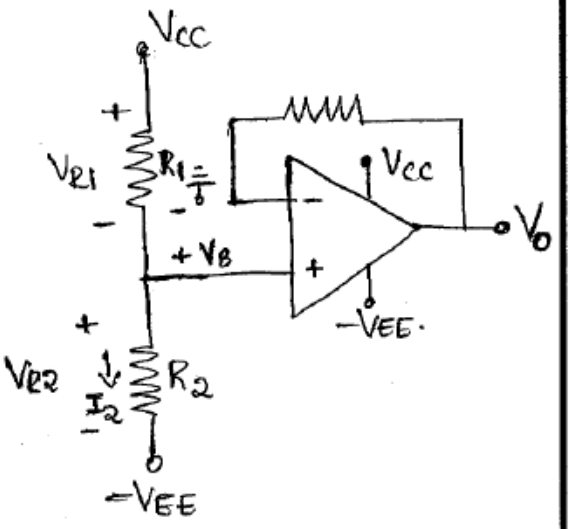

fig ① : Illustrates potential divider

fig ② : Illustrates potential divider.

fig ① shows a potential divider (R_1 & R_2) employed to derive a bias voltage from the two supply voltages, V_{CC} & $-V_{EE}$.

The potential divider current 'I_2' should be much larger than the op-amp <u>maximum I/p bias current</u>.

* Usually I_2 is made more more than 100 times the maximum bias current $I_{B(max)}$ of op-amp.

Then, $\boxed{R_1 = \frac{V_{R1}}{I_2}}$ and.

$\boxed{R_2 = \frac{V_{R2}}{I_2}}$

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From data sheet of 741 : $\boxed{I_{B(max)} = 500\,nA}$

$\therefore I_2 \geq 100\, I_{B(max)}$

$\geq 100 \times 500\,nA$

$\boxed{I_2 = 50\,\mu A}$

This is a minimum level for I_2 when 741 is used. In practice, I_2 can be chosen as high as 1mA.

* The resistance seen when looking out of the Non-INV i/p terminal in fig ① is $R_1 \| R_2$.

To equalize the voltage drop at the I/p terminals.

$$I_{B2} R_3 \approx I_{B1} (R_1 \| R_2)$$

$$\boxed{R_3 \approx R_1 \| R_2}$$

NOTE :-

For op-amp 741 : the I/p voltage range is minimum of $\pm 12\,V$ for a $\pm 15\,V$ supply.

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Potential divider bias with single polarity supply :-

OR

Voltage follower potential divider bias with single polarity supply :-

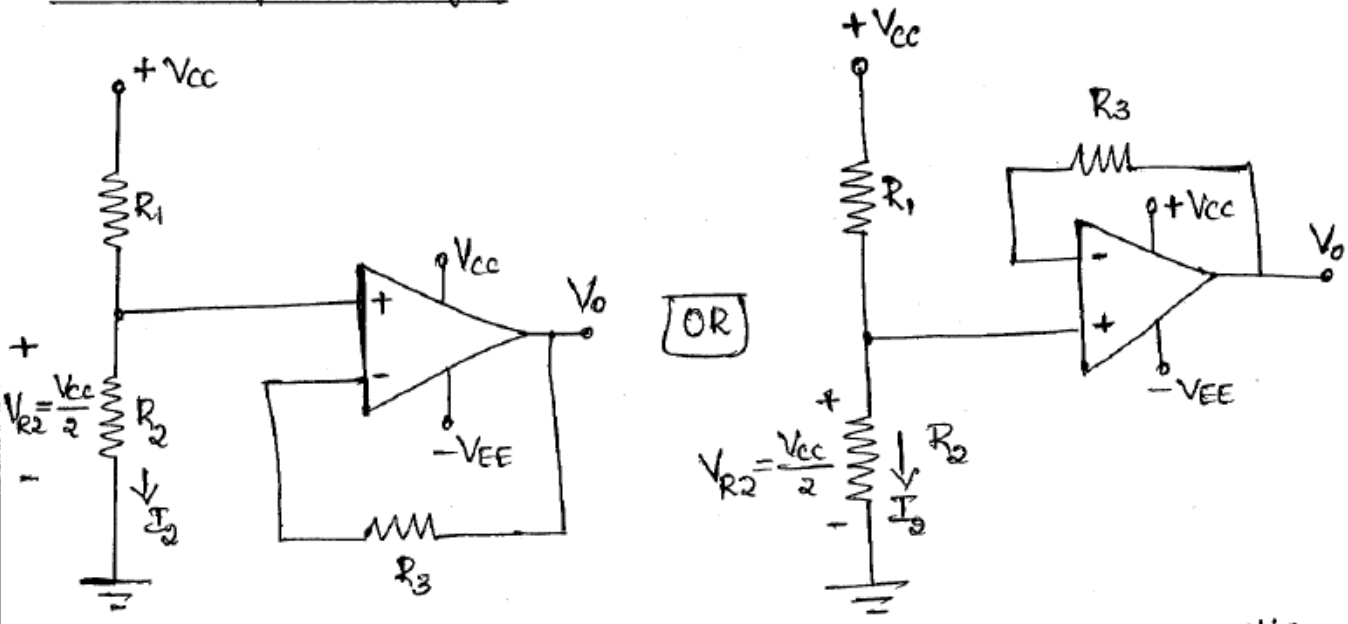

fig ③ : Voltage follower potential divider bias with single polarity supply.

* A single polarity supply voltage can be employed with an op-amp. for 741 op-amp a +30V supply can be used as shown in fig ③.

* In this case, the I/p terminal bias voltage should be approximately half the supply voltage (i.e. ≈ +15V for a 30V supply).

* V_B might be within the I/p voltage range i.e. ± 12 V for a 741 using a ±15V supply.

fig ③ is a voltage follower, the dc o/p voltage will be equal to the bias voltage level.

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Exam Questions :-

1) Explain potential divider bias for an op-amp I/p, with the necessary design steps. **June - 09, 6m**

2) Explain with circuit diagram how a dual supply op-amp can be configured to operate with single supply. **Jan - 09, 8m**

Biasing BIFET OP-Amps :-

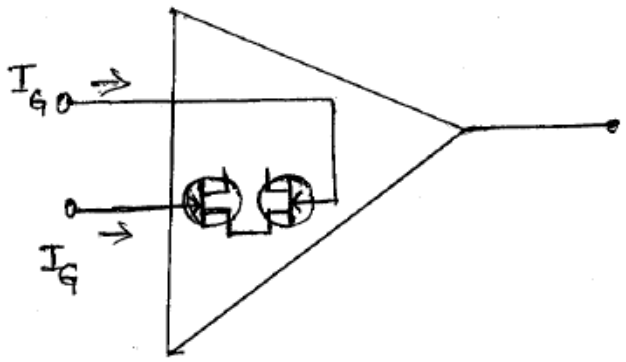

fig ① : BIFET op-amp with FET I/p stages.

* BIFET op-amps are op-amps with BIFET I/p stages as shown in fig ①. They draw very low-levels of I/p bias current i.e 50pA & offer very-high I/p impedance.

* The usual design approach of selecting resistors current $100 \times I_{B(max)}$ would result in very large values of resistors which are undesirable due to the following reasons.

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1) When the bias resistors at the gate terminal of a FET are extremely large, a charge can accumulate at the gate & this might take a relatively long time to discharge. Thus the gate voltage would not be a stable quantity & the op-amps bias conditions coould be uncertain.

2) If the bias resistors are large, then stray capacitance becomes more effective resulting in unwanted ckt oscillations.

Because of above reasons, the maximum value of resistance when looking out from the IIp of BIFET op-amps should not exceed 1MΩ.

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Directly Coupled Voltage follower :-

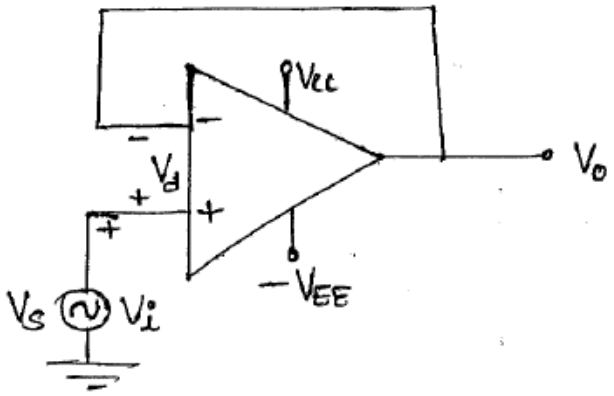

fig ① : Directly coupled voltage follower ckt.

* Without using any external components, it is possible to use op-amp as a direct coupled voltage follower circuit as shown in fig ①.

{ Due to very high open loop gain (M) of the op-amp, there will be a very very small difference b/w the I/p vtg 'V_i' & the o/p voltage V_o. }

The differential I/p should be such as to produce an o/p close to V_i & is given by:

$$V_d = \frac{V_i}{M} \longrightarrow ①$$

Where $M \rightarrow$ open loop gain of op-amp

Applying KVL from I/p to o/p

$$V_i - V_d - V_o = 0$$

$$V_o = V_i - V_d \longrightarrow ②$$

Substituting eq ① in eq ②, we get

$$V_o = V_i - \frac{V_i}{M}$$

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$$V_o = V_i \left[1 - \frac{1}{M}\right]$$

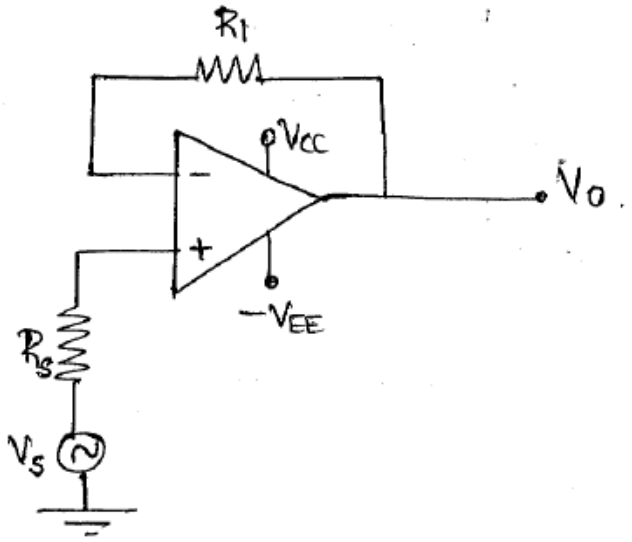

Fig ②: Directly coupled voltage follower with external resistor R_1.

In directly coupled voltage follower, the resistor R_1 is used between o/p & inverting terminal to match the source resistance R_s.

* Let maximum values of I_{B1} & I_{B2} are $I_{B1(max)}$ & $I_{B2(max)}$, then the maximum voltage drop across each resistor is

$$I_{B1(max)} R_s = I_{B2(max)} \cdot R_1$$

* The I/p offset voltage produced is given by

$$V_{ios} = I_{ios} \times (R_s \text{ or } R_1)$$

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* The I/p impedance of voltage follower is given by, $Z_{in} = (1+M)Z_i$ $\because \boxed{\beta = 1}$

* The o/p impedance is given by:

$$Z_{out} = \frac{Z_o}{(1+M)} \quad \because \boxed{\beta = 1}$$

NOTE :- for voltage follower $\beta = 1$

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Performance :-

Reducing loading effect using voltage follower :-

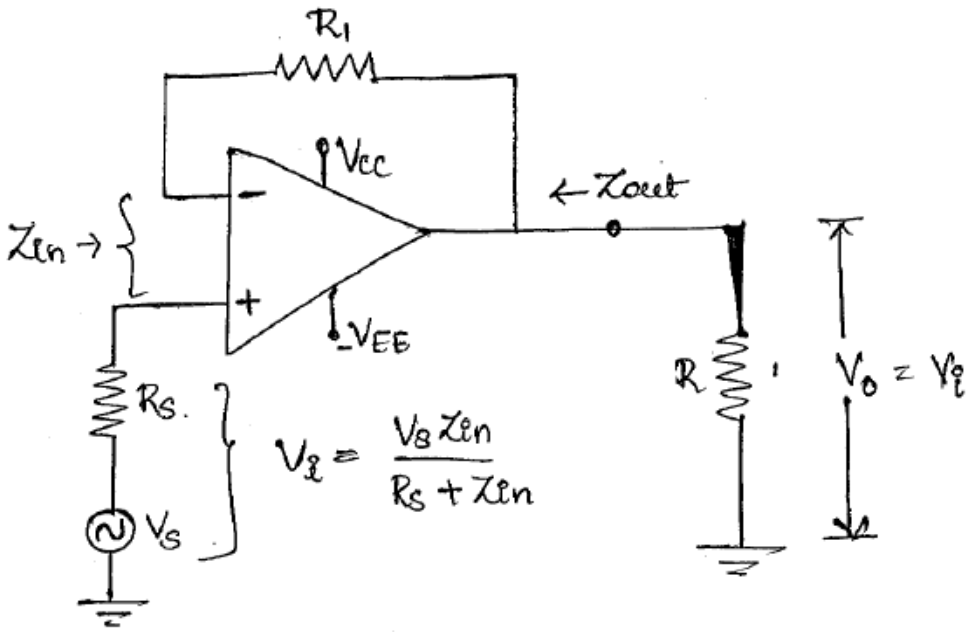

fig ① ⓐ : The high I/p impedance of the voltage follower prevents any significant signal loss.

* The I/p impedance of a voltage follower is very high & is given by

$$Z_{in} = [1 + M]\, Z_i \qquad \because \boxed{\beta = 1}$$

* The o/p impedance of a voltage follower is very low & is given by :

$$Z_{out} = \frac{Z_o}{(1+M)} \qquad \because \boxed{\beta = 1}$$

* Because of high Zin & low Zout, voltage follower is used to convert high impedance source to a low o/p impedance thus acting as a Buffer.

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Thus voltage follower is also called as Buffer amplifier

* The load voltage is given by

$$V_L = I R_L$$

where,

$$V_L = \frac{V_o}{R_L + Z_{out}} \cdot R_L$$

$$I = \frac{V_o}{R_L + Z_{out}}$$

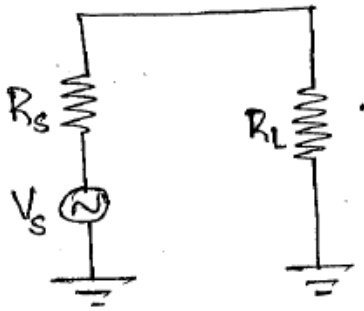
* I_{out} is normally much smaller than any load resistance. i.e. $R_L \gg Z_{out}$. Thus neglecting Z_{out}

$$V_L = \frac{V_o}{\cancel{R_L}} \cdot \cancel{R_L}$$

$$V_L = V_o$$

Thus there is effectively no signal loss & all of o/p voltage V_o appears across load resistance.

* Consider that load resistor R_L is directly connected to the source as shown in fig ② below



$$V_L = \frac{V_s}{R_s + R_L} \cdot R_L$$

fig ②: part of signal is lost when a load is directly connected.

* The load voltage is given by:

$$V_L = I R_L$$

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$$V_L = \frac{V_s}{R_s + R_L} \cdot R_L$$

Where,
$$I = \frac{V_s}{R_s + R_L}$$

thus some part of V_s gets lost, when load is directly connected.

Directly coupled voltage follower ckt.

FORMULAE

1) Maximum voltage drop across each resistor
   i) $I_{B1(max)} R_s$
   ii) $I_{B2(max)} R_1$

2) I/p offset voltage produced by the I/p offset current.

$$V_{i(offset)} = I_{i(offset)} \times (R_s \text{ or } R_1)$$

3) I/p Impedance : $Z_{in} = (1+M) Z_i$

4) o/p Impedance : $Z_{out} = \frac{Z_o}{(1+M)}$

5) I/p voltage : $V_i = \frac{V_s \times Z_{in}}{R_s + Z_{in}}$

6) Load voltage :
   i) When load is directly connected to source

$$V_L = \frac{V_s \times R_L}{R_s + R_L}$$

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ii) When the vtg follower is b/w the load & the source.

$$V_L = \frac{V_o \times R_L}{R_L + Z_{out}}$$

7) o/p voltage : $V_o = V_i \left(1 - \frac{1}{M}\right)$

8) $\beta = 1$

PROBLEMS

1) A voltage follower using a 741 op-amp is connected to a signal source via a 47kΩ resistor as shown in fig ①. select a suitable value for resistor R_1. Also, calculate the maximum voltage drop across each resistor & the maximum I/p offset voltage produced by the I/p offset current.

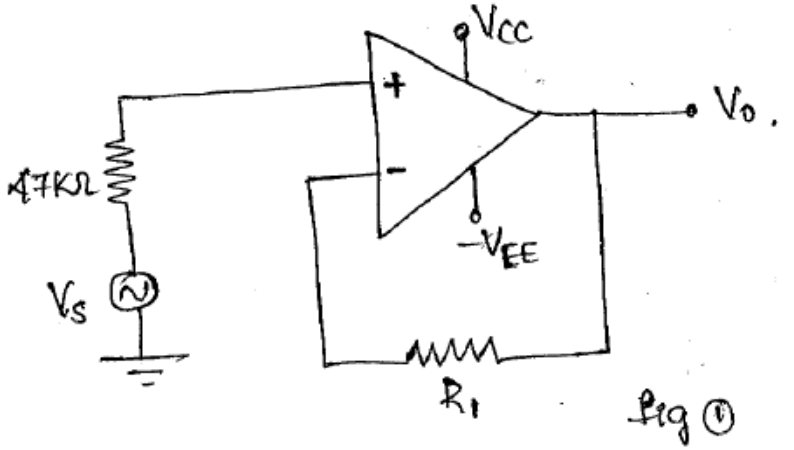

fig ①

Sol : Given $R_s = 47\,k\Omega$ $\therefore$ $R_s = R_1 = 47\,k\Omega$

For op-amp 741, $I_{B(max)} = 500\,nA$ &

$I_{os} = 20\,nA$

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* The voltage drop across each resistor is

$$I_{B1(max)} \cdot R_S = I_{B2(max)} \cdot R$$
$$= 500\,nA \times 47K\Omega$$
$$= 23.5\,mV$$

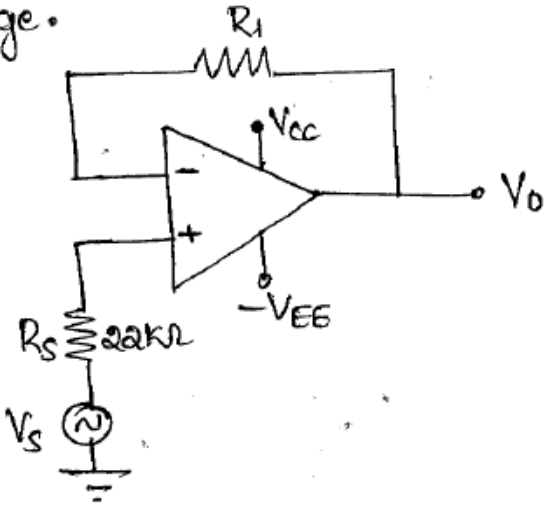
* I/p offset voltage

$$V_{i(offset)} = I_{i(offset)} * (R_S \text{ or } R_1)$$
$$= 20\,nA \times 47K\Omega$$

$$\boxed{V_{i(offset)} = 0.94\,mV}$$

---

2) For the voltage follower circuit shown in fig① select the value of R_1, calculate the maximum voltage drop across each resistor & maximum input offset voltage.



Given : $R_S = 22K\Omega$

for op-amp 741 : $I_{B(max)} = 500\,nA$

$I_{IOS} = 20\,nA$

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Sol :-

* For matching the voltage drops, R_1 must be selected equal to R_S

$$\therefore \boxed{R_1 = R_S = 22K\Omega}$$

* The voltage drop across each resistor is.

$$I_{B1(max)} \cdot R_S = I_{B2(max)} R_1 = 500nA \times 22K\Omega = \underline{11mV}$$

* I/p offset voltage :

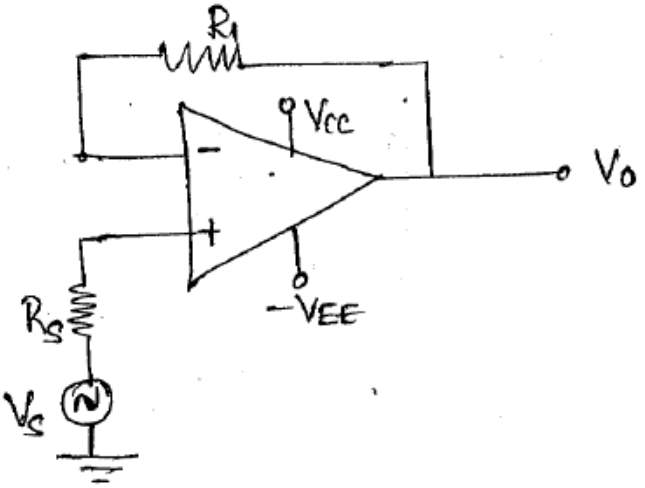
$$V_{ios} = I_{i(offset)} \times (R_S \text{ or } R_1)$$

$$= 20nA \times 22K\Omega$$

$$\boxed{V_{i(offset)} = 0.44mV} \qquad \{V_{ios} = V_{i(offset)}\}$$

---

3) A signal source with a resistance of 15 KΩ is connected to a LM 108 op-amp working as a direct coupled voltage follower of fig ①. Select a suitable value for R_1 & determine the maximum voltage drop across each resistor. Also determine the maximum I/p offset voltage produced by the I/p offset current. Assume $I_{B(max)} = 2nA$ & $I_{i(offset)} = 0.2nA$ for LM 108 op-amp.



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Given : $R_s = 15\,K\Omega$, $I_{B(max)} = 2nA$, $I_{I(offset)} = 0.2\,nA$.

Sol :-

* The value of R_1 is chosen same as equal to R_s

$$\therefore \boxed{R_s = R_1 = 15K\Omega}$$

* Maximum voltage drop across each resistor

$$= I_{B(max)} \cdot R_1 = I_{B(max)} \cdot R_s = 2\times10^{-9} \times 15 \times 10^{3} = \underline{30\mu V}$$

* Maximum I/p offset voltage :

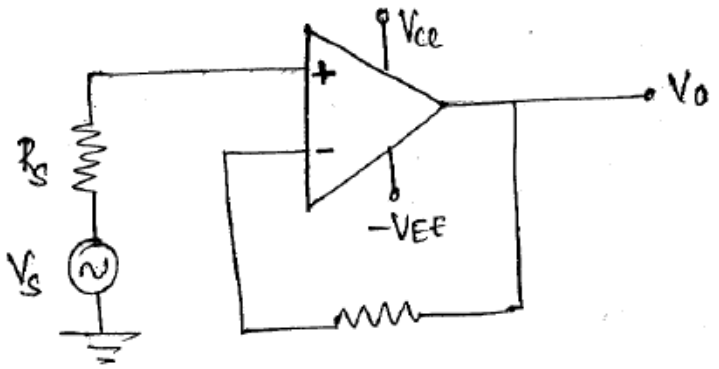
$$V_{I(offset)} = I_{I(offset)} \times (R_1 \text{ or } R_s)$$

$$= 0.2\times10^{-9} \times 15 \times 10^{3}$$

$$\boxed{V_{I(offset)} = 3\,\mu V}$$

---

4) A voltage follower using a 741 op-amp is connected to a signal source via a 50KΩ resistor, as in fig (a). Select a suitable value for resistor R_1. Also calculate the maximum voltage drop across each resistor & the maximum I/p offset voltage produced by the I/p offset current.



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Given : $R_S = 50\,k\Omega$

For op-amp 741 : $I_{B(max)} = 500\,nA$ & $I_{IOS} = 20\,nA$

Sol:-

* The value of R_1 is chosen same as equal to R_S

$$\therefore \boxed{R_S = R_1 = 50\,k\Omega}$$

* Maximum voltage drop across each resistor

$$= I_{B(max)} R_1 = I_{B(max)} R_S = 2 \times 10^{-9} \times 50 \times 10^3 = \underline{25mV}$$

* Maximum I/p offset voltage :

$$V_{i(offset)} = I_{I(offset)} \times (R_1 \text{ or } R_S)$$

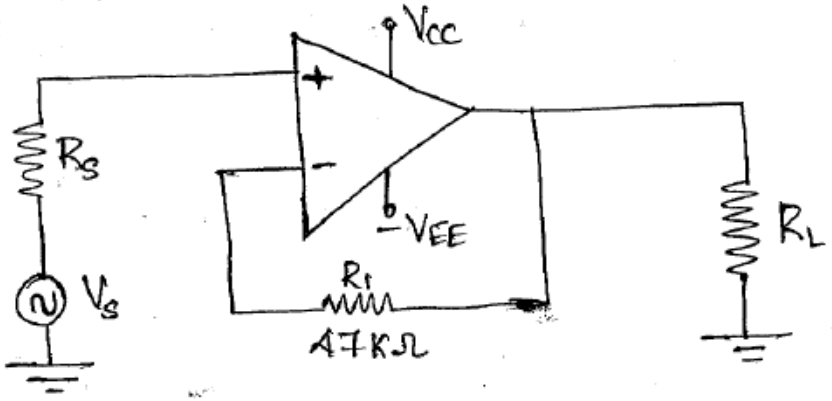
$$= 20nA \times 50\,k\Omega$$

$$\boxed{V_{i(offset)} = 1\,mV}$$

5) The voltage follower in fig ① has a 1V signal & a 20kΩ load. Calculate the load voltage.

ⓐ When the load is directly connected to source.

ⓑ When the voltage follower is between the load & the source.



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Given :- $V_s = 1V$, $R_1 = 47K\Omega$, $R_L = 20K\Omega$

For 741 op-amp : $M = 200000$, $Z_i = 2M\Omega$ & $Z_o = 75\Omega$.

a) When the load is directly connected to the source

$$V_L = \frac{V_s \times R_L}{R_s + R_L} = \frac{1V \times 20K\Omega}{47K\Omega + 20K\Omega}$$

$$\boxed{V_L = 298\,mV}$$

b) When the voltage follower is between the load & the source :

$$V_i = \frac{V_s \times Z_{in}}{R_s + Z_{in}}$$

$$Z_{in} = (1+M)\,Z_i = (1+200000)\,2M\Omega$$

$$\boxed{Z_{in} = 4\times10^{11}\,\Omega}$$

$$\therefore \quad V_i = \frac{1V \times (4\times10^{11}\,\Omega)}{47K\Omega + 4\times10^{11}\,\Omega}$$

$$\boxed{V_i = 1V}$$

* $V_o = V_i\left(1 - \frac{1}{M}\right) = 1V\left(1 - \frac{1}{200000}\right)$ $\therefore \boxed{V_o = 1V}$

* o/p Impedance : $Z_{out} = \frac{Z_o}{(1+M)} = \frac{75\Omega}{(1+200000)} = \underline{\underline{37\times10^{-5}\,\Omega}}$

* Load voltage : $V_L = \frac{V_o \times R_L}{R_L + Z_{out}} = \frac{1V \times 20K\Omega}{20K\Omega + (37\times10^{-5}\Omega)} = \underline{\underline{1V}}$

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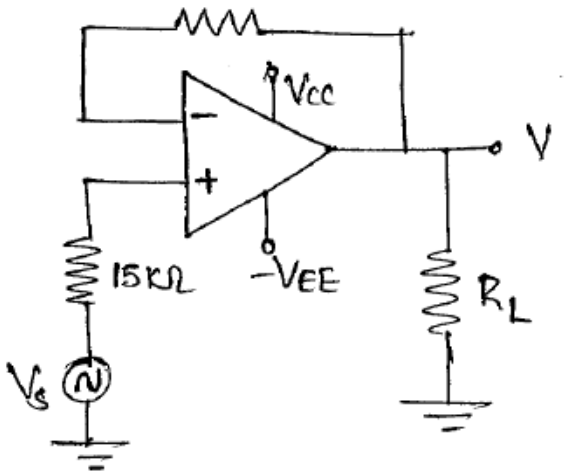
6) If the voltage follower of fig ① has a 200mV I/p signal & a 5kΩ load, determine the load voltage
i) When the load is directly connected to the source.
ii) When the voltage follower is used. for LM 108, $M = 3,00,000$, $Z_i = 70M\Omega$ and $Z_o = 75\Omega$



Given :- $V_s = 200mV$, $R_s = 15k\Omega$, $R_L = 5k\Omega$, $M = 300000$.
$Z_i = 70M\Omega$ & $Z_o = 75\Omega$

i) When the load is directly connected to the source

$$V_L = \frac{V_s R_L}{R_s + R_L} = \frac{200mV \times 5k\Omega}{15k\Omega + 5k\Omega}$$

$$\boxed{V_L = 50mV}$$

ii) When the voltage follower is between the load & the source :

$$V_i = \frac{V_s * Z_{in}}{R_s + Z_{in}}$$

$$Z_{in} = (1+M) Z_i = (1+300000)\ 70 \times 10^6.$$

$$\boxed{Z_{in} = 2.1 \times 10^{13}\Omega}$$

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* $V_i = \frac{V_s \times Z_{in}}{R_s + Z_{in}} = \frac{(200\,mV) \times (2.1 \times 10^{13})}{15 \times 10^3 + 2.1 \times 10^{13}}$

$$\boxed{V_i = 200\,mV}$$

* $V_o = V_i \left(1 - \frac{1}{M}\right) = 200mV \left(1 - \frac{1}{300000}\right)$

$$\boxed{V_o = 200mV}$$

* $Z_{out} = \frac{Z_o}{(1+M)} = \frac{75\,\Omega}{(1+300000)}$

$$\boxed{Z_{out} = 2.5 \times 10^{-4}\,\Omega}$$

* The load voltage is given by:

$$V_L = \frac{V_o \times R_L}{R_L + Z_{out}} = \frac{200\,mV \times 5 \times 10^3}{5 \times 10^3 + 2.5 \times 10^{-4}}$$

$$\boxed{V_L = 200mV}$$

---

7) A load resistance of 22KΩ is to be connected to a source of 1.5V with source resistance of 56KΩ. Calculate the load voltage if

i) Load is directly connected.

ii) Load is connected through voltage follower using 0-p op-amp with $Z_o = 75\Omega$, $Z_i = 2M\Omega$ & $M = 2 \times 10^5$.

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Given :- $R_L = 22K\Omega$, $R_S = 56K\Omega$, $V_S = 1.5V$, $Z_o = 75V$, $Z_i = 2M\Omega$ & $M = 2\times10^5$.

Sol :- i) When load is directly connected :

$$V_L = \frac{V_S R_L}{R_S + R_L} = \frac{1.5V \times 22K\Omega}{56K\Omega + 22K\Omega}$$

$$\boxed{V_L = 0.42307V}$$

ii) When load is connected through voltage follower:

* $Z_{in} = (1+M) Z_i = (1 + 2\times10^5) 2\times10^6$

$$\boxed{Z_{in} = 4\times10^{11}\Omega}$$

* $V_i = \frac{V_S \times Z_{in}}{R_S + Z_{in}} = \frac{1.5V \times 4\times10^{11}}{56\times10^3 + 4\times10^{11}} = 1.4999V$

$$\boxed{V_i \approx 1.5V}$$

* $V_o = V_i \left[1 - \frac{1}{M}\right] = 1.5V \left(1 - \frac{1}{2\times10^5}\right)$

$$\boxed{V_o = 1.4999V}$$

* $Z_{out} = \frac{Z_o}{1+M} = \frac{75\Omega}{1 + 2\times10^5} = \underline{3.7499\times10^{-4}\Omega}$

* $V_L = \frac{V_o R_L}{R_L + Z_{out}} = \frac{1.4999 \times 22\times10^3}{22\times10^3 + 3.7499\times10^{-4}} = \underline{1.4999V}$

$$\boxed{V_L \approx 1.4999V}$$

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Voltage follower using potential divider bias :-

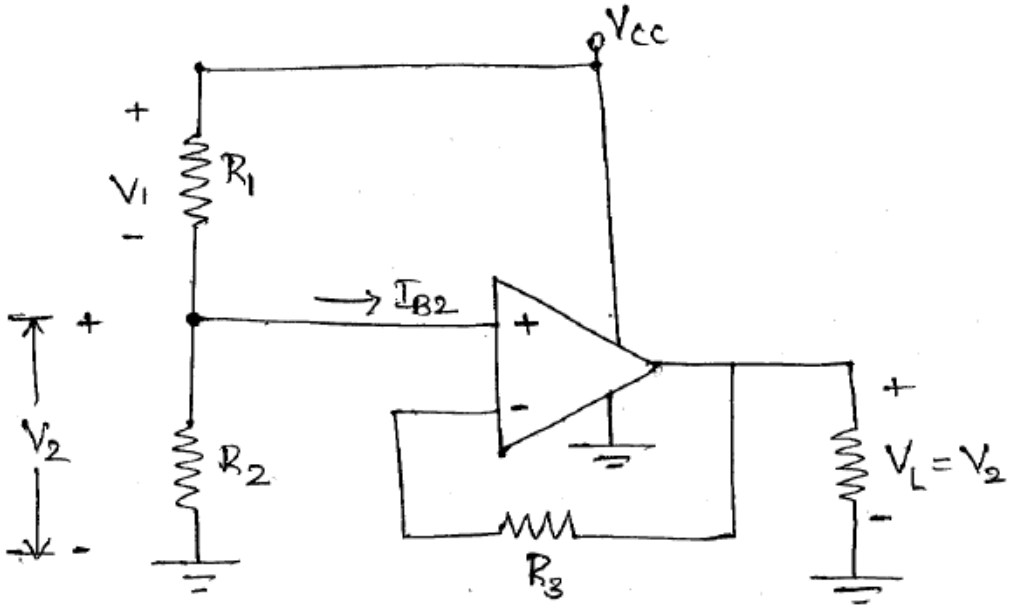

fig 1 @ : A potential divider & voltage follower produces a constant V_L.

{

OR

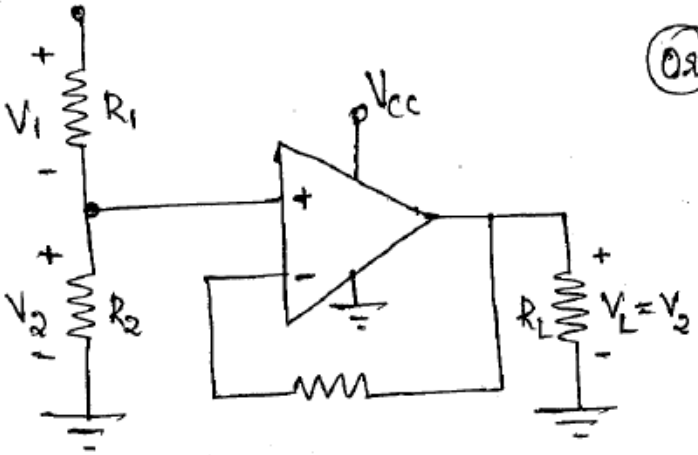

fig 1 @

Or

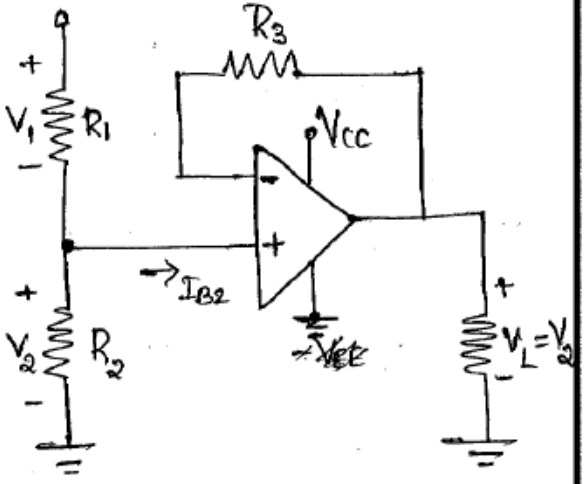

fig 1 @

}

A potential divider bias can be used to bias a voltage follower circuit as shown in fig ① @ with negative supply terminal of op-amp being grounded.

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The presence of the voltage follower maintains the load voltage constant regardless of the load resistor value.

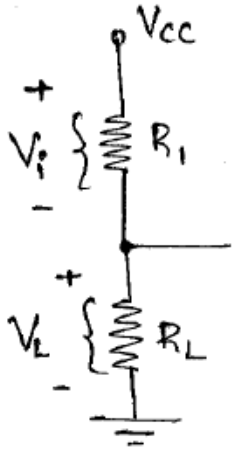
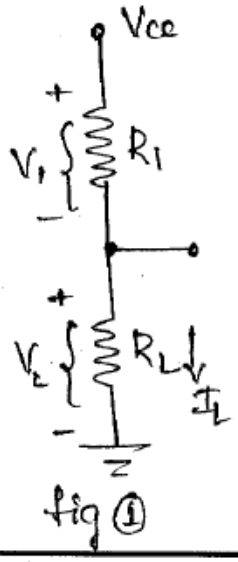


fig 1 ⓑ shows load R_L directly connected to supply through R_1 without using voltage follower.

In fig 1 ⓑ, load R_L is directly connected in series with resistor R_1 to derive a voltage V_L from the supply V_{cc}. The arrangement has the disadvantage that the load varies if the load resistance changes.

Design procedure :-

i) A potential divider bias directly connected to load 'R_L' (without voltage divider)



1) $I_L = \frac{V_L}{R_L}$

2) Applying KVL to the ckt

$V_{cc} - V_1 - V_L = 0$

$$\boxed{V_1 = V_{cc} - V_L}$$

3) $R_1 = \frac{V_1}{I_L}$

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4) $V_L = I_L R_L$

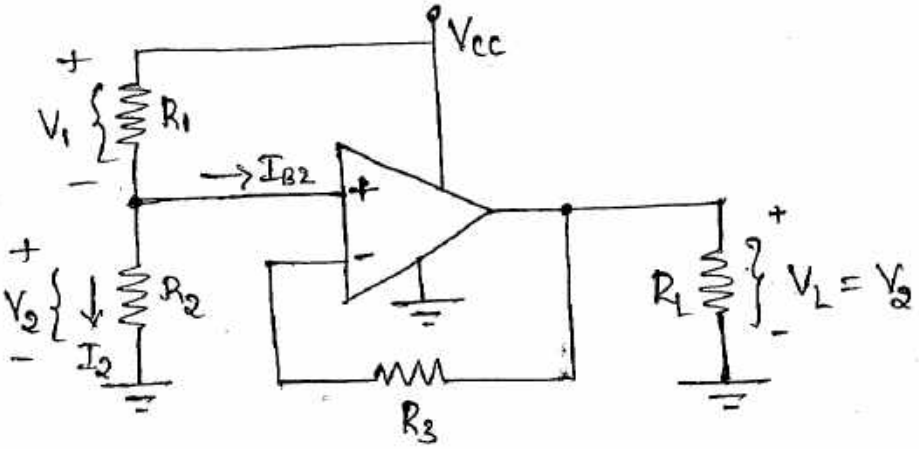
where $I_L = \dfrac{V_{cc}}{R_1 + R_L}$

$$\therefore V_L = \frac{V_{cc} R_L}{R_1 + R_L}$$

5) When R_L changes (say -10%).

$$V_L = \frac{V_{cc}\,(R_L - 10\%\text{ of } R_L)}{R_1 + (R_L - 10\%\text{ of } R_L)}$$

ii) potential divider bias used to bias voltage follower.



1) $V_2 = V_L$

2) $V_1 = V_{cc} - V_L$

3) $I_2 = 100\, I_{B(max)}$

4) $R_2 = \dfrac{V_2}{I_2}$

5) $R_1 = \dfrac{V_1}{I_2}$.

6) when R_L changes (by say -10%)

$$\boxed{V_L = V_2}$$

7) $R_3 = R_1 \,||\, R_2$.

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1) A 1KΩ load is to have 5V developed across it from a 15V source. Design suitable circuits & calculate the load voltage variation in each case when the load resistance varies by -10%. Use a 741 op-amp.

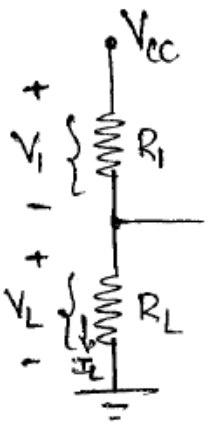

fig 1 @

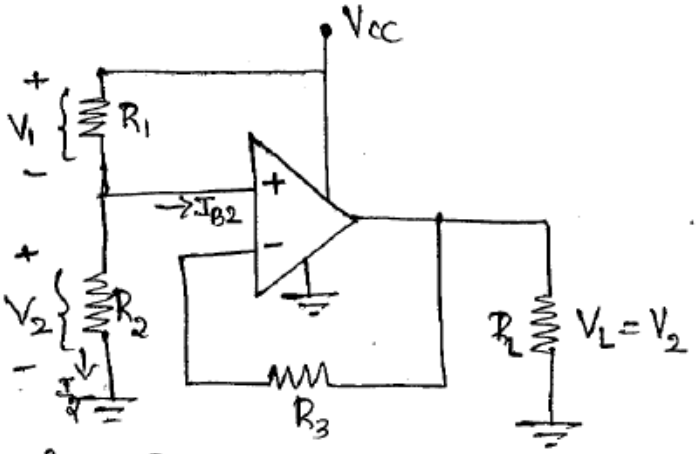

fig 1 (b)

Given :-

$R_L = 1K\Omega$, $V_L = 5V$, $V_{cc} = 15V$.

Sol :-

1) For fig 1 @ :

* $I_L = \frac{V_L}{R_L} = \frac{5V}{1K\Omega} = 5mA$ $\therefore$ $\boxed{I_L = 5mA}$

* $V_1 = V_{cc} - V_L = 15V - 5V = 10V$ $\therefore$ $\boxed{V_1 = 10V}$

* $R_1 = \frac{V_1}{I_L} = \frac{10V}{5mA} = 2K\Omega$ $\therefore$ $\boxed{R_1 = 2K\Omega}$

* When R_L changes by -10 %

$$V_L = \frac{V_{cc} * (R_L - 10\% \text{ of } R_L)}{R_1 + (R_L - 10\% \text{ of } R_L)} = \frac{15V \times (1K\Omega - 100\Omega)}{2K\Omega + (1K\Omega - 100\Omega)}$$

$$= \frac{15V \times 900\Omega}{2900\Omega}$$

$$\boxed{V_L = 4.655V}$$

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ii) For fig 1 (b): Here $V_L = V_2 = 5V$

WKT for op-amp 741 : $I_{B(max)} = 500nA$

* Let $I_2 = 100 \times I_{B(max)} = 100 \times 500nA = 50\mu A$

$$\boxed{I_2 = 50\mu A}$$

* $R_2 = \frac{V_2}{I_2} = \frac{5V}{50\mu A}$

$$\boxed{R_2 = 100K\Omega}$$

* $R_1 = \frac{V_1}{I_2} = \frac{10V}{50\mu A}$

$$\boxed{R_1 = 200K\Omega}$$

* When R_L changes by -10%

$V_L = V_2 = 5V$ $\therefore$ $\boxed{V_L = 5V}$

* $R_3 = R_1 \| R_2 = 200K\Omega \| 100K\Omega$

$$\boxed{R_3 = 66.66K\Omega}$$

---

2) A voltage of 3 volts is needed across a load resistor of value 12 KΩ. The supply voltage available is +24 volts. Design the resistor values in the circuits of fig 1 & fig (2) and determine the load voltage variation in each case when the load resistance increases by 20%. Use op-amp with parameters: $I_{B(max)} = 500mA$, $Z_0 = 75\Omega$, $M = 2 \times 10^5$.

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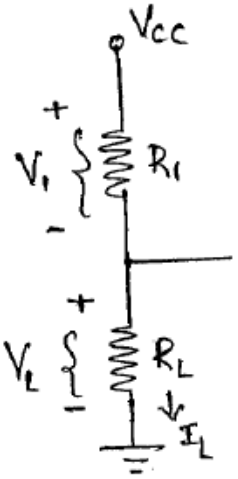

fig ①

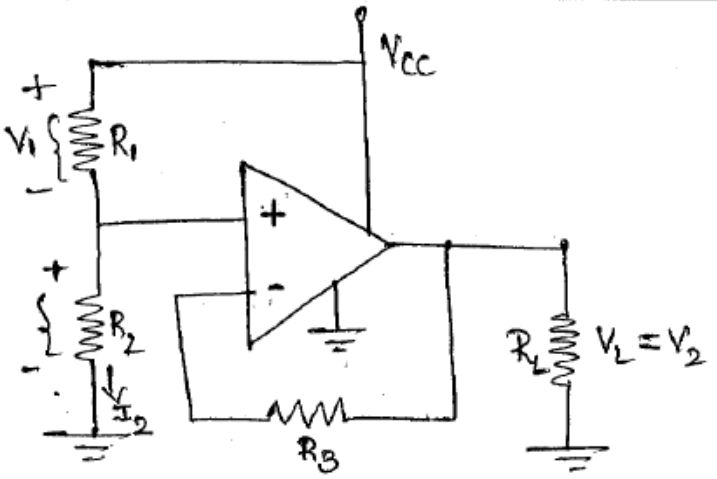

fig ②

Given :- $V_L = 3V$, $R_L = 12k\Omega$, $V_{cc} = 24V$

$I_{B(max)} = 500nA$, $Z_o = 75\Omega$, $M = 2 \times 10^5$

Sol :-

i) For fig ①

* $I_L = \frac{V_L}{R_L} = \frac{3V}{12k\Omega} = 250\mu A$ $\therefore$ $\boxed{I_L = 250\mu A}$

* $V_1 = V_{cc} - V_L = 24V - 3V$. $\boxed{V_1 = 21V}$

* $R_1 = \frac{V_1}{I_L} = \frac{21V}{250\mu A} = 84k\Omega$ $\boxed{R_1 = 84k\Omega}$

* When R_L changes by +20%

i.e $R_L = 12k\Omega + (0.2 \times 12k\Omega) = 14.4k\Omega$

$\boxed{R_L = 14.4k\Omega}$

$V_L = \frac{V_{cc} \cdot R_L}{R_1 + R_L} = \frac{24V \times 14.4k\Omega}{84k\Omega + 14.4k\Omega}$

$\boxed{V_L = 3.51V}$

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ii) for fig ② : Here $V_L = V_2 = 3V$

$$V_1 = V_{CC} - V_L = 24V - 3V = 21V$$

* Let $I_2 = I_{B(max)} \times 100$

$= 100 \times 500nA$

$$\boxed{I_2 = 50\ \mu A}$$

* $R_2 = \frac{V_2}{I_2} = \frac{3V}{50\ \mu A} = 60\ k\Omega$ $\therefore \boxed{R_2 = 60\ k\Omega}$

* $R_1 = \frac{V_1}{I_2} = \frac{21V}{50\ \mu A} = 420\ k\Omega$ $\therefore \boxed{R_1 = 420\ k\Omega}$

* $R_3 = R_1 \parallel R_2 = \frac{420k\Omega \times 60k\Omega}{420k\Omega + 60k\Omega} = 52.5k\Omega$

$$\boxed{R_3 = 52.5\ k\Omega}$$

* When R_L changes by $+20\%$

$V_L = V_2 = 3V$

$\therefore \boxed{V_L = 3V}$

---

3) It is required to obtain 2V across 1kΩ load from 10V supply voltage. Design the circuits without & with voltage follower. Hence calculate the change in load voltage if R_L changes by -5%. Use 741 op-amp.

Given: $R_L = 1k\Omega$, $V_L = 2V$, $V_{CC} = 10V$.

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For op-amp 741 : $I_{B(max)} = 500nA$

1) potential divider without using voltage divider.

* $I_L = \frac{V_L}{R_L} = \frac{2V}{1K\Omega} = 2mA$ $\therefore$ $\boxed{I_L = 2mA}$

* $V_1 = V_{cc} - V_L = 10V - 2V = 8V$ $\therefore$ $\boxed{V_1 = 8V}$

* $R_1 = \frac{V_1}{I_L} = \frac{8V}{2mA} = 4K\Omega$ $\therefore$ $\boxed{R_1 = 4K\Omega}$

* When R_L changes by -5%

$R_L = R_L - (5\% \text{ of } R_L) = 1K\Omega - 50\Omega$

$\boxed{R_L = 950\Omega}$

$V_L = \frac{V_{cc} \cdot R_L}{R_1 + R_L} = \frac{10V \times 950\Omega}{4K\Omega + 950\Omega} = 1.9191V$

ii) potential divider bias with voltage follower

Here $V_2 = V_L = 2V$

* $I_2 = 100 \times I_{B(max)} = 100 \times 500nA = 50\mu A$

$\boxed{I_2 = 50\mu A}$

* $R_2 = \frac{V_2}{I_2} = \frac{2V}{50\mu A}$ $\therefore$ $\boxed{R_2 = 40K\Omega}$

* $R_1 = \frac{V_1}{I_2}$.

$V_1 = V_{cc} - V_L = 10V - 2V$

$\boxed{V_1 = 8V}$

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$$R_1 = \frac{V_1}{I_2} = \frac{8V}{50\mu A} = 160K\Omega \quad \therefore \boxed{R_1 = 160K\Omega}$$

* When R_L changes by -5%.

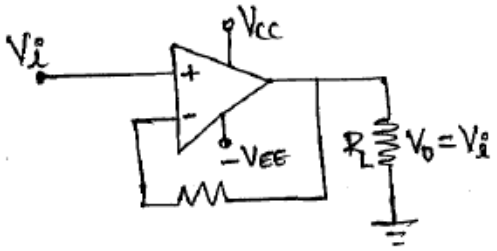
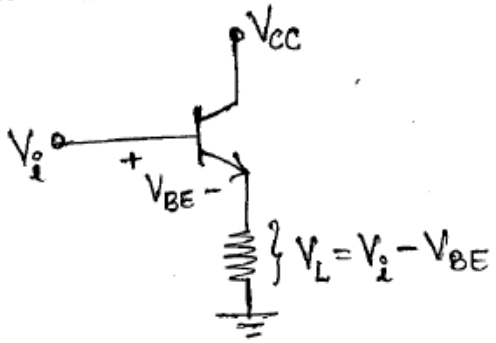
$$V_L = V_2 = 2V$$

$$\therefore \boxed{V_L = 2V}$$

---

* Comparison of voltage follower and Emitter follower :-.
* Compare a voltage follower and an emitter follower.

June -08, 4M

Voltage follower	Emitter follower
1) 	1) 
2) Voltage follower are buffer amplifier.	2) Emitter follower are also buffer amplifier.
3) Much higher I/p impedance than emitter follower	3) I/P impedance is lesser than voltage follower.
4) Much lower O/p impedance than emitter follower	4) O/p impedance is higher than voltage follower.
5) The dc loss is $\frac{V_i}{M}$ which is very small.	5) The dc loss is the voltage drop of the transistor ie V_{BE}
6) AC signal voltage loss is very less compared to emitter follower	6) AC signal voltage loss is more than voltage follower

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Directly - coupled Non - Inverting amplifiers :-

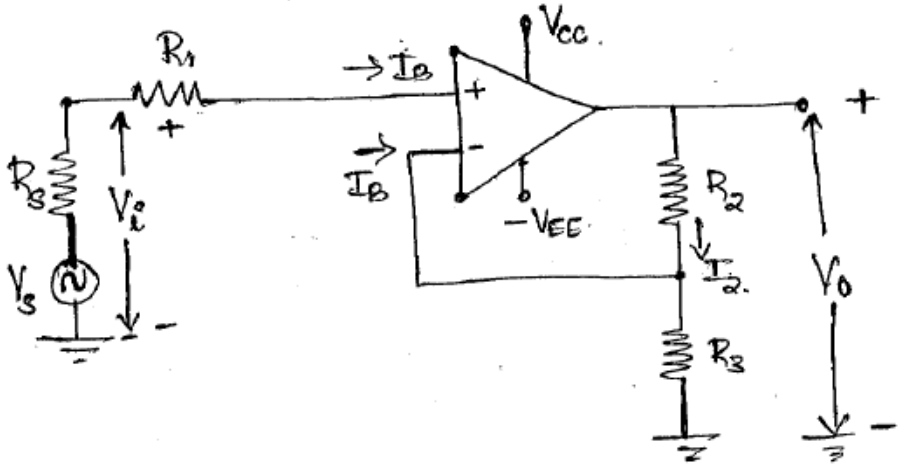

fig ①: Directly - coupled Non-INV amplifier.

* the voltage gain of NON-INV amplifier is

$$A_V = \frac{R_2 + R_3}{R_3} \qquad \therefore A_V = 1 + \frac{R_2}{R_3}$$

Design steps :-

1) The potential divider resistor values are determined by using V_i, V_o and I_2

* $R_3 = \frac{V_{R3}}{I_2}$ but $V_{R3} = V_i$ $\therefore R_3 = \frac{V_i}{I_2}$

* The o/p voltage 'V_o' appears across $(R_2 + R_3)$

Applying KVL to o/p circuit

$$V_o - I_2R_2 - I_2R_3 = 0.$$

$$V_o = I_2(R_2 + R_3)$$

$$R_2 + R_3 = \frac{V_o}{I_2}.$$

$$\therefore R_2 = \frac{V_o}{I_2} - R_3$$

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2) To equalize the $I_B R$ voltage drop at the op-amp I/p's, R_1 is calculated as :

$$R_1 = (R_2 \parallel R_3)$$

3) If R_1 as determined from above equation is not very much larger than the source resistance i.e $R_1 \ll R_s$ then,

$$(R_s + R_1) = (R_2 \parallel R_3)$$

PROBLEMS

1) Using a 741 op-amp, design a non-inverting amplifier to have a voltage gain of approximately 66. The signal amplitude is to be 15 mV.

Given : $A_V = 66$, $V_i = 15\,mV$

For 741 op-amp : $I_{B(max)} = 500\,nA$.

Sol :

Let $I_2 = 100 \times I_{B(max)}$

$= 100 \times 500\,nA$

$$I_2 = 50\,\mu A$$

* $R_3 = \frac{V_i}{I_2} = \frac{15mV}{50\mu A} = 300\,\Omega$ $\therefore$ $R_3 = 300\,\Omega$

* Use a standard value resistor i.e $R_3 = 270\,\Omega$

Now I_2 level changes i.e.

I_2 becomes $I_2 = \frac{V_i}{R_3} = \frac{15mV}{270\,\Omega}$

$$I_2 = 55.6\,\mu A$$

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* WKT $A_V = \frac{V_0}{V_i}$

$V_0 = A_V V_i = 66 \times 15\,mV$

$\boxed{V_0 = 990\,mV}$

* $R_2 + R_3 = \frac{V_0}{I_2}$

$R_2 = \left(\frac{V_0}{I_2} - R_3\right) = \left(\frac{990\,mV}{55.6\,\mu A} - 270\Omega\right)$

$R_2 = 17.80\,K\Omega - 270\Omega$

$\boxed{R_2 = 17.53\,K\Omega}$

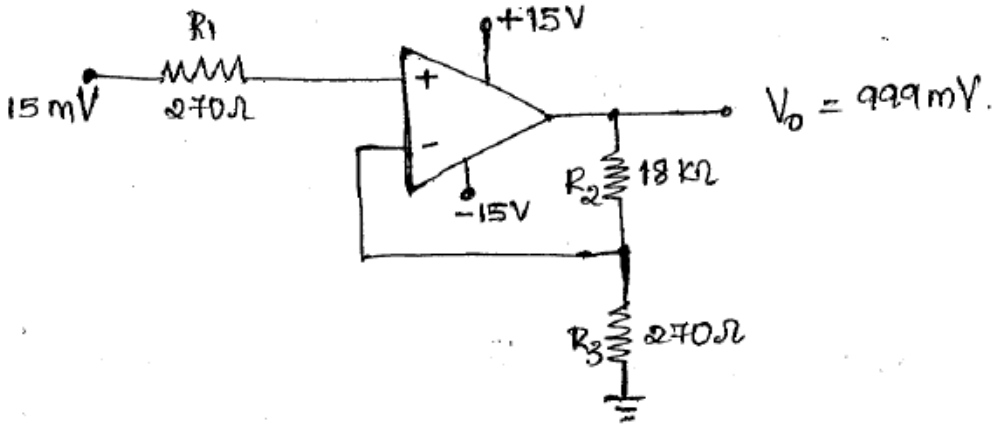
Use standard value resistor of R_2 i.e.

$\boxed{R_2 = 18\,K\Omega}$

* $R_1 = (R_2 \parallel R_3) = \frac{18\,K\Omega \times 270\Omega}{18K\Omega + 270\Omega}$

$\boxed{R_1 = 265.2\,\Omega}$

Use standard value of R_1 i.e. $\boxed{R_1 = 270\,\Omega}$



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2) Design a Non-INV amplifier with a voltage gain of 51 and signal voltage of 10 mV. use op-amp 741.

Given :- $A_V = 51$, $V_i = 10\,mV$

for 741 op-amp : $I_{B(max)} = 500\,nA$

Sol :- Let $I_2 = 100 \times I_{B(max)} = 100 \times 500\,nA$

$$\boxed{I_2 = 50\,\mu A}$$

* $R_3 = \frac{V_i}{I_2} = \frac{10\,mV}{50\,\mu A} = 200\,\Omega$ $\quad \boxed{R_3 = 200\,\Omega}$

Use standard value $\boxed{R_3 = 180\,\Omega}$

Now I_2 becomes :

$$I_2 = \frac{V_i}{R_3} = \frac{10\,mV}{180\,\Omega}$$

$$\boxed{I_2 = 55.5\,\mu A}$$

* WKT $V_o = A_V \times V_i = 51 \times 10\,mV$

$$\boxed{V_o = 510\,mV}$$

* $(R_2 + R_3) = \frac{V_o}{I_2}$

$$= \frac{510\,mV}{55.5\,\mu A}$$

$$= 9.18\,K\Omega$$

$$R_2 = 9.18\,K\Omega - R_3 = 9.18\,K\Omega - 180\,\Omega$$

$$\boxed{R_2 = 9\,K\Omega}$$

Use standard value of $\boxed{R_2 = 9.1\,K\Omega}$

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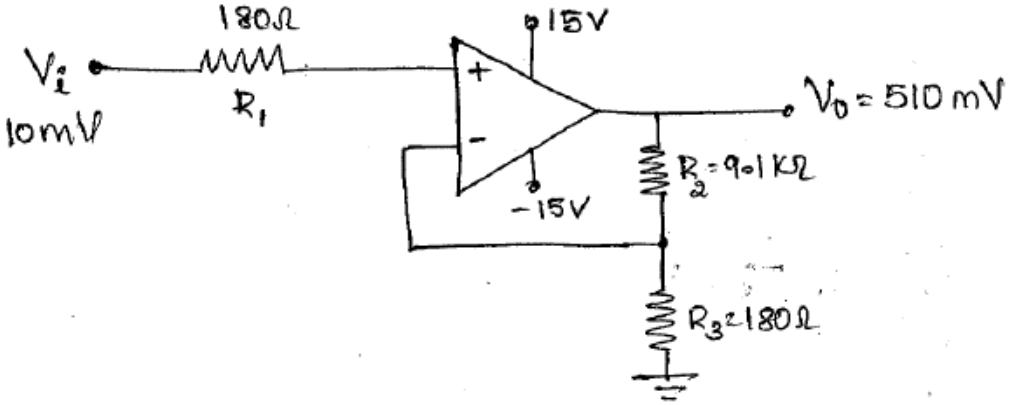
* $R_1 = (R_2 \parallel R_3) = \dfrac{9.1\,k\Omega \times 180\Omega}{9.1\,k\Omega + 180\Omega}$

$$R_1 = 176.5\,\Omega$$

Use standard value of $R_1 = 180\Omega$



3) Design a Non-INV amplifier to have a voltage gain of 70 using a 741 op-amp. The signal amplitude is to be 12mV.

Given :- $V_i = 12$ mV, $A_V = 70$

for 741 op-amp : $I_{B(max)} = 500$nA

Sol :- Let $I_2 = 100 \times I_{B(max)} = 100 \times 500$nA

$$I_2 = 50\,\mu A$$

* $R_3 = \dfrac{V_i}{I_2} = \dfrac{12\text{mV}}{50\,\mu A} = 240\Omega$ $\quad R_3 = 240\Omega$

* Use a standard value resistor i.e $R_3 = 220\Omega$

Now I_2 becomes.

$$I_2 = \frac{V_i}{R_3} = \frac{12\text{mV}}{220\Omega}$$

$$I_2 = 54.5\,\mu A$$

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* O/P voltage : $V_0 = A_V V_i = 70 \times 12mV = 840\,mV$

$$\boxed{V_0 = 840\,mV}$$

* $R_2 = \frac{V_0}{I_2} - R_3 = \left(\frac{840\,mV}{54.5\,\mu A} - 220\Omega\right)$

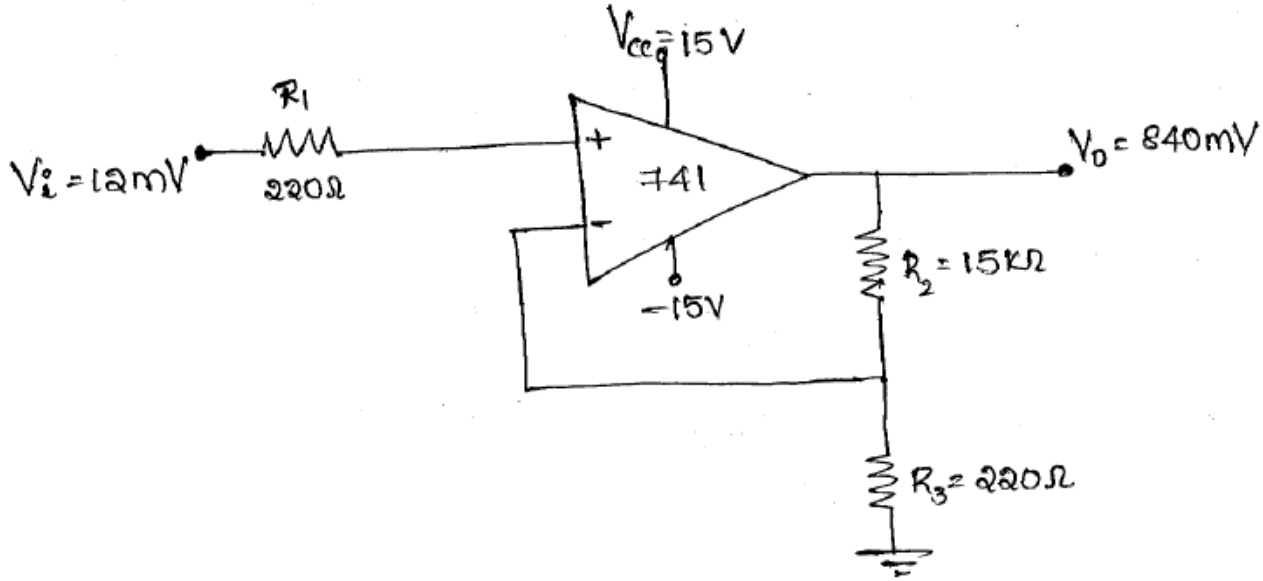
$$\boxed{R_2 = 15.18\,K\Omega}$$

Use standard value. $\boxed{R_2 = 15K\Omega}$

* $R_1 = (R_2 \,||\, R_3) = \frac{220\Omega \times 15K\Omega}{220\Omega + 15K\Omega}$

$$\boxed{R_1 = 216.8\Omega}$$

Use standard value : $\boxed{R_1 = 220\Omega}$



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4) Design a Non-INV amplifier to amplify a 100mV signal to a level of 4 volts. Using a 741 op-amp Assume $I_{B(max)} = 500nA$ & $R_s = 1K\Omega$

Given :- $V_i = 100\,mV$, $V_o = 4V$, $R_s = 1K\Omega$ & $I_{B(max)} = 500\,nA$

Sol: Let $I_2 = 100 \times I_{B(max)} = 100 \times 500nA$

$$\boxed{I_2 = 50\,\mu A}$$

* $R_3 = \frac{V_i}{I_2} = \frac{100mV}{50\mu A} = 2K\Omega$ $\boxed{R_3 = 2K\Omega}$

Use standard value : $\boxed{R_3 = 1.8\,K\Omega}$

* Now I_2 becomes: $I_2 = \frac{V_i}{R_3} = \frac{100mV}{1.8K\Omega}$

$$\boxed{I_2 = 55.6\,\mu A}$$

* $R_2 = \frac{V_o}{I_2} - R_3 = \frac{4V}{55.6\mu A} - 1.8K\Omega$

$\boxed{R_2 = 70.14K\Omega}$ Use standard value : $\boxed{R_2 = 68K\Omega}$

* $R_1 = (R_2 \,||\, R_3) = \frac{68K\Omega \times 1.8K\Omega}{68K\Omega + 1.8K\Omega}$

$$\boxed{R_1 = 1.75K\Omega}$$

* R_1 is Not very much greater than R_s

Thus

$$(R_1 + R_s) = (R_2 \,||\, R_3)$$

$$(R_1 + R_s) = (68K\Omega \,||\, 1.8K\Omega)$$

$$(R_1 + R_s) = 1.75K\Omega$$

$$R_1 = 1.75K\Omega - R_s.$$

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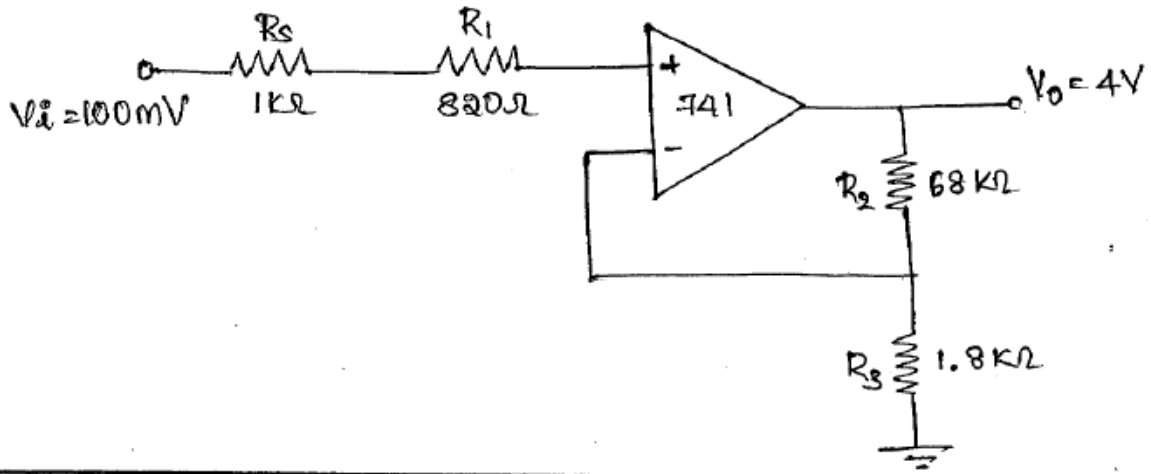
$R_1 = 1.75K\Omega - 1K\Omega$.

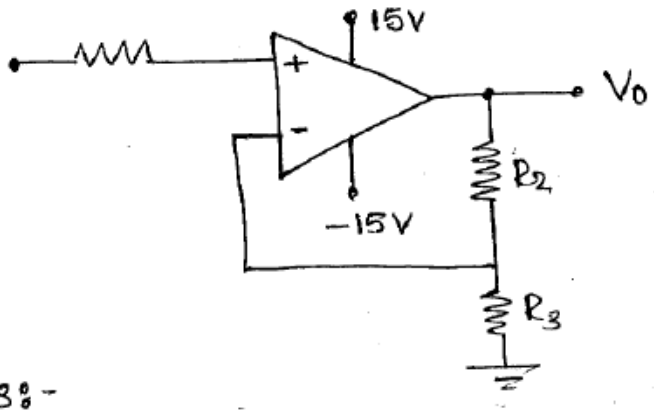
$\boxed{R_1 = 750\Omega}$

use standard value : $\boxed{R_1 = 820\Omega}$



FOR BIFET OP-AMP (LF-353)

Directly-coupled. Non-INV amplifier using LF353-BIFET



Design steps:-

1) First select higher resistance of the potential divider resistor : $\boxed{R_2 = 1M\Omega}$

2) WKT $A_V = \frac{R_2 + R_3}{R_3} = \frac{R_2}{R_3} + \frac{R_3}{R_3} = \frac{R_2}{R_3} + 1$.

$$\frac{R_2}{R_3} = A_V - 1$$

$$\boxed{R_3 = \frac{R_2}{A_V - 1}}$$

* $R_1 = (R_2 \| R_3)$.

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1) Design the non-INV. amplifier using a LF 353 BIFET. The gain is 66 and signal amplitude is to be 15mV.

Given :- $A_V = 66$, $V_i = 15\,mV$.

For LF-353 op-amp : $\boxed{I_{B(max)} = 200pA}$

Sol :-

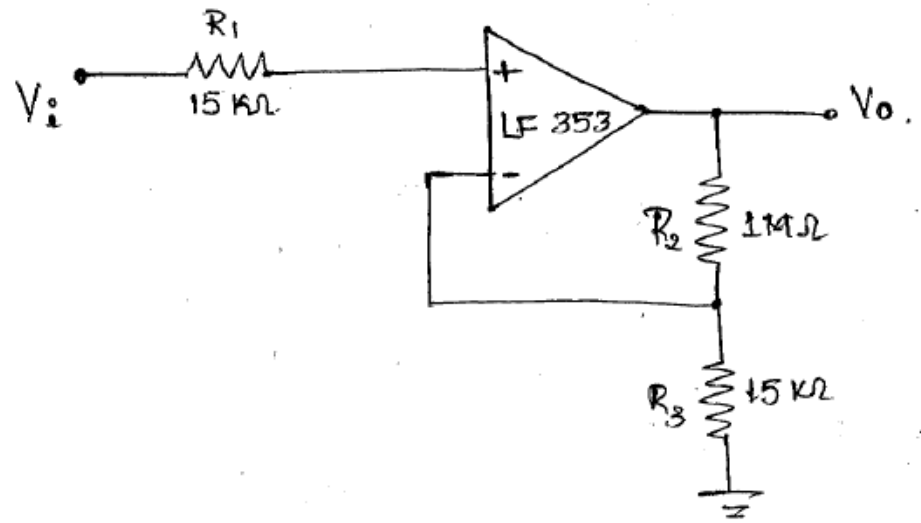
* Select $\boxed{R_2 = 1M\Omega}$

* $R_3 = \frac{R_2}{A_V - 1} = \frac{1M\Omega}{66-1}$

$\boxed{R_3 = 15.38k\Omega}$ use standard value : $\boxed{R_3 = 15k\Omega}$

* $R_1 = (R_2 \parallel R_3) = (1M\Omega \parallel 15k\Omega)$

$\boxed{R_1 = 15k\Omega}$



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a) Design the Non-INV amplifier using a LF-353 BIFET. the gain is 70. and signal amplitude is to be 12 mV.

Given :- $V_i = 10mV$, $A_V = 70$

for LF-353 op-amp : $I_{B(max)} = 200\,pA$

Sol :-

* select $R_2 = 1M\Omega$

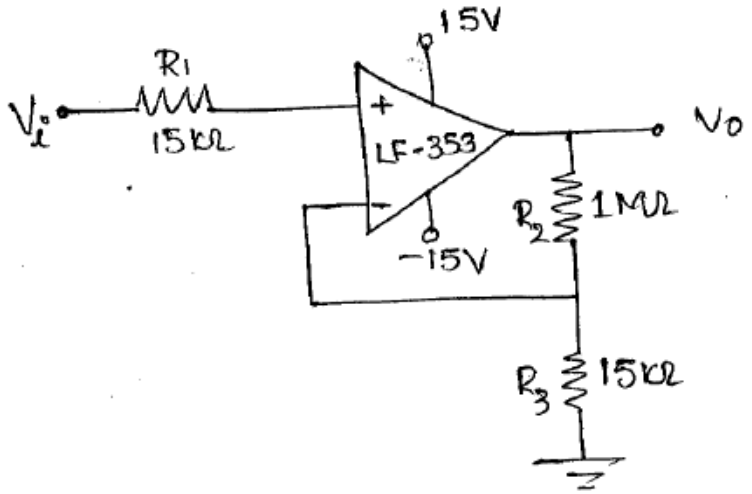
* $R_3 = \frac{R_2}{A_V - 1} = \frac{1M\Omega}{70-1} = 14.49K\Omega$ $\quad R_3 = 14.49K\Omega$

Use standard value : $R_3 = 15K\Omega$

* $R_1 = (R_2 \,||\, R_3) = (1M\Omega \,||\, 15K\Omega)$

$R_1 = 14.78K\Omega$

Use standard value : $R_1 = 15K\Omega$



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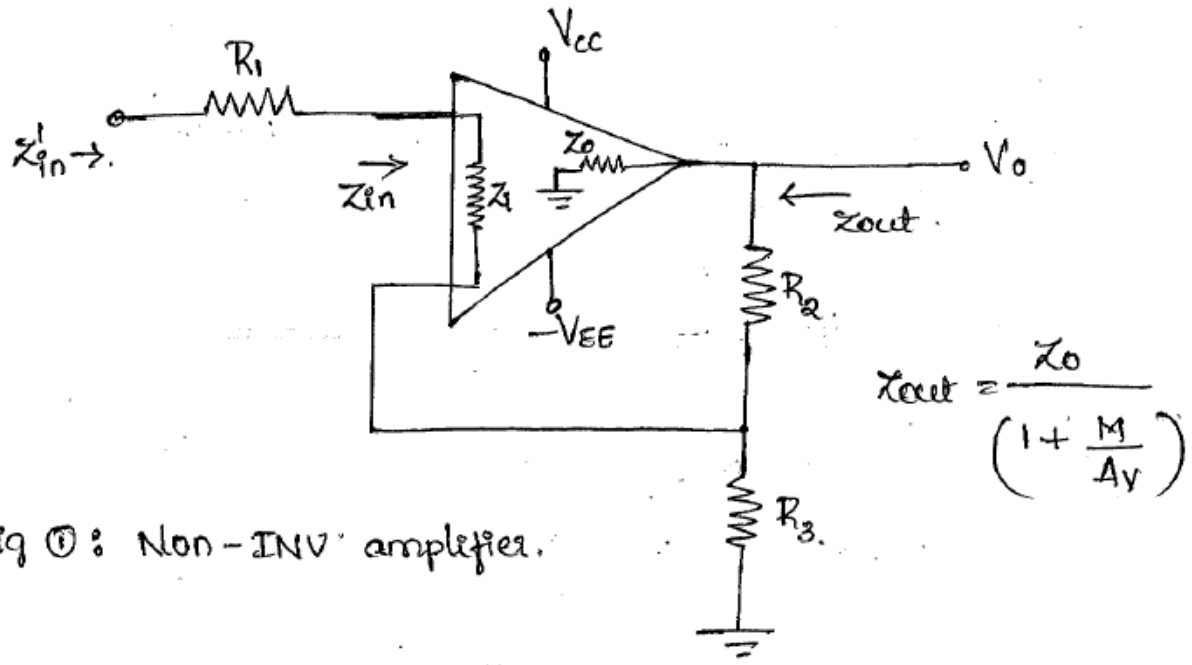
I/p & o/p Impedance of Non-INV amplifier :-



$$Z_{out} = \frac{Z_o}{\left(1 + \frac{M}{A_V}\right)}$$

fig ①: Non-INV amplifier.

* For NON-INV amplifier feedback factor β is given by

$$\beta = \frac{R_3}{R_2 + R_3} = \frac{1}{A_V} \qquad \left\{ \because A_V = \frac{R_2 + R_3}{R_3} \right.$$

$$\therefore \boxed{\beta = \frac{1}{A_V}}$$

* The I/p Impedance of an op-amp ciacuit given by

$$Z_{in} = (1 + M\beta)\, Z_i$$

∴ I/p Impedance of Non-INV amplifier is.

$$\boxed{Z_{in} = \left(1 + \frac{M}{\beta}\right) Z_i}$$

* The I/p Impedance when seen from the signal source is

$$\boxed{Z'_{in} = R_1 + Z_{in}}$$

* The o/p Impedance of an op-amp ciacuit is given by:

$$\boxed{Z_{out} = \frac{Z_o}{1 + M\beta}}$$

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* Since $\beta = \frac{1}{A_V}$

∴ o/p Impedance of Non-INV amplifier is

$$Z_{out} = \frac{Z_o}{\left(1 + \frac{M}{A_V}\right)} \qquad \left\{\because \beta = \frac{1}{A_V}\right\}$$

NOTE :-

Typical values for LF353 BIFET op-amp :

1) $M = 100000$
2) $Z_i = 10^{12}\,\Omega$
3) $Z_o = 75\,\Omega$
4) $I_{B(max)} = 200\,pA.$

1) Calculate the I/p & o/p impedance of an Non-INV amplifier having gain 66. Use the typical parameters of LF 353 op-amp. Assume $R_1 = 15\,K\Omega$

Given :- $A_v = 66$, $R_1 = 15\,K\Omega$.

Typical values for op-amp LF 353 :

$M = 100000$, $Z_i = 10^{12}\,\Omega$, $Z_o = 75\,\Omega$

Sol :- I/p Impedance :-

* $Z_{in} = \left(1 + \frac{M}{A_V}\right) Z_i = \left(1 + \frac{100000}{66}\right) \times 10^{12}\,\Omega$

$$Z_{in} = 1.5 \times 10^{15}\,\Omega$$

* $Z'_{in} = R_1 + Z_{in} = 15\,K\Omega + 1.5 \times 10^{15}\,\Omega$

$$Z'_{in} = 1.5 \times 10^{15}\,\Omega$$

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o/p Impedance:-

* $Z_{out} = \frac{Z_o}{\left(1 + \frac{M}{A_V}\right)} = \frac{75}{\left(1 + \frac{100000}{66}\right)}$

$\boxed{Z_{out} = 49.46\ m\Omega}$

---

2) A Non-INV amplifier is to be designed using a LF 353A BIFET op-amp having parameters given by $I_{B(max)} = 200pA$, $M = 10^5$, $Z_i = 10^{12}\Omega$, $Z_o = 75\Omega$. The source voltage used has $V_s = 50mV$ having a source resistance of $R_s = 2.2K\Omega$. The o/p voltage required is 3.3 volts. Find the values of all resistors R_1, R_2 & R_3. Also determine Z_{in}, Z_{out}, and Z'_{in} of the designed circuit.

Given:- $I_{B(max)} = 200pA$, $M = 10^5$, $Z_i = 10^{12}\Omega$, $Z_o = 75\Omega$,
$R_s = 2.2K\Omega$, $V_s = V_i = 50mV$, $V_o = 3.3V$.

Sol:-

* Select $\boxed{R_2 = 1M\Omega}$

* $R_3 = \frac{R_2}{A_V - 1}$

* $A_V = \frac{V_o}{V_i} = \frac{3.3V}{50mV} = 66$ $\therefore \boxed{A_V = 66}$

* $R_3 = \frac{1M\Omega}{66 - 1} = 15.385K\Omega$ $\therefore \boxed{R_3 = 15.385K\Omega}$

Use standard value $\boxed{R_3 = 15K\Omega}$

* $R_1 = (R_2 \parallel R_3) = (1M\Omega \parallel 15K\Omega) = 12.58K\Omega$.

Use standard value: $\boxed{R_1 = 12K\Omega}$

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* I/p Impedance :

$$Z_{in} = \left(1 + \frac{M}{A_V}\right) Z_i = \left(1 + \frac{10^5}{66}\right) 10^{12}\,\Omega$$

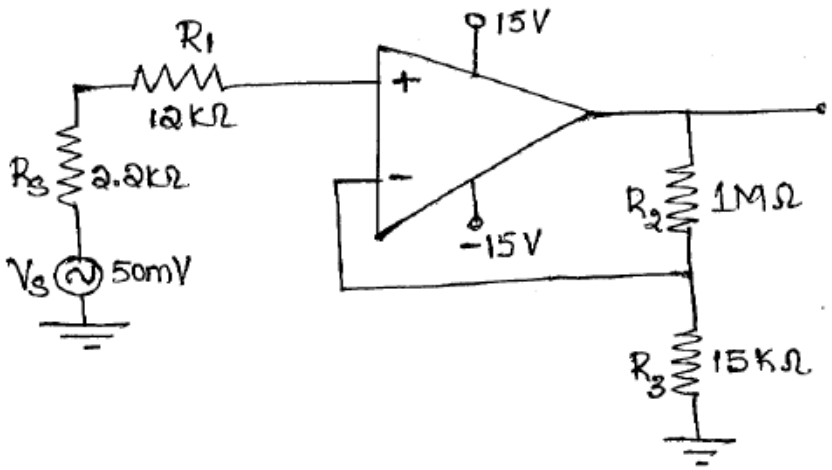
$$\boxed{Z_{in} = 1.52 \times 10^{12}\,\Omega}$$

* $Z'_{in} = R_1 + Z_{in} = 12\,K\Omega + 1.52 \times 10^{12}\,\Omega$

$$\boxed{Z'_{in} = 1.52 \times 10^{12}\,\Omega}$$

* o/p Impedance : $Z_{out} = \dfrac{Z_o}{\left(1 + \frac{M}{A_V}\right)} = \dfrac{75\,\Omega}{\left(1 + \frac{10^5}{66}\right)}$

$$\boxed{Z_{out} = 0.05\,\Omega}$$



* A Non-INV amplifier is to amplify a 100mV signal to a level of 3V. Using a 741 op-amp, design a suitable circuit.

June -10, 6m

Given:- $V_i = 100mV$, $V_o = 3V$.

for 741 op-amp : $I_{B(max)} = 500nA$.

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Sol:- * Let $I_2 = 100 \times I_{B(max)} = 100 \times 500mA = 50\mu A$

$\boxed{I_2 = 50\mu A}$

* $R_3 = \frac{V_i}{I_2} = \frac{100mV}{50\mu A} = \underline{\underline{2K\Omega}}$

Use standard resistor value, $\boxed{R_3 = 1.8K\Omega}$ ← (2m)

* Now I_2 level changes i.e.

$I_2 = \frac{V_i}{R_3} = \frac{100mV}{1.8K\Omega}$ $\therefore \boxed{I_2 = 55.6\mu A}$

* WKT $A_V = \frac{V_o}{V_i} = \frac{3V}{100mV} = 30$

* $R_2 + R_3 = \frac{V_o}{I_2}$.

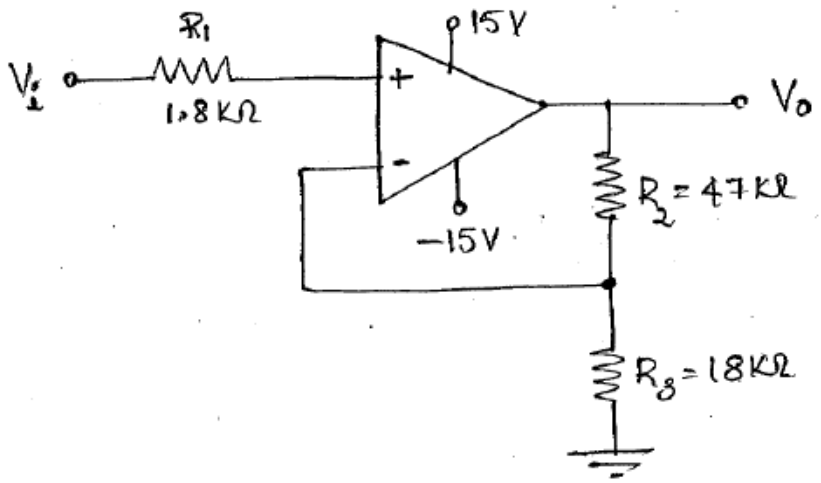
$R_2 = \left(\frac{V_o}{I_2} - R_3\right) = \left(\frac{3V}{55.6\mu A} - 1.8K\Omega\right)$

$R_2 = 52.15K\Omega$

Use standard value $\boxed{R_2 = 47K\Omega}$ ← (2m)

* $R_1 = (R_2 \parallel R_3) = (47K\Omega \parallel 1.8K\Omega) = 1.73K\Omega$

Use standard value resistor $\boxed{R_1 = 1.8K\Omega}$ ← (2m)



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Direct coupled INV-amplifier :- (for 741 op-amp)

1) With a neat ckt diagram, explain direct-coupled INV amplifier. June-09, 4m

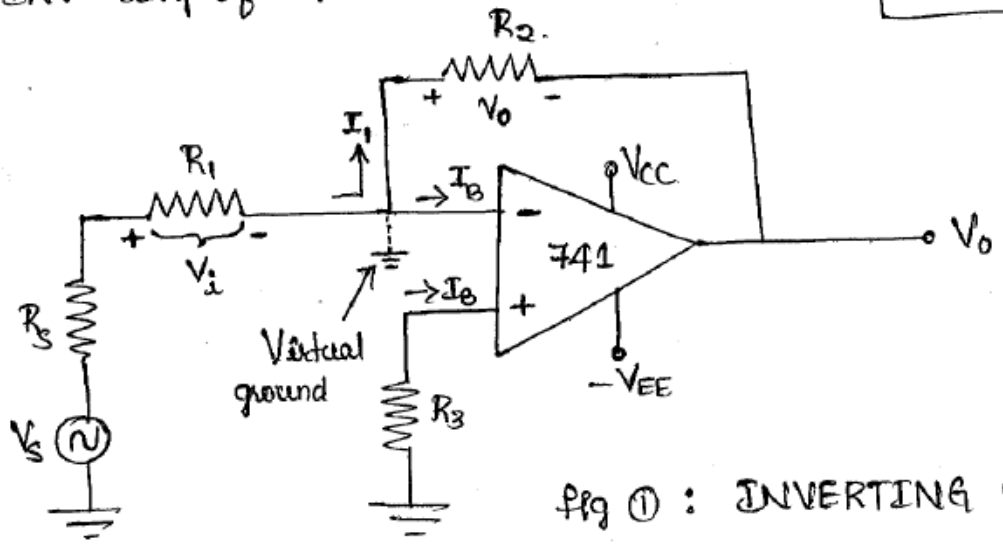

fig ① : INVERTING amplifier.

* The gain of the INV-amplifier is given by:

$$A_V = -\frac{R_2}{R_1}$$

Design steps:-

1) current I_1 is to be selected much higher than $I_{B(max)}$ of the op-amp.

$$I_1 = 100 \times I_{B(max)}$$

2) $$R_1 = \frac{V_i}{I_1}$$

3) $$R_2 = \frac{V_o}{I_1}$$

4) When looking out from each I/p terminal of op-amp:

$$R_3 = R_1 \parallel R_2$$

And if R_1 is not very much larger then the source resistance, then

$$R_3 \approx (R_1 + R_s) \parallel R_2$$

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Direct coupled INV-amplifier (for BIFET (LF 353) op-amp):-

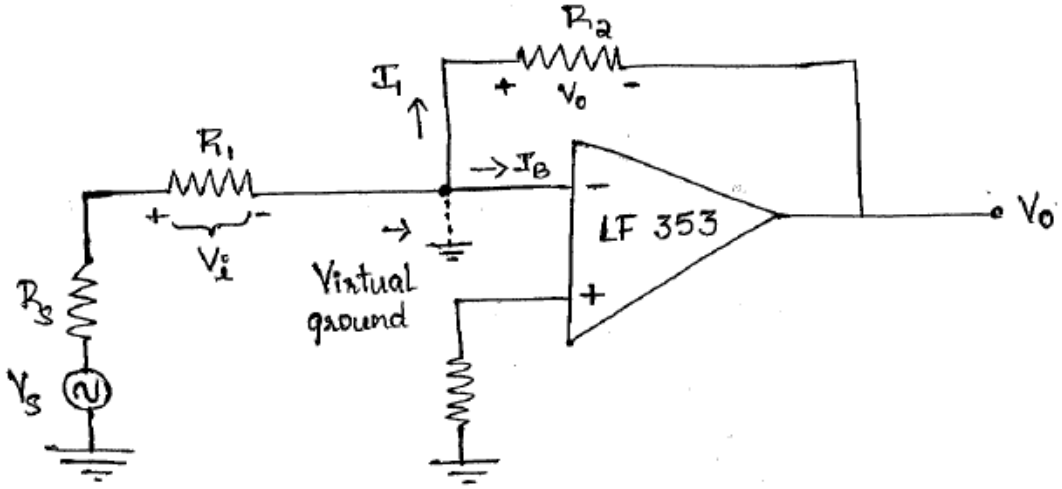

fig ①: INV-amplifier

Design steps:-

1) For BIFET op-amps select largest value resistor

$$R_2 = 1\,M\Omega$$

2) $$R_1 = \frac{R_2}{A_V}$$

3) $$R_3 \cong (R_1 \parallel R_2)$$

4) $$-A_V = \frac{R_2}{R_1}$$

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I/p & O/p Impedance of INV-amplifier :-

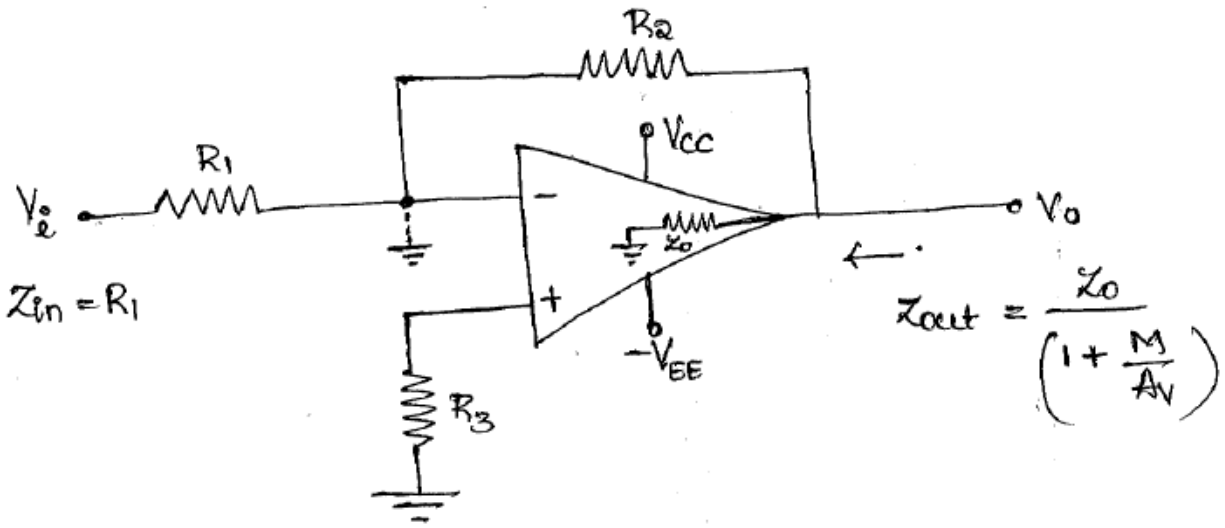

fig ① : Directly coupled INV-amplifier.

* The resistor 'R_1' is seen with its other end at ground level.

$$\therefore \boxed{Z_{in} = R_1}$$

* For INV-amplifier

$$\boxed{\beta = \frac{R_1}{R_1 + R_2}} \rightarrow ① \quad \& \quad \boxed{A_V = \frac{R_1 + R_2}{R_1}}$$

* the o/p Impedance of the INV amplifier is given by:

$$\boxed{Z_{out} = \frac{Z_o}{1 + M\beta}} \rightarrow ②$$

Substituting eq ① in eq ②, we get

$$Z_{out} = \frac{Z_o}{1 + M\left(\frac{R_1}{R_1 + R_2}\right)}$$

$$\boxed{Z_{out} = \frac{Z_o}{1 + \frac{M}{A_V}}}$$

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Problems.

1) Design an inverting amplifier using a 741 op-amp. The voltage gain is to be 50 and the o/p voltage amplitude is to be 2.5V.

Given: $A_V = 50$, $V_o = 2.5V$

For 741 op-amp: $I_{B(max)} = 500nA$

Sol:-

* Let $I_1 = 100 \times I_{B(max)} = 100 \times 500nA$

$I_1 = 50\mu A$

* WKT $A_V = \frac{V_o}{V_i}$

$V_i = \frac{V_o}{A_V} = \frac{2.5V}{50} = 50mV.$ $\quad V_i = 50mV$

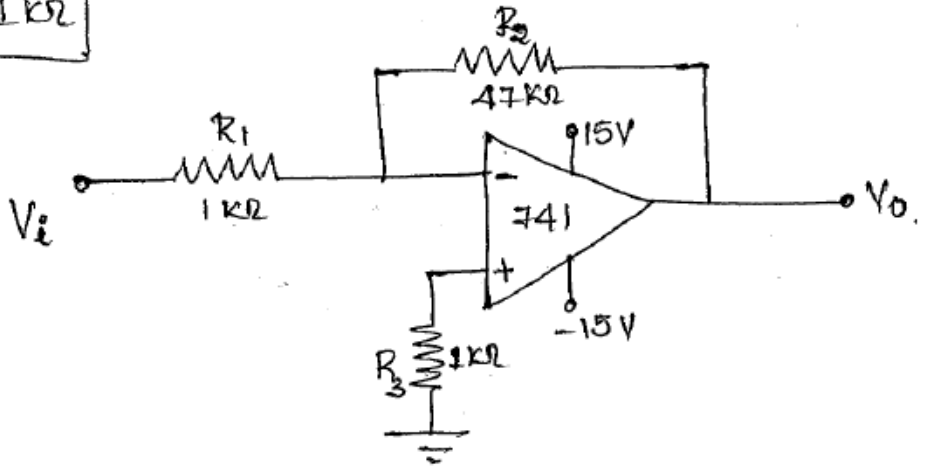
* $R_1 = \frac{V_i}{I_1} = \frac{50mV}{50\mu A} = 1K\Omega$ $\quad \therefore R_1 = 1K\Omega$

* $R_2 = \frac{V_o}{I_1} = \frac{2.5V}{50\mu A} = 50K\Omega$

Use standard value: $R_2 = 47K\Omega$

* $R_3 = R_1 \parallel R_2 = 1K\Omega \parallel 47K\Omega$

$R_3 \approx 1K\Omega$



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2) Design an inverting amplifier using op-amp 741 with a voltage gain of 60 and the o/p voltage required is 3V.

Given :- $A_V = 60$, $V_o = 3V$

for 741 op-amp : $I_{B(max)} = 500nA$

Sol :-

* Let $I_1 = 100 \times I_{B(max)} = 100 \times 500nA = 50\,\mu A$

$\boxed{I_1 = 50\mu A}$

* WKT $A_V = \frac{V_o}{V_i}$

$$V_i = \frac{V_o}{A_V} = \frac{3V}{60}$$

$\boxed{V_i = 50mV}$

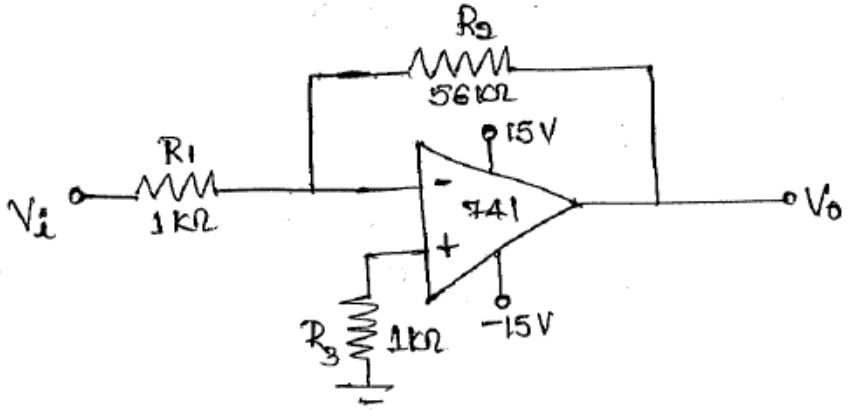
* $R_1 = \frac{V_i}{I_1} = \frac{50mV}{50\,\mu A}$ $\therefore \boxed{R_1 = 1K\Omega}$

* $R_2 = \frac{V_o}{I_1} = \frac{3V}{50\,\mu A}$ $\boxed{R_2 = 60K\Omega}$

Use standard value $\boxed{R_2 = 56K\Omega}$

* $R_3 = (R_1 \,||\, R_2) = \frac{1K\Omega \times 56K\Omega}{1K\Omega + 56K\Omega}$ $\boxed{R_3 = 983.6\Omega}$

Use standard value $\boxed{R_3 = 1K\Omega}$



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LF 353 BIFET

1) Design the INVERTING amplifier using a LF 353 BIFET op-amp. The voltage gain is to be 50 and the o/p voltage amplitude is to be 2.5V.

Given :- $A_V = 50$, $V_o = 2.5V$

Sol :-

* For BIFET op-amps select largest value resistor

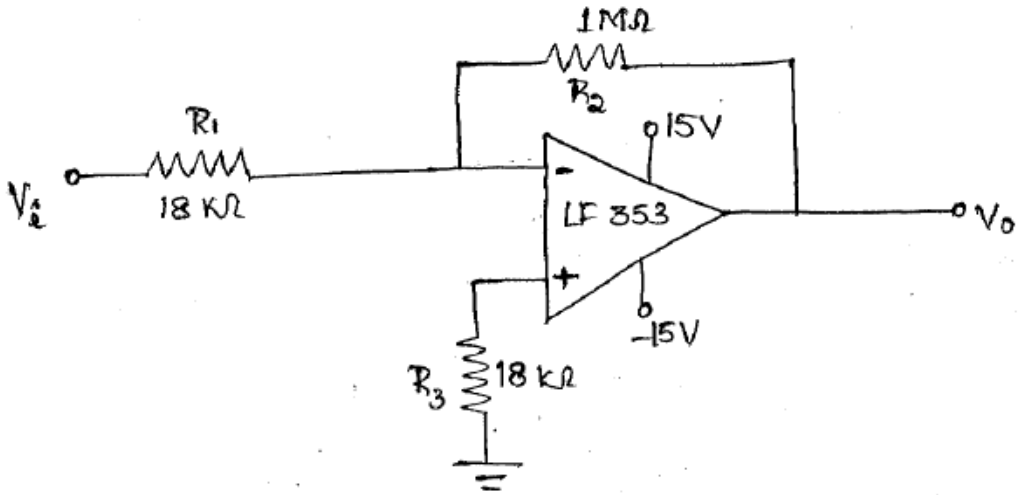
$R_2 = 1M\Omega$

* $R_1 = \frac{R_2}{A_V} = \frac{1M\Omega}{50}$ $\quad R_1 = 20K\Omega$

Use standard value $R_1 = 18K\Omega$

* $R_3 = (R_1 \parallel R_2) = \frac{18K\Omega \times 1M\Omega}{18K\Omega + 1M\Omega}$ $\quad R_3 = 17.68K\Omega$

Use standard value $R_3 = 18K\Omega$



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2) Design the inverting amplifier using a LF 353 BIFET op-amp. The voltage gain is to be 40 and the o/p voltage amplitude is to be 3V.

Given :- $A_V = 40$, $V_o = 3V$

Sol:-

* Select largest value resistor

$$R_2 = 1M\Omega$$

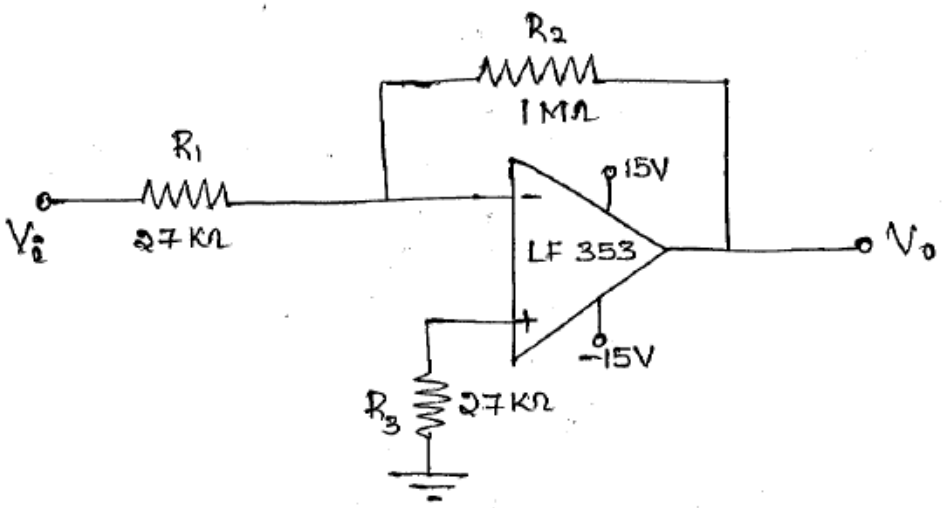
* $$R_1 = \frac{R_2}{A_V} = \frac{1M\Omega}{40}$$

$R_1 = 25K\Omega$ Use standard value $R_1 = 27K\Omega$

* $$R_3 = (R_1 \parallel R_2) = \frac{27K\Omega \times 1M\Omega}{27K\Omega + 1M\Omega}$$

$R_3 = 26.29K\Omega$

Use standard value $R_3 = 27K\Omega$



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3) An inverting amplifier using BIFET LF 353A op-amp is to be employed to amplify a 50mV signal to a level of 3.5 volts. Design the required circuit and determine its I/p and o/p Impedances. Assume $R_s = 1.2K\Omega$, $M = 10^5$ and $Z_o = 75\Omega$ for BIFET op-amp.

Given: $V_i = 50mV$, $V_o = 3.5V$, $R_s = 1.2K\Omega$, $M = 10^5$, $Z_o = 75\Omega$.

Sol :-

* Select largest value resistor : $R_2 = 1M\Omega$

* WKT $A_V = \frac{V_o}{V_i} = \frac{3.5V}{50mV}$ $\boxed{A_V = 70}$

* $R_1 = \frac{R_2}{A_V} = \frac{1M\Omega}{70}$ $\boxed{R_1 = 14.28K\Omega}$

Use standard value $R_1 = 15K\Omega$.

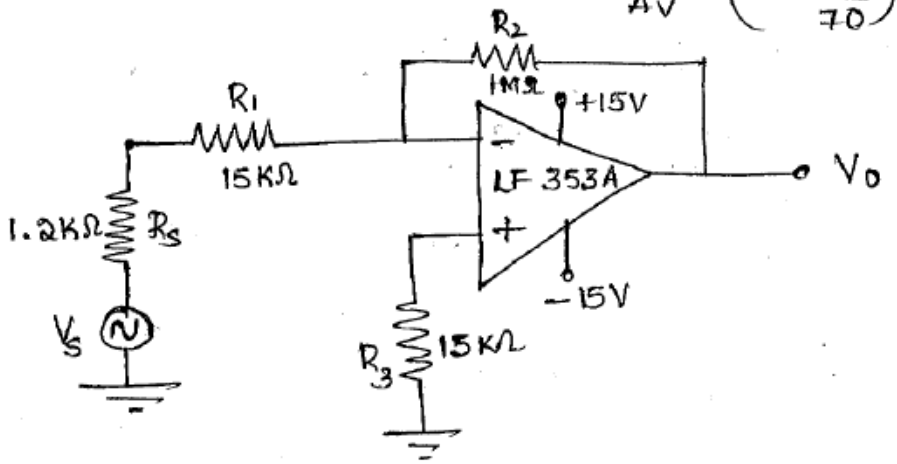
* $R_3 = (R_1 \parallel R_2) = \frac{15K\Omega \times 1M\Omega}{15K\Omega + 1M\Omega}$ $\boxed{R_3 = 14.77K\Omega}$

Use standard value $\boxed{R_3 = 15K\Omega}$

* The I/p Impedance, $Z_{in} = R_1$

$\boxed{Z_{in} = 15K\Omega}$

* O/p Impedance: $Z_{out} = \frac{Z_o}{1 + \frac{M}{A_V}} = \frac{75\Omega}{\left(1 + \frac{10^5}{70}\right)} = \underline{0.052\Omega}$



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SUMMING AMPLIFIERS

INVERTING SUMMING CIRCUIT :-

* Sketch the circuit of a two-I/p inverting summing amplifiers. Explain the operation of the ckt & derive the equation for the o/p voltage.

June -10, 8M

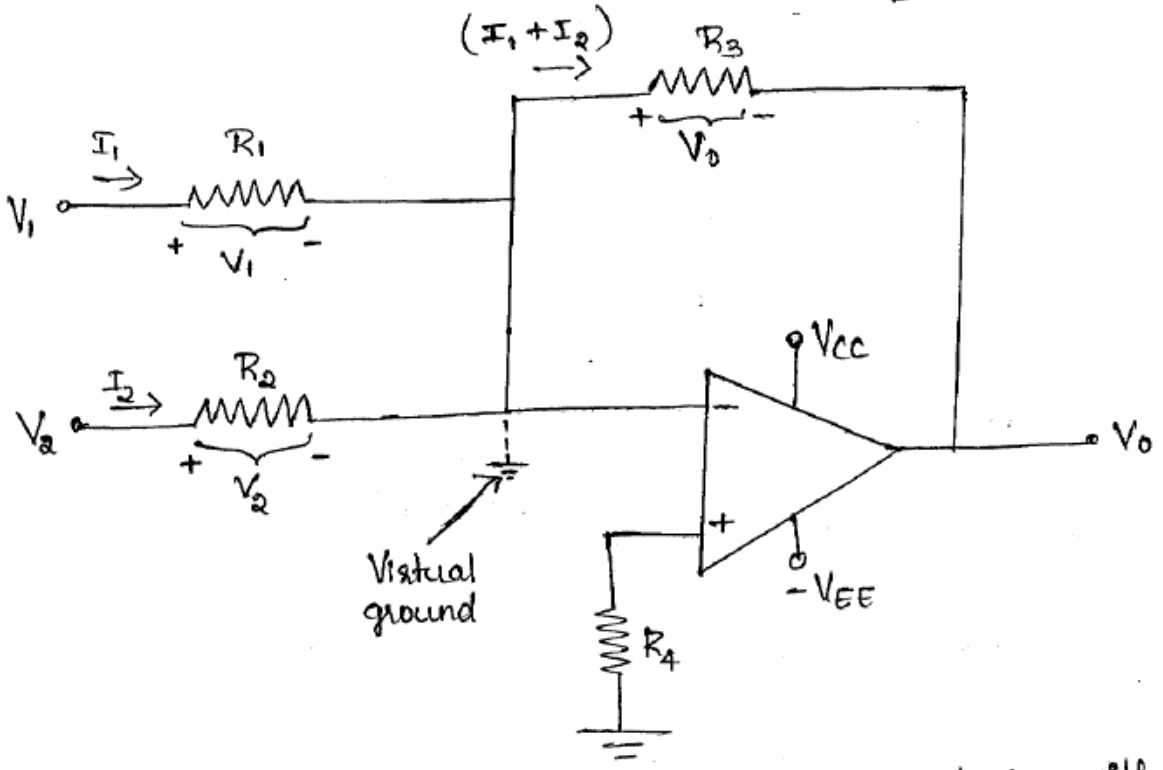

fig ① : op-amp INV summing amplifier with 2 I/ps.

fig ① shows a circuit that amplifies the sum of two or more I/p's. Since the inverting terminal behaves as a Virtual ground, the currents through the resistors R_1 & R_2 are respectively given by :

$$I_1 = \frac{V_1}{R_1} \quad \text{and} \quad I_2 = \frac{V_2}{R_2}$$

* These two currents flow through R_3.

Applying KVL from R_3 to o/p.

$$-(I_1 + I_2) R_3 - V_0 = 0$$

$$V_0 = -(I_1 + I_2) R_3 \rightarrow ①$$

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Substituting I_1 & I_2 in eq ①, we get

$$V_0 = -\left[\frac{V_1}{R_1} + \frac{V_2}{R_2}\right] R_3$$

$$V_0 = -R_3\left[\frac{V_1}{R_1} + \frac{V_2}{R_2}\right]$$

With $R_1 = R_2$

$$V_0 = -R_3\left[\frac{V_1}{R_1} + \frac{V_2}{R_1}\right]$$

$$\boxed{V_0 = -\frac{R_3}{R_1}\left[V_1 + V_2\right]} \rightarrow ②$$

But $\boxed{A_V = -\frac{R_3}{R_1}}$

$$\therefore \boxed{V_0 = A_V\left[V_1 + V_2\right]} \rightarrow ③$$

* If $R_1 = R_2 = R_3$, then $A_V = -1$, then eq ③ becomes

$$V_0 = -1\left[V_1 + V_2\right]$$

$$\boxed{V_0 = -\left[V_1 + V_2\right]}$$

* $\boxed{R_4 = R_1 \parallel R_2 \parallel R_3}$

* Suppose there are three I/p's to a summing circuit as shown in fig ②

* the o/p voltage is given by:

$$V_0 = -\left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right] R_4$$

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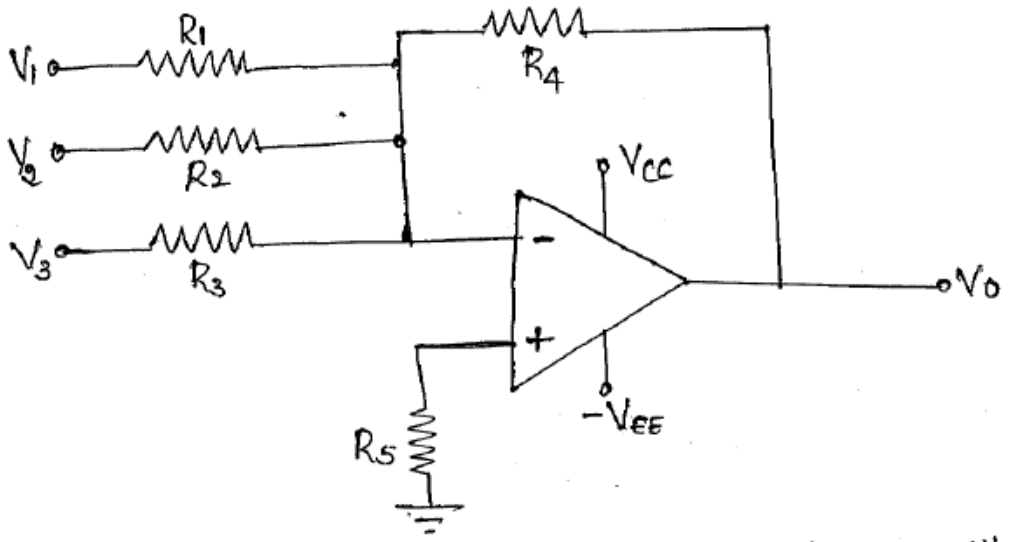

Fig ③ : INV Summing amplifier with 3 I/p's.

Suppose that $\boxed{R_1 = R_2 = R_3}$ then,

$$V_0 = -R_4 \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_1} \right]$$

$$\boxed{V_0 = -\frac{R_4}{R_1} [V_1 + V_2 + V_3]}$$

If $R_4 = \frac{R_1}{3}$, then

$$V_0 = -\frac{R_1}{3R_1} [V_1 + V_2 + V_3]$$

$$\boxed{V_0 = -\frac{1}{3} [V_1 + V_2 + V_3]} \longrightarrow ④$$

Equation ④ shows that the o/p voltage is the average value of the three I/p's. Thus, the summing amplifier can be designed to be an averaging circuit.

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INV - summing amplifier Design procedure :-

1) $I_{1(min)} = 100 \times I_{B(max)}$

2) $R_1 = \dfrac{V_{S(min)}}{I_{1(min)}}$

3) $R_1 = R_2$

4) for $A_V = -1$, $R_1 = R_3$

5) $R_4 = R_1 \parallel R_2 \parallel R_3$

Problems

1) Design a INV summing amplifier to give the direct sum of two I/p's which each range from 0.1V to 1V. Use a 741 op-amp.

(OR)

1) Two signals which each range from 0.1V to 1V are to be summed. Using a 741 op-amp design a suitable inverting summing circuit

June - 08, 6M

Given : $V_{S(min)} = 0.1V$, $V_{S(max)} = 1V$

For 741 op-amp : $I_{B(max)} = 500nA$.

Sol : * $I_{1(min)} = 100 \times I_{B(max)} = 100 \times 500nA$

$I_{1(min)} = 50\mu A$ ← 1M

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* $R_1 = \frac{V_{S(min)}}{I_{1(min)}} = \frac{0.1V}{50\mu A}$

$R_1 = 2K\Omega$ Use standard value $R_1 = 1.8K\Omega$ ← (2m)

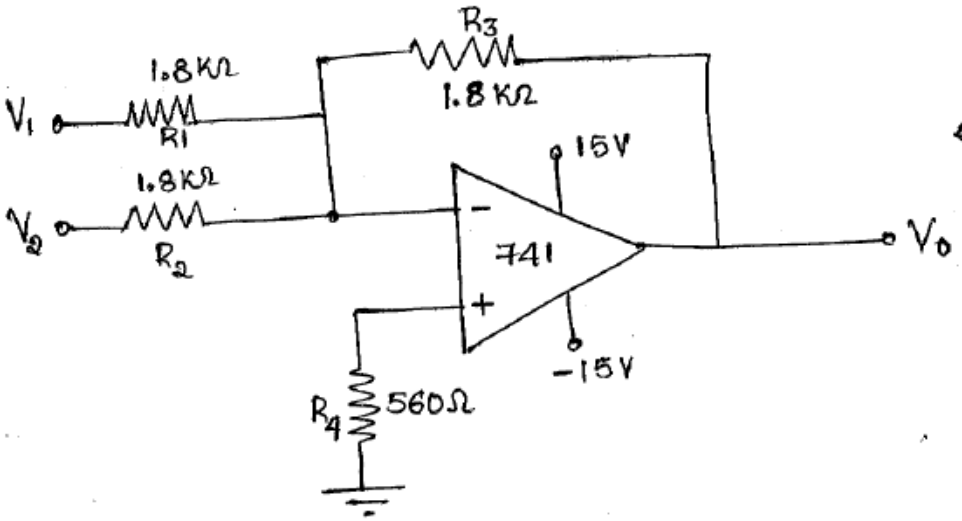
* $R_1 = R_2 = 1.8K\Omega$

* for $A_V = 1$, $R_1 = R_3 = 1.8K\Omega$ ← (1m)

* $R_4 = R_1 \| R_2 \| R_3 = 1.8K\Omega \| 1.8K\Omega \| 1.8K\Omega$

$R_4 = 600\Omega$

Use standard value $R_4 \approx 560\Omega$ ← (1m)



← (1m)

2) Three signals each ranging from 0.2V to 0.5V are to be summed. Using a 741 op-amp, design a suitable inverting summer circuit. Choose $I_{B(max)} = 500nA$ for 741 op-amp.

Given :- $V_{S(min)} = 0.2V$, $V_{S(max)} = 0.5V$, $I_{B(max)} = 500nA$

Sol :- * $I_{1(min)} = 100 \times I_{B(max)}$

$= 100 \times 500nA$

$\therefore$ $I_{1(min)} = 50\mu A$

ARUNKUMAR G M.Tech, *Lecturer in E&CE Dept. S.T.J.I.T., Ranebennur.*

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* $R_1 = \frac{V_{S(min)}}{I_{1(min)}} = \frac{0.2V}{50\mu A}$ $\boxed{R_1 = 4K\Omega}$

Use standard value $\boxed{R_1 = 3.9K\Omega}$

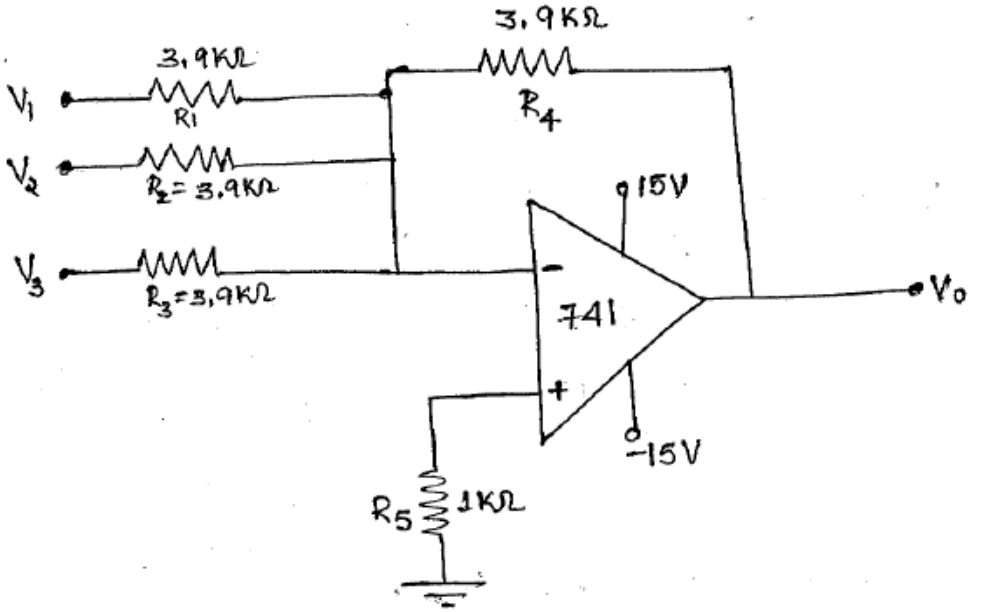
* $R_1 = R_2 = R_3 = 3.9K\Omega$

* For $A_V = 1$, $R_4 = R_1 = \underline{3.9K\Omega}$

* $R_5 = R_1 \| R_2 \| R_3 \| R_4 = 3.9K\Omega \| 3.9K\Omega \| 3.9K\Omega \| 3.9K\Omega$

$\boxed{R_5 = 975\Omega}$

Use standard value $\boxed{R_5 = 1K\Omega}$



3) Design a INV summing amplifier to give the sum of the two I/p's which each range from 0.5V to 1V. Use as 741 op-amp and gain of the circuit as 2.

Given :- $V_{S(min)} = 0.5V$, $V_{S(max)} = 1V$, $A_V = 2$

For op-amp 741 : $I_{B(max)} = 500nA$

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Sol : $I_{1(min)} = 100 \times I_{B(max)} = 100 \times 500nA$

$\boxed{I_{1(min)} = 50\mu A}$

* $R_1 = \frac{V_{S(min)}}{I_{1(min)}} = \frac{0.5V}{50\mu A}$ $\boxed{R_1 = 10K\Omega}$

* $\boxed{R_1 = R_2 = 10K\Omega}$

* Given $A_V = 2$.

WKT $|A_V| = \left|\frac{R_3}{R_1}\right|$

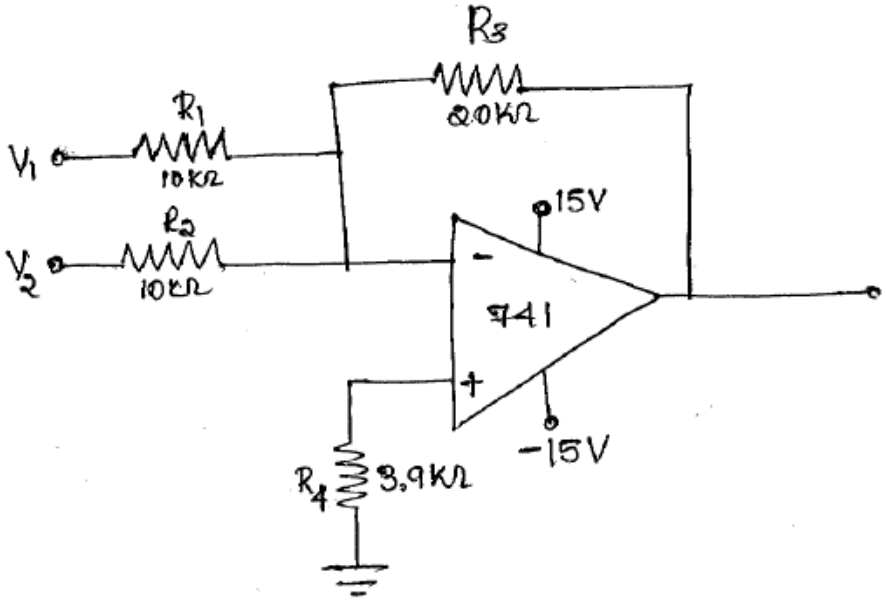
$2 = \frac{R_3}{R_1}$

$R_3 = 2R_1 = 2 \times 10K\Omega$ $\boxed{R_3 = 20K\Omega}$

Use standard value : $\boxed{R_3 = 22K\Omega}$

* $R_4 = R_1 \parallel R_2 \parallel R_3 = 10K\Omega \parallel 10K\Omega \parallel 22K\Omega$

$\boxed{R_4 = 4.07K\Omega}$ Use standard value $\boxed{R_4 = 3.9K\Omega}$



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NON - INVERTING SUMMING CKT :-

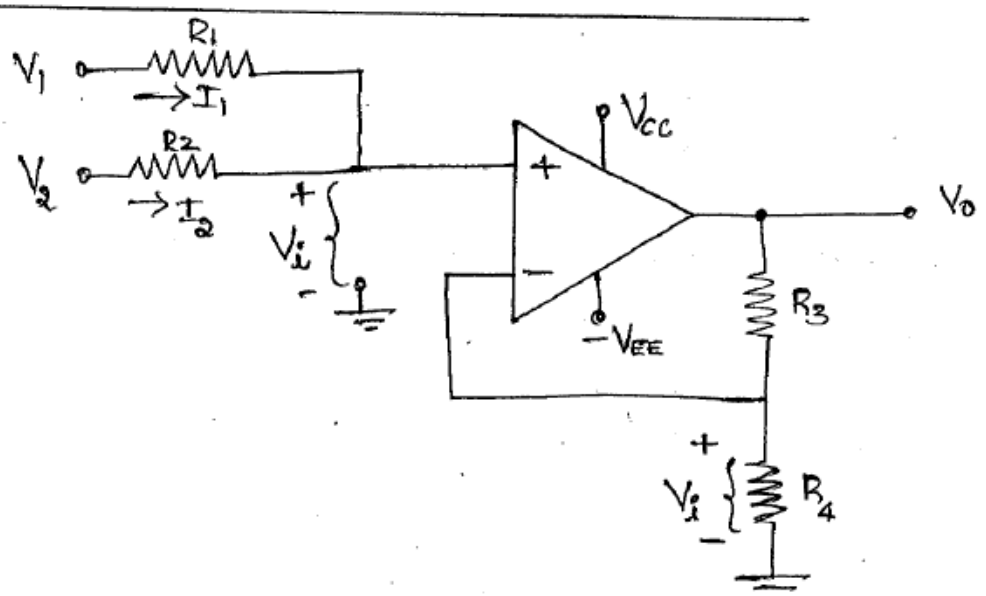


fig ① : Non - INV Summing amplifier with two I/p's.

fig ① shows a Non - INV summing amplifier. The o/p will be a direct sum of +ve I/p signals.

The equation for the o/p voltage can be derived by using superposition theorem.

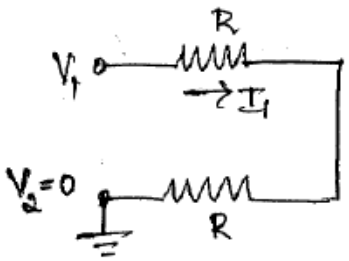
* Let $V_2 = 0$ & $R_1 = R_2 = R$

$$V_{i1} = I_1 R$$

$$= \frac{V_1 R}{R+R}$$

$$= \frac{V_1 R}{2R}$$

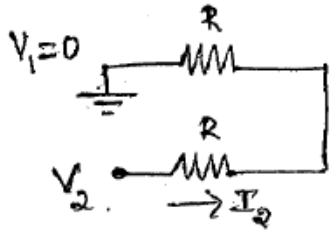
$$\boxed{V_{i1} = \frac{V_1}{2}} \rightarrow ①$$



$\because I_1 = \frac{V_1}{R+R}$

* Let $V_1 = 0$ & $R_1 = R_2 = R$

$$V_{i2} = I_2 R$$



$\because I_2 = \frac{V_2}{R+R}$

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$$V_{i2} = \frac{V_2 R}{R+R} = \frac{V_2 R}{2R}$$

$$\boxed{V_{i2} = \frac{V_2}{2}} \rightarrow (2)$$

* The I/p voltage V_i is given by:

$$\boxed{V_i = V_{i1} + V_{i2}} \rightarrow (3)$$

Substituting eq (1) & (2) in eq (3), we get

$$V_i = \frac{V_1}{2} + \frac{V_2}{2}$$

$$\therefore \boxed{V_i = \frac{V_1 + V_2}{2}}$$

* For Non-INV amplifier, the voltage gain is given by

$$\boxed{A_V = \frac{R_3 + R_4}{R_4}} \rightarrow (4)$$

* WKT $A_V = \frac{V_0}{V_i}$

$$\boxed{V_0 = A_V V_i} \rightarrow (5)$$

Substituting eq (3) & (4), we get

$$V_0 = \frac{R_3 + R_4}{R_4}\left(\frac{V_1 + V_2}{2}\right)$$

If $R_3 = R_4 = R$.

$$V_0 = \frac{R+R}{R}\left(\frac{V_1 + V_2}{2}\right)$$

$$V_0 = \frac{2R}{R}\left(\frac{V_1 + V_2}{2}\right) \qquad \left(\because V_0 = \frac{2R}{2R}(V_1 + V_2)\right.$$

$$\boxed{V_0 = (V_1 + V_2)}$$

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* Fig ② shows the Non-INV Summing amplifier with three I/p's.

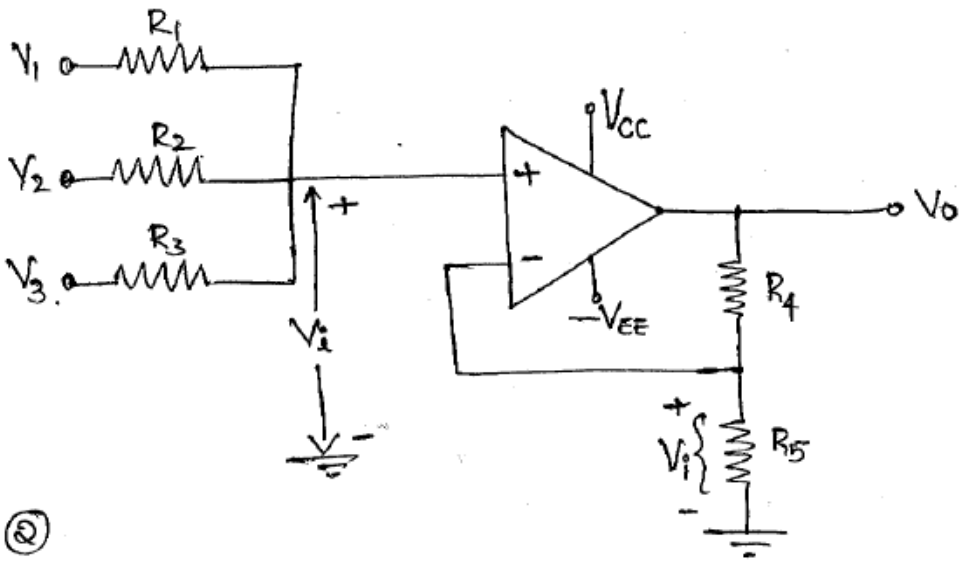

fig ②

* For the three-I/p Non-INV Summing ckt in fig ②, the voltage at the op-amp Non-INV I/p when

$R_1 = R_2 = R_3 = R$

$$V_i = \frac{V_1 + V_2 + V_3}{3}$$

WKT $V_o = A_V V_i$

$$V_o = A_V \left(\frac{V_1 + V_2 + V_3}{3} \right)$$

With $\boxed{A_V = 3}$

$$V_o = \cancel{3} \left(\frac{V_1 + V_2 + V_3}{\cancel{3}} \right)$$

$$\boxed{V_o = (V_1 + V_2 + V_3)}$$

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Difference Amplifier :-

A difference amplifier or differential amplifier, amplifies the difference between the two I/p signals. An IC op-amp is a difference amplifier having INV & Non-INV I/p's. Since the open-loop gain of the op-amp is very large, it has to be used with negative feedback.

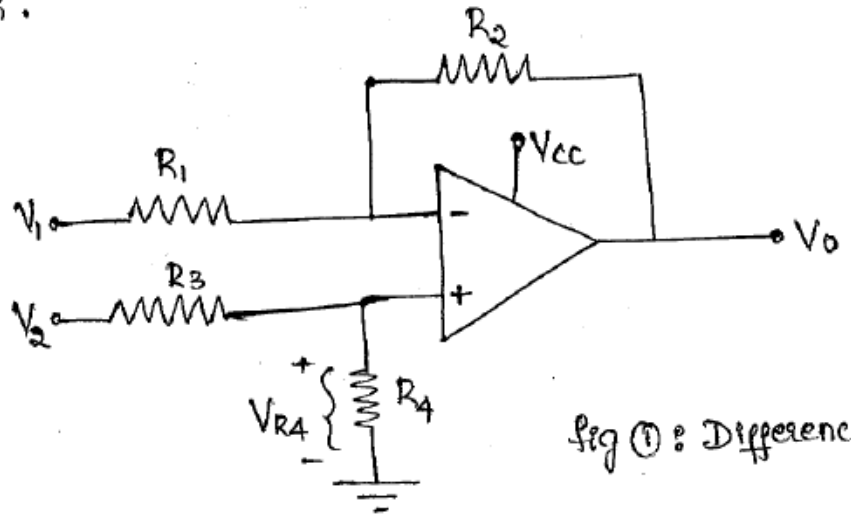

fig ①: Difference amplifier ckt.

Operation :-

Let us use superposition principle to find out the expression for the o/p :

Case i :

V_1 acting, $V_2 = 0V$ (grounded). Let the o/p is V_{01}.

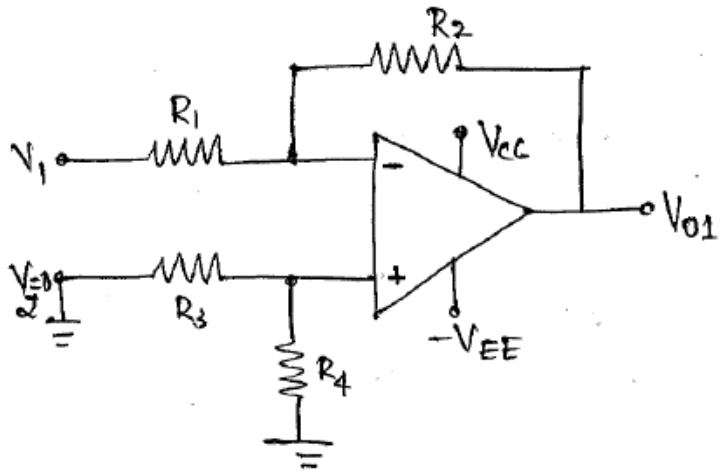

fig ②: V_1 acting & $V_2 = 0V$

* Now fig ② acts as an INV amplifier

$$\therefore \boxed{V_{01} = -\frac{R_2}{R_1} V_1} \rightarrow (1)$$

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Case II : V_2 acting, $V_1 = 0V$ (grounded). Let the o/p is V_{02}.

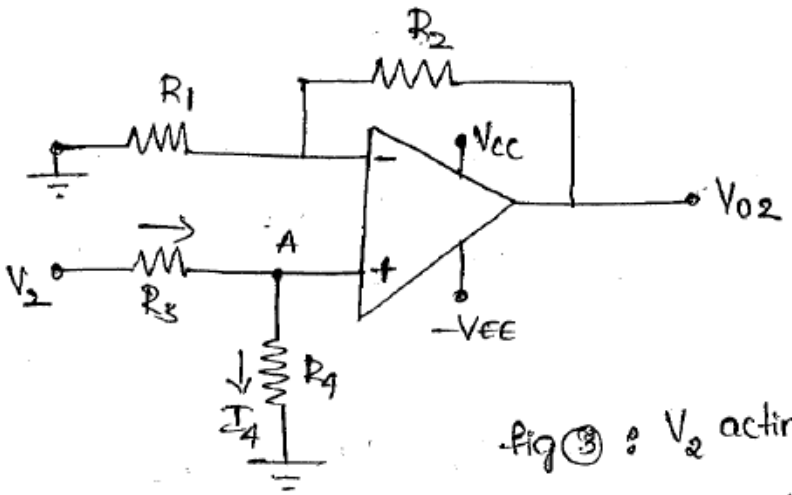

fig ③ : V_2 acting & $V_1 = 0$

* Now fig ③ : acts as Non-INV amplifier & hence :

* the o/p voltage is given by :

$$V_{02} = A_V V_A$$

{ ∵ WKT $A_V = \frac{V_0}{V_A}$ }

WKT the gain of the Non-INV amplifier is given by

$$A_V = \left(1 + \frac{R_2}{R_1}\right)$$

$$V_{02} = \left(1 + \frac{R_2}{R_1}\right) V_A \quad \rightarrow ②$$

from fig ③ the voltage at Node A is given by :

$$V_A = IR_4$$

where, $I = \frac{V_2}{R_3 + R_4}$

$$\therefore V_A = \frac{V_2 R_4}{R_3 + R_4} \quad \rightarrow ③$$

Substituting eq ③ in eq ②, we get

$$V_{02} = \left(1 + \frac{R_2}{R_1}\right)\left(\frac{V_2 R_4}{R_3 + R_4}\right) \quad \rightarrow ④$$

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With both signals present,

$$\boxed{V_o = V_{o1} + V_{o2}} \rightarrow (5)$$

Substituting eq (1) & (4) in eq (5), we get.

$$V_o = -\frac{R_2}{R_1} V_1 + \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_4}{R_3 + R_4}\right) V_2$$

select the resistance as $R_3 = R_1$ and $R_4 = R_2$

$$V_o = -\frac{R_2}{R_1} V_1 + \left(\frac{R_1 + R_2}{R_1}\right)\left(\frac{R_2}{R_1 + R_2}\right) V_2$$

$$V_o = -\frac{R_2}{R_1} V_1 + \frac{R_2}{R_1} V_2$$

$$V_o = \frac{R_2}{R_1}\left[V_2 - V_1\right]$$

($\because V_o = A_V V_i$ where $A_V = \frac{R_2}{R_1}$, $V_i = V_2 - V_1$)

When $R_1 = R_2$

$$\boxed{V_o = (V_2 - V_1)}$$

Now the o/p is the direct difference of the two I/p voltage.

Continued →

P.T.O

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I/p Resistance :-

i) Differential I/p resistance :-

The differential I/p resistance is the resistance offered to a signal source which is connected directly across the I/p terminals.

i.e $\boxed{R_{i\,(diff)} = R_1 + R_3 + R_4}$

ii) Common mode I/p resistance :-

The common mode I/p resistance is the resistance offered to a signal source which is connected b/w both I/p terminals and ground.

i.e. $\boxed{R_{i\,(cm)} = R_1 \,||\, (R_3 + R_4)}$

Difference Amplifier → FORMULAE

1) For LF 353 op-amp : Select $R_2 = 1\,M\Omega$

2) $A_V = \frac{R_2}{R_1}$

3) $R_3 = R_1$

4) $R_4 = R_2$

5) $R_{i(dif)} = R_1 + (R_3 + R_4)$

6) $R_{i(cm)} = R_1 \,||\, (R_3 + R_4)$

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PROBLEMS

1) The difference of two I/p signals to be amplified by a factor of 37. Each I/p has an amplitude of approximately 50mV. Using an LF 353 op-amp, design a suitable circuit and calculate the differential and common mode I/p resistance.

Given: $A_V = 37$, $V_i = 50mV$

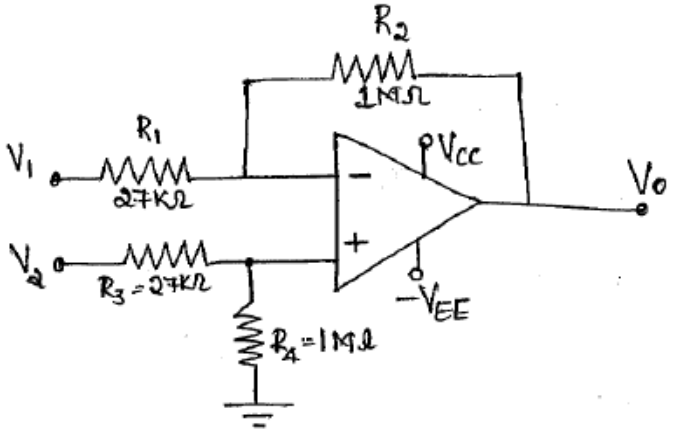
Sol:- For LF 353 op-amp:

* Select largest value resistor: $R_2 = 1M\Omega$

* WKT $A_V = \frac{R_2}{R_1}$

$$R_1 = \frac{R_2}{A_V} = \frac{1M\Omega}{37}$$

$$R_1 = 27K\Omega$$



* $R_3 = R_1 = 27K\Omega$

* $R_4 = R_2 = 1M\Omega$

* $R_{i(dif)} = R_1 + R_3 + R_4$

$= 27K\Omega + 27K\Omega + 1M\Omega$

$$R_{i(diff)} = 1.054M\Omega$$

Use standard value resistor: $R_{i(diff)} = 1M\Omega$

* $R_{i(cm)} = R_1 \| (R_3 + R_4) = 27K\Omega \| (27K\Omega + 1M\Omega)$

$$R_{i(cm)} = 26.3K\Omega$$

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2) The difference of two I/p signals is to be amplified by a factor 40. Each I/p has an amplitude of approximately 40mV. Using a LF 353 - OP-amp, design a circuit and calculate the differential and common mode I/p resistance.

Given :- $A_V = 40$, $V_i = 40\,mV$

Sol :- For LF353 op-amp :

* Select largest value resistor, $\boxed{R_2 = 1M\Omega}$

* WKT $A_V = \frac{R_2}{R_1}$

$$R_1 = \frac{R_2}{A_V} = \frac{1M\Omega}{40}$$

$$\boxed{R_1 = 25K\Omega}$$

* $R_3 = R_1 = 25K\Omega$ Use standard value resistor

$$\boxed{R_3 = R_1 = 27K\Omega}$$

* $R_4 = R_2 = 1M\Omega$

* $R_i(dif) = R_1 + R_3 + R_4 = 27K\Omega + 27K\Omega + 1M\Omega$

$$\boxed{R_i(dif) = 1.054\,M\Omega}$$

Use standard value resistor : $\boxed{R_i(dif) = 1M\Omega}$

* $R_i(cm) = R_1 \,||\, (R_3 + R_4)$

$= 27K\Omega \,||\, (27K\Omega + 1M\Omega)$

$$\boxed{R_i(cm) = 26.308K\Omega}$$

Use standard value resistor :

$$\boxed{R_i(cm) = 27K\Omega}$$

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3) Design a difference amplifier with gain 50. Also calculate the values of differential and common mode I/p resistance.

Given :- $A_V = 50$

Sol :-

* Select largest value resistor

$$\boxed{R_2 = 1M\Omega}$$

* $A_V = \frac{R_2}{R_1}$

$$R_1 = \frac{R_2}{A_V} = \frac{1M\Omega}{50}$$

$$\boxed{R_1 = 20K\Omega}$$

* $R_3 = R_1 = 20K\Omega$

* $R_4 = R_2 = 1M\Omega$

* $R_{i(dif)} = R_1 + R_3 + R_4 = \underline{1.04M\Omega}$

* $R_{i(cm)} = R_1 \| (R_3 + R_4)$

$= 20K\Omega \| (20K\Omega + 1M\Omega)$

$$\boxed{R_{i(cm)} = 19.615\ K\Omega}$$

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Common Mode Voltages :-

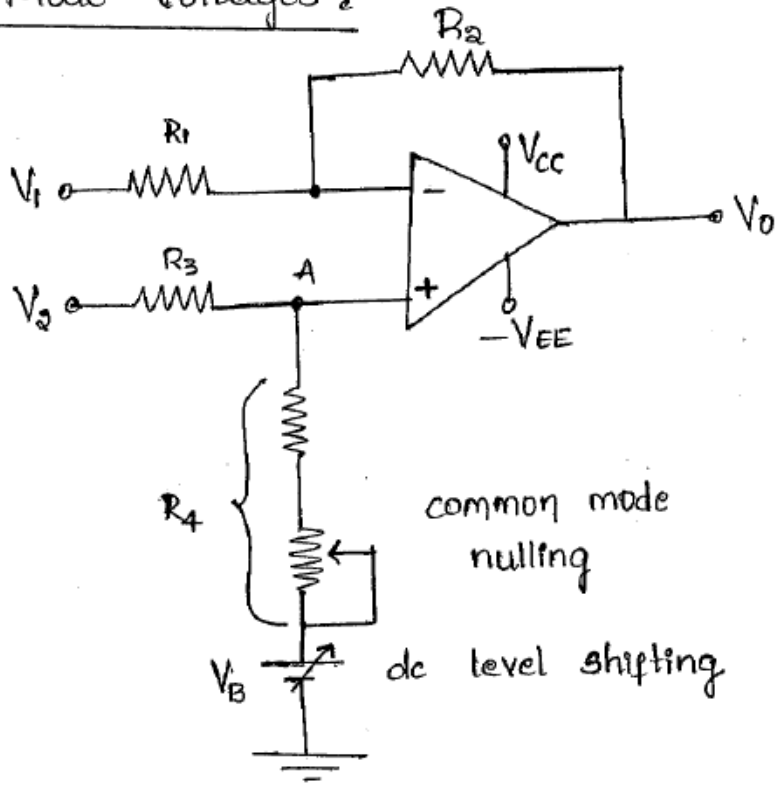

fig ①: Difference amplifier to nullify common-mode o/p & o/p level shifting.

* Let 'V_c' is the common voltage gets applied to both the I/p terminals. Hence input 1 becomes $(V_1 + V_c)$ While I/p 2 becomes $(V_2 + V_c)$.

* The amplified o/p is the difference b/w the two I/p's i.e. $V_i = (V_2 + V_c) - (V_1 + V_c)$

$$= V_2 + V_c - V_1 - V_c$$

$$\therefore \boxed{V_i = V_2 - V_1}$$

* The 'V_c' gets cancelled and has no effect on the o/p if $\left(\frac{R_4}{R_3} = \frac{R_2}{R_1}\right)$ are equal.

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* If these ratios are unequal then 'V_c' at one I/p gets amplified more than that at the other I/p.
Hence V_c will not get cancelled & will be present at o/p.

* Practically it is impossible to match these ratios perfectly and some common mode voltage is found to be present.

* To minimise common mode o/p, the resistor R_4 is selected as the combination of fixed resistor and a smaller variable resistor.

* By adjusting the (potentiometer) variable part of 'R_4', the ratio R_4/R_3 is made almost equal to R_2/R_1 in order to null the common mode o/p voltage to zero.

o/p Level shifting :-

In fig ①: R_4 is connected to a bias voltage V_B. To understand the effect of V_B, assume that both I/p voltages ($V_1 = V_2 = 0$) are zero.

* The voltage at the op-amp Non-INV I/p terminal will be

$$V_A = IR_3$$

where $$I = \frac{V_B}{R_3 + R_4}$$

$$\boxed{V_A = V_B \cdot \frac{R_3}{R_3 + R_4}} \rightarrow ①$$

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* The ckt behaves as Non-INV amplifier hence,

$$V_0 = V_A\left(1 + \frac{R_2}{R_1}\right) \longrightarrow (2)$$

Substituting eq (1) in eq (2), we get

$$V_0 = V_B\left(\frac{R_3}{R_3 + R_4}\right) \cdot \left(1 + \frac{R_2}{R_1}\right)$$

But $\boxed{\frac{R_2}{R_1} = \frac{R_4}{R_3}}$

$$V_0 = V_B\left(\frac{R_3}{R_3 + R_4}\right)\left(1 + \frac{R_4}{R_3}\right)$$

$$V_0 = V_B\left(\frac{\cancel{R_3}}{\cancel{R_3 + R_4}}\right)\left(\frac{\cancel{R_3 + R_4}}{\cancel{R_3}}\right)$$

$$\boxed{V_0 = V_B}$$

i.e. there is a shift in the o/p level by an amount equal to the voltage V_B.

∴ By adjusting the voltage 'V_B', it is possible to get any desired shift in the o/p level.

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* Define the following terms as applied to an op-amp and mention their typical values for IC 741:

i) CMRR
ii) PSRR
iii) Slew rate
iv) o/p Impedance

Jan-10, 8M

* Define the following parameters:

i) I/p offset voltage
ii) CMRR
iii) Slewrate

Mention their typical values for op-amp 741

June-10, 6M

---

* CMRR :-

CMRR is defined as the ratio of the open-loop gain 'M' to the Common mode gain 'A_{cm}'.

$$CMRR = \frac{M}{A_{CM}}$$

The CMRR is usually expressed in decibels

$$(CMRR)_{dB} = 20 \log_{10} \left(\frac{M}{A_{CM}}\right)_{dB}$$

For 741 op-amp, typical value of CMRR is 90 dB

---

* PSRR :-

The PSRR is the ability of the op-amp to reject variations in the power Supply voltages

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$$PSRR = \frac{V_{o(ripple)}}{V_{s(ripple)}}$$

If a variation of 1V in V_{cc} & V_{EE} causes the o/p to change by 1V, then PSRR is 1 per volt.

For 741 op-amp, the PSRR is typically 30 μV/V.

---

* Slew rate :-

The Slew rate 'S' of an op-amp is the maximum rate at which the o/p voltage can change.

When the Slew rate is too Slow for the I/p, then o/p will distort.

$$\text{Slew rate} = \frac{\Delta V}{\Delta t} \quad \text{&} \quad S = \left.\frac{dV_o}{dt}\right|_{max}$$

Typical value for 741 op-amp is 0.5V/μsec.

---

* o/p Impedance :-

o/p Impedance is the impedance as Seen at the o/p terminal w.r.to ground.

$$Z_{out} = \frac{Z_o}{1+M\beta}$$

Typical value for 741 op-amp is 75Ω.

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I/p Impedance :-

I/p Impedance of an ideal op-amp is infinite, but it will have a finite value depending on the type of application

$$\boxed{Z_{in} = Z_i(1+M\beta)}$$

Typical value for 741 op-amp is 0.3MΩ

o/p Offset voltage :-

For the o/p voltage to be exactly equal to the I/p, the transistors Q_1 & Q_2 must be perfectly matched.

The o/p voltage can be calculated as

$$V_o = V_i - V_{BE1} + V_{BE2}$$

With $V_{BE1} = V_{BE2}$ and $V_i = 0$

o/p $\boxed{V_o = V_i = 0}$

* Now Suppose that the transistors are not perfectly matched and that $V_{BE1} = 0.7V$ & $V_{BE2} = 0.6V$ with $V_i = 0V$,

then o/p $V_o = V_i - V_{BE1} + V_{BE2}$

$= 0 - 0.7V + 0.6V$

$\boxed{V_o = -0.1V}$

This unwanted o/p is known as an o/p offset voltage.

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I/p offset voltage :-

Now Suppose that the transistors are not perfectly matched & that $V_{BE1} = 0.7V$ while $V_{BE2} = 0.6V$.

With the I/p $V_i = 0$,

$$V_o = V_i - V_{BE1} + V_{BE2}$$

$$= 0 - 0.7V + 0.6V$$

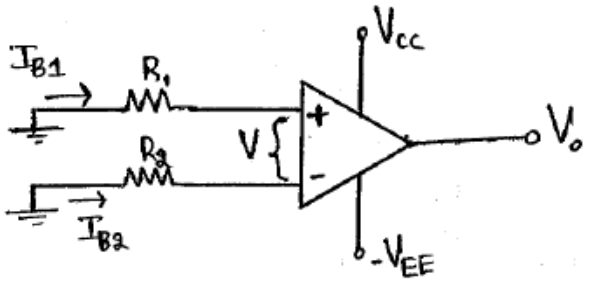
$$\boxed{V_o = -0.1V}$$

* To Set V_o to ground level, the I/p would have to be raised to +0.1V. This is termed as input offset voltage V_{ios}.

For 741 op-amp, typical value of $V_{ios} = 1mV$ &

maximum value of $V_{ios} = 5mV$

* I/p offset current :-



$$\boxed{V = I_{B1}R_1 - I_{B2}R_2}$$

* The algebraic difference between the currents flowing into the two I/p terminals of the op-amp is called I/p offset current & denoted as I_{ios}

$$\boxed{I_{ios} = |I_{b1} - I_{b2}|}$$

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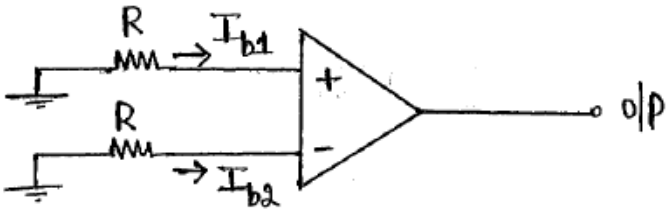
For 741 op-amp, maximum value of I_{ios} is 200nA

I/p bias Current :-



* The average value of the two currents flowing into the op-amp input terminals is called I/p bias current.

$$I_b = \frac{I_{b1} + I_{b2}}{2}$$

For 741 op-amp, maximum value of I_b is 500nA

Offset Nulling :-

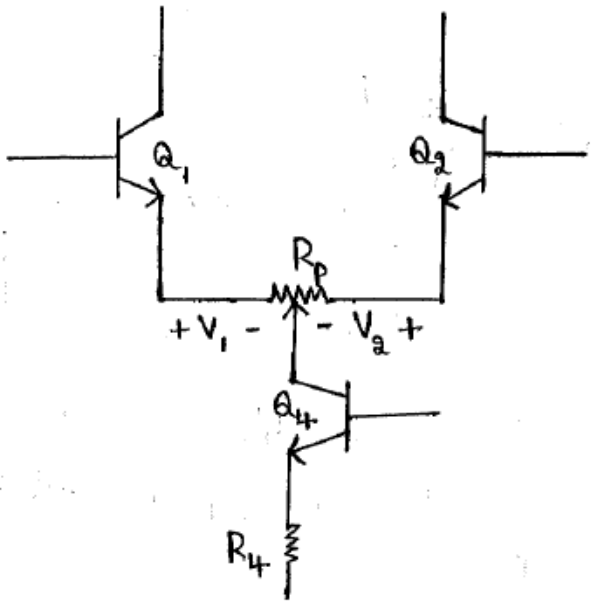


fig : use of potentiometer for offset Nulling

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To minimize the effect of offset voltages and currents, a variable resistance is introduced between the emitters of Q_1 & Q_2 as shown in figure.

The variable resistance R_p is the low resistance potentiometer which alters the voltage drop from base of each transistor to the common moving point of potentiometer. Hence the I/p base current also get altered.

As I/p offset current produces an offset voltage, by adjusting R_p, both I/p offset current as well as input offset voltage can be nulled.

I/p voltage range :-

The maximum positive going & negative going I/p voltage that can be applied to the op-amp so that it functions properly is called its I/p voltage range.

For 741 op-amp, I/p voltage range of ±13 V for ±15 V supply.

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* Define CMRR of an op-amp. If a Non-INV amplifier is designed for a gain of 100 using an op-amp with 95dB CMRR. calculate the Common mode o/p (V_{ocm}) for a Common mode I/p (V_{icm}) of 2V

Dec-10, 6M

* CMRR is defined as the ratio of the open-loop gain 'M' to the Common mode gain 'A_{cm}'.

$$CMRR = \frac{M}{A_{CM}}$$

The CMRR is usually expressed in decibels ← 2M

$$(CMRR)_{dB} = 20 \log_{10} \left(\frac{M}{A_{CM}}\right)_{dB}$$

Given: $A_V = 100$, $(CMRR)_{dB} = 95dB$, $V_{icm} = 2V$

WKT $(CMRR)_{dB} = 20 \log_{10} (CMRR)$

$$CMRR = \text{antilog}\left(\frac{95}{20}\right)$$

$$CMRR = 56,234$$ ← 2M

WKT $V_{ocm} = \frac{V_{icm}}{CMRR} \cdot A_V = \frac{2V}{56234} \times 100$

$$V_{ocm} = 3.55mV$$ ← 2M

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* Design a Non-INV amplifier to provide a gain 50 for an I/p of 100mv. Compute its I/p & o/p impedances. Given $R_i = 2M\Omega$, $R_o = 75\Omega$, $I_{B\,max} = 500nA$, & $M = 2,00,000$ for the op-amp (741).

Dec-10, 8M

Given :- $A_V = 50$, $V_i = 100mV$, $I_{B\,max} = 500nA$

Sol :-

Let $I_2 = 100 \times I_{B(max)}$

$= 100 \times 500nA$

$\boxed{I_2 = 50\mu A}$

* $R_3 = \frac{V_i}{I_2} = \frac{100mV}{50\mu A} = 2K\Omega$ ← (1M)

* WKT $A_V = \frac{V_o}{V_i}$

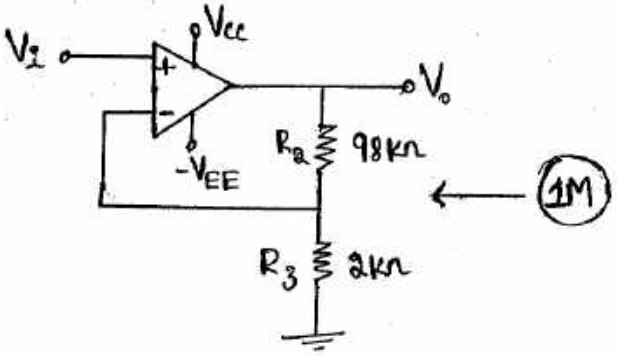
$V_o = A_V V_i = 50 \times 100mV$

$\boxed{V_o = 5V}$

* $R_2 + R_3 = \frac{V_o}{I_2}$

$R_2 = \frac{V_o}{I_2} - R_3 = \frac{5V}{50\mu A} - 2K\Omega$

$\boxed{R_2 = 98K\Omega}$ ← (1M)



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* Feedback Factor for Non-INV amplifier is $\beta = \frac{1}{A_V} = \frac{R_3}{R_2+R_3} = \frac{98k\Omega}{2k\Omega+98k\Omega}$

$$\boxed{\beta = 0.02}$$

* $Z_{in} = Z_i(1+M\beta) = 2M\Omega(1+200000\times 0.02)$

$$\boxed{Z_{in} = 8\times 10^9\,\Omega} \leftarrow (2M)$$

* $Z_{out} = \frac{Z_o}{(1+M\beta)} = \frac{75\Omega}{(1+200000\times 0.02)}$

$$\boxed{Z_{out} = 18.75\,m\Omega} \leftarrow (2M)$$

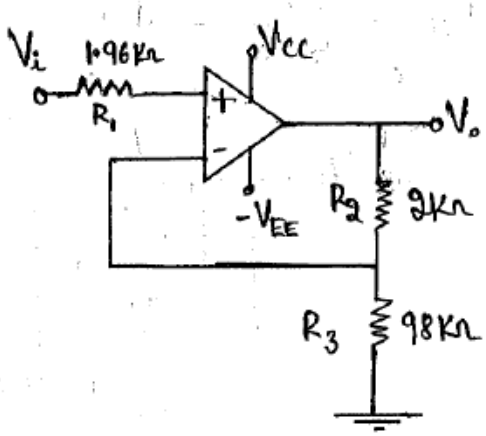
* How do you provide Compensation for the bias current for the amplifier of above question?

Dec-10, 2M

Sol:- Compensation is done by using R_1

i.e. $R_1 = (R_2 \| R_3) = \frac{R_2R_3}{R_2+R_3} = \frac{2k\Omega\times 98k\Omega}{2k\Omega+98k\Omega}$

$$\boxed{R_1 = 1.96k\Omega} \leftarrow (1M)$$



← (1M)

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OP-Amps as AC Amplifiers

Introduction :-

* Op-amp can be used as dc as well as ac amplifier.

For op-amp ac amplifiers, the coupling capacitors are necessary at the I/p as well as o/p terminals. These capacitors must not be allowed to interrupt the bias current paths to the op-amp I/p terminals.

This sometimes requires additional bias resistors which can affect the circuit I/p Impedance.

* Since the capacitors have their highest Impedances at the lowest signal frequency. All the coupling capacitor values are determined at the lower cut-off frequency 'f_1'.

* The Impedance of coupling capacitors at f_1 is usually one tenth of the resistance in series with them.

* The f_1 is determined using largest capacitor in the circuit and capacitive Impedance is made equal to the series resistance.

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Capacitor - coupled voltage follower :-

* Draw a capacitor coupled voltage follower ckt, and explain functions of the capacitors used. Also explain how these capacitors are to be chosen

June - 05, 8M (E&E)

* Design a capacitor - coupled voltage follower using IC 741 op-amp. The lower cut-off frequency for the ckt is to be 100Hz and the load resistance is 4.7 kΩ. Draw the ckt & explain the operation.

Jan - 10, 12M

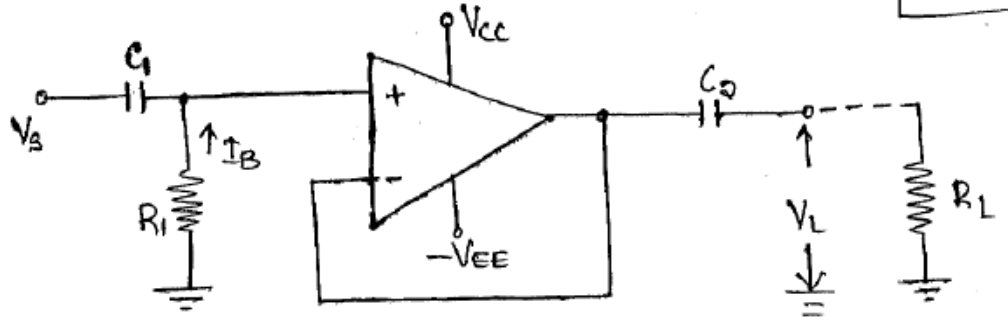
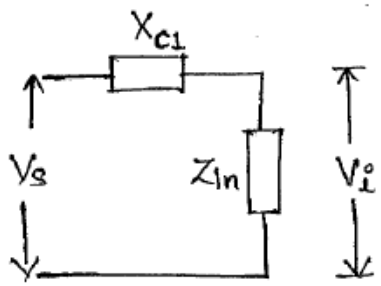
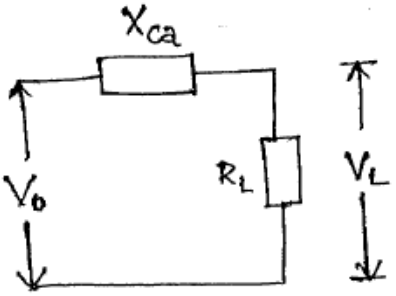


fig @ : capacitor coupled voltage follower ckt



(b) The signal voltage is divided across X_{C1} & Z_{in}



(c) : The o/p voltage is divided across X_{C2} and R_L

Fig @ : shows a capacitor coupled voltage follower ckt.

* The Non-INV terminal must be grounded via a resistor 'R_1'. This resistor is required to pass the bias current to the amplifier Non-INV terminal.

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* A resistor equal to 'R_1' might be included in series with the inverting terminal to equalize the $I_B R_B$ voltage & thus minimize the o/p offset voltage.

* The o/p capacitor C_2 blocks the small dc offset voltage.

Design :

Design involves calculation of R_1, C_1 and C_2.

* The maximum value of R_1 is determined as

$$R_{1(max)} = \frac{0.1\, V_{BE}}{I_{B(max)}}$$

* I/p Impedance of the ckt is

$$Z_{in} = R_1 \parallel Z_i'$$

Where $Z_i' = (1+M\beta) Z_i$

Z_i' is the I/p Impedance at the NON-INV terminal & is very much larger than R_1

$$\therefore \quad Z_{in} = R_1$$

* Load resistor R_L normally has a lower resistance than R_1.

* At the lower 3dB frequency 'f_1', the impedance of C_1 should be much smaller than Z_{in}.

$$\therefore \text{ At } f_1, \quad X_{C1} = \frac{Z_{in}}{10}$$

$$\frac{1}{2\pi f_1 C_1} = \frac{R_1}{10}$$

$$C_1 = \frac{10}{2\pi f_1 R_1}$$

$\left\{ \begin{array}{l} Z_{in} = R_1 \text{ \&} \\ X_{C1} = \frac{1}{2\pi f_1 C} \end{array} \right.$

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$$\therefore \boxed{C_1 = \frac{1}{2\pi f_1 (R_1/10)}}$$

from fig ©, the load voltage V_L is given by:

$$V_L = I R_L$$

Where $I = \frac{V_0}{R_L - jX_{C2}}$

$$V_L = \frac{V_0 R_L}{R_L - jX_{C2}}$$

$$\therefore \text{Magnitude of } V_L = \frac{V_0 R_L}{\sqrt{R_L^2 + X_C^2}}$$

When $X_L = R_L$, then

$$V_L = \frac{V_0 R_L}{\sqrt{R_L^2 + R_L^2}} = \frac{V_0 R_L}{\sqrt{2 R_L^2}} = \frac{V_0 \cancel{R_L}}{\sqrt{2}\,\cancel{R_L}}$$

$$V_L = \frac{V_0}{\sqrt{2}}$$

$$\boxed{V_L = 0.707 V_0}$$

i.e the ckt low 3 dB frequency f_1 occurs when

$X_{C2} = R_L$

$$\therefore X_{C2} = R_L \text{ at } f_1$$

$$\frac{1}{2\pi f_1 C_2} = R_L$$

$$\boxed{C_2 = \frac{1}{2\pi f_1 R_L}}$$

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Capacitor - Coupled voltage follower :-

FORMULAE :- For 741.

1) $R_{1(max)} = \dfrac{0.1 V_{BE}}{I_{B(max)}}$

2) $X_{C1} = \dfrac{R_1}{10}$ at f_1. i.e. $\boxed{C_1 = \dfrac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)}}$

3) $X_{C2} = R_L$ at f_1 i.e. $\boxed{C_2 = \dfrac{1}{2\pi f_1 R_L}}$

4) I/p Impedance, $Z_{in} = R_1$

FORMULAE For- LF 353 BIFET

1) For LF 353 BIFET op-amp, 1st select maximum resistance. i.e. $\boxed{R_1 = R_{1(max)} = 1M\Omega}$

2) $X_{C1} = \dfrac{R_1}{10}$ at f_1. ie. $\boxed{C_1 = \dfrac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)}}$

3) $X_{C2} = R_L$ at f_1 ie. $\boxed{C_2 = \dfrac{1}{2\pi f_1 R_L}}$

4) I/p Impedance. $Z_{in} = R_1$

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Problems

1) Design a capacitor coupled voltage follower using 741 op-amp. The lower cut-off frequency for the ckt is to be 50Hz and the load resistance is $R_L = 3.9K\Omega$.

Given :- $f_1 = 50Hz$, $R_L = 3.9K\Omega$, Assume $V_{BE} = 0.7V$

For 741 op-amp : $\boxed{I_{B(max)} = 500nA}$

Sol :-

* $R_{1(max)} = \frac{0.1 V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7V}{500nA}$

$\boxed{R_{1(max)} = 140K\Omega}$

Use standard value resistor $\boxed{R_{1(max)} = 120K\Omega}$

* $X_{C1} = \frac{R_1}{10}$ at f_1

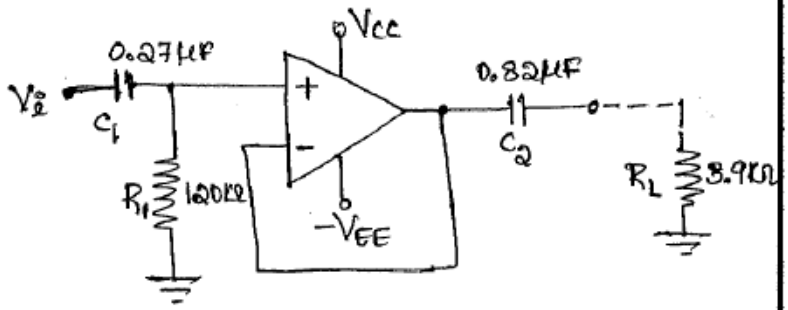
$$C_1 = \frac{1}{2\pi f_1 (R_1/10)} = \frac{1}{2\pi \times 50 \times \left(\frac{120K\Omega}{10}\right)}$$

$\boxed{C_1 = 0.27\mu F}$

* $X_{C2} = R_L$ at f_1

$$C_2 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 50 \times 3.9K\Omega}$$

$\boxed{C_2 = 0.82\mu F}$



NOTE :-

$Z_{in} = R_1 = 120K\Omega$

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2) A 709 op-amp is used in the ckt of a capacitor coupled voltage follower for which $I_{B(max)} = 200nA$. It is desired to have lower cut-off frequency of 30Hz and to supply a load resistance of 5.6 KΩ. Design the component values of R_1, C_1 and C_2.

Given :- $I_{B(max)} = 200nA$, $f_1 = 30Hz$, $R_L = 5.6K\Omega$.

Assume $V_{BE} = 0.7V$.

Sol :-

* $R_{1(max)} = \frac{0.1 V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7V}{200nA} = 350K\Omega$

Use standard value resistor $\boxed{R_{1(max)} = 330K\Omega}$

* $X_{C1} = \frac{R_1}{10}$ at f_1.

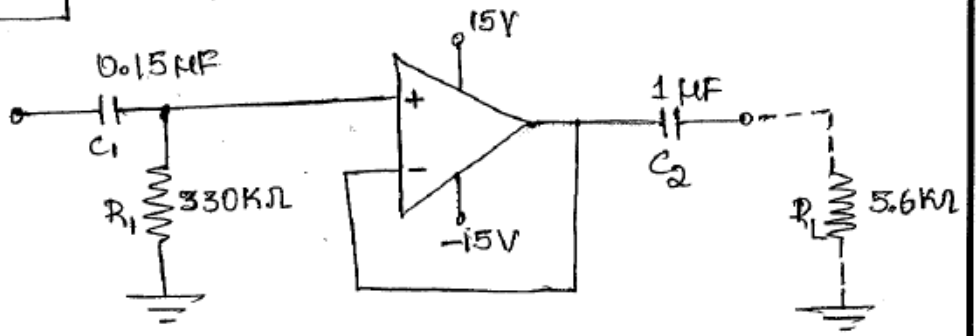
$$C_1 = \frac{1}{2\pi f_1 (R_1/10)} = \frac{1}{2\pi \times 30Hz \times \left(\frac{330K\Omega}{10}\right)} = 0.1608\mu F$$

Choose. $\boxed{C_1 = 0.15\mu F}$

* $X_{C2} = R_L$ at f_1

$$C_2 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 30 \times 3.9K\Omega} = 0.947 MF.$$

Choose $\boxed{C_2 = 1\mu F}$



NOTE :-

$Z_{in} = R_1 = 330K\Omega$

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3) Design a capacitor coupled voltage follower using a 741 op-amp. The lower cut-off frequency for the ckt is to be 50Hz & the load resistance is $R_L = 4K\Omega$.

Given :- $f = 50Hz$, $R_L = 4K\Omega$

for 741 op-amp : $I_{B(max)} = 500nA$

Assume $V_{BE} = 0.7V$.

Sol :-

* $R_{1(max)} = \frac{0.1\,V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7\,V}{500nA} = 140K\Omega$

Choose $\boxed{R_{1(max)} = 120K\Omega}$

* $X_{C1} = \frac{R_1}{10}$ at f_1.

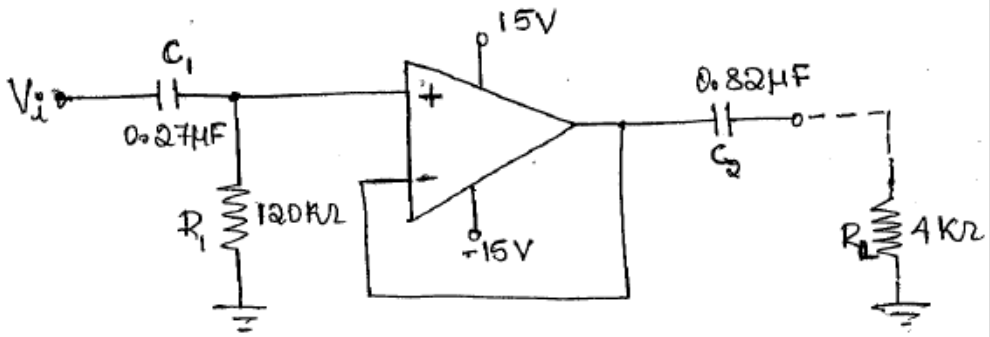
$$C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)} = \frac{1}{2\pi \times 50 \times (120K\Omega/10)}$$

$\boxed{C_1 = 0.27\mu F}$

* $X_{C2} = R_L$ at f_1

$$C_2 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 50 \times 4K\Omega} = 0.79\mu F$$

Choose $\boxed{C_2 = 0.82\mu F}$



NOTE :-

$Z_{in} \simeq R_1 = 120K\Omega$

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4) Design a capacitor coupled voltage follower using a 741 op-amp. The lower cut-off frequency of the ckt is to be 115 Hz. The load resistance is 6.8 KΩ

June-07, 6M (EE)

Given :- $f_1 = 115\,Hz$, $R_L = 6.8\,K\Omega$

For 741 op-amp : $I_{B(max)} = 500nA$

Sol :-

* $R_{i(max)} = \frac{0.1 V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7V}{500nA} = 140K\Omega$

Choose $R_{i(max)} \simeq R_i = 120\,K\Omega$ ← (1m)

* $X_{C1} = \frac{R_i}{10}$ at f_1

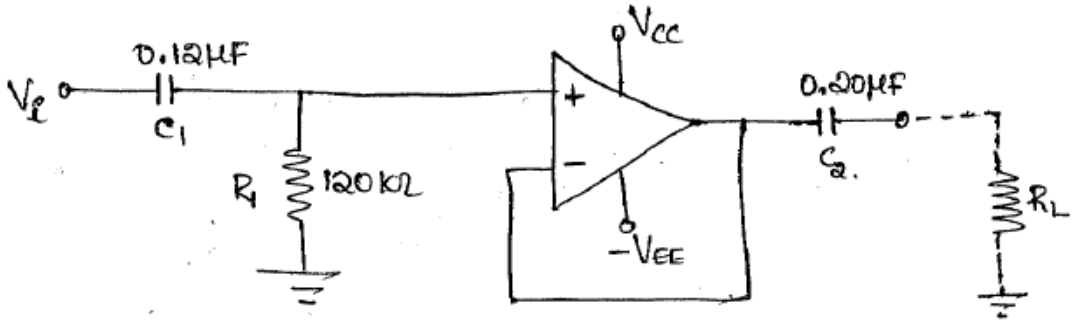
$$C_1 = \frac{1}{2\pi f_1 \left(\frac{R_i}{10}\right)} = \frac{1}{2\pi \times 115 \times \left(\frac{120K\Omega}{10}\right)} = 0.115\mu F$$

Choose $C_1 = 0.12\mu F$ ← (2m)

* $X_{C2} = R_L$ at f_1.

$$C_2 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 115 \times 6.8K\Omega} = 0.20\mu F.$$

$C_2 = 0.20\mu F$ ← (2m)



NOTE :-

$Z_{in} = R_i = 120K\Omega$

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Capacitor - Coupled Voltage follower :-

LF 353 BIFET op-amp → problems.

1) Design a capacitor - coupled voltage follower using a LF 353 BIFET op-amp. The lower cut-off frequency for the ckt is to be 50 Hz & the load resistance is $R_L = 3.9K\Omega$.

Given :- $R_L = 3.9K\Omega$, $f_1 = 50Hz$.

Soln:- For LF 353 BIFET

* Select $\boxed{R_1 = 1M\Omega}$

* $X_{C1} = \frac{R_1}{10}$ at f_1

$$C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)} = \frac{1}{2\pi \times 50 \times \left(\frac{1M\Omega}{10}\right)}$$

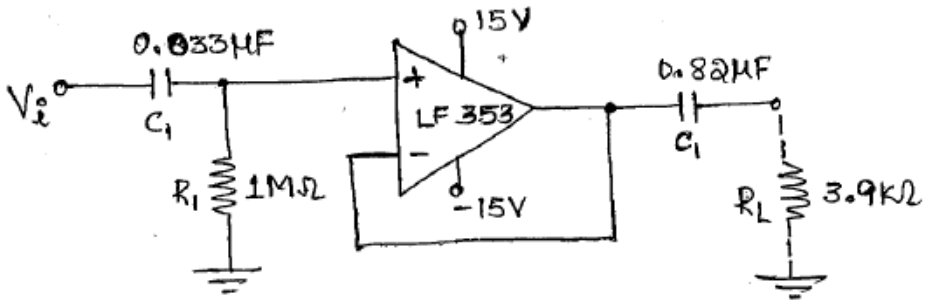
$\boxed{C_1 = 0.032\mu F}$

Choose : $\boxed{C_1 = 0.033\mu F}$

* $X_{C2} = R_L$ at f_1

$$C_2 = \frac{1}{2\pi f_2 R_L} = \frac{1}{2\pi \times 50 \times 3.9K\Omega}$$

$\boxed{C_2 = 0.82\mu F}$



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2) A capacitor - coupled voltage follower is to be designed to have a lower cut off frequency of 110 Hz. The load resistance is 6.8 kΩ & op-amp used is LM 353B. Design a suitable ckt.

Given:- $R_L = 6.8\ k\Omega$, $f_1 = 110\ Hz$.

Sol:- For LM 353B

* Select $\boxed{R_1 = 1M\Omega}$

* $X_{C1} = \frac{R_1}{10}$ at f_1

$$C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)} = \frac{1}{2\pi \times 110 \times \left(\frac{1M\Omega}{10}\right)}$$

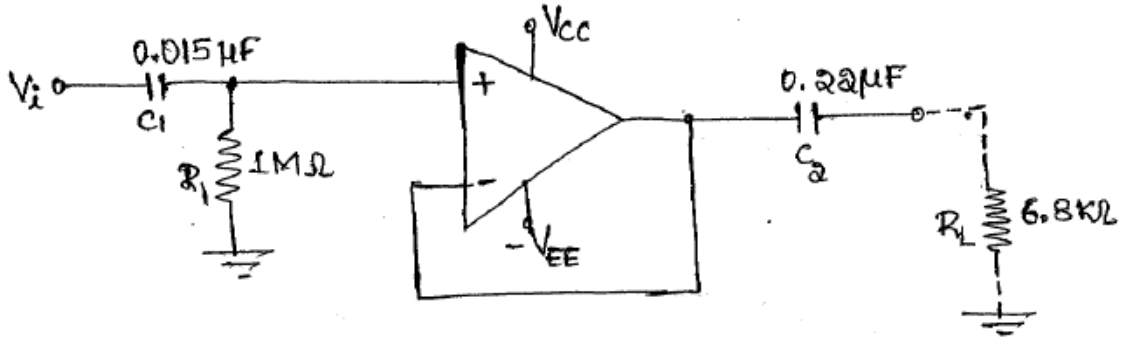
$\boxed{C_1 = 0.0144\mu F}$

Choose $\boxed{C_1 = 0.015\ \mu F}$

* $X_{C2} = R_L$ at f_1

$$C_2 = \frac{1}{2\pi f_1 R_1} = \frac{1}{2\pi \times 110 \times 6.8k\Omega} = 0.213\mu F$$

Choose $\boxed{C_2 = 0.22\mu F}$



NOTE :- $Z_{in} = R_1 = 1M\Omega$.

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* Design a capacitor-coupled voltage follower using IC 741 op-amp. The lower cut-off frequency for the ckt. is to be 100Hz and the load resistance is 4.7KΩ. Draw the ckt & explain the operation.

Jan-10, 12 M

Sol:-

i) Draw the ckt of capacitor-coupled voltage follower & explain with Design procedure. 6M

ii) Given:- $f_1 = 100Hz$, $R_L = 4.7K\Omega$

Sol:- For 741 op-amp: $I_{B(max)} = 500nA$

* $R_{1(max)} = \frac{0.1 V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7V}{500nA} = 140K\Omega$

choose $R_1 = 120K\Omega$

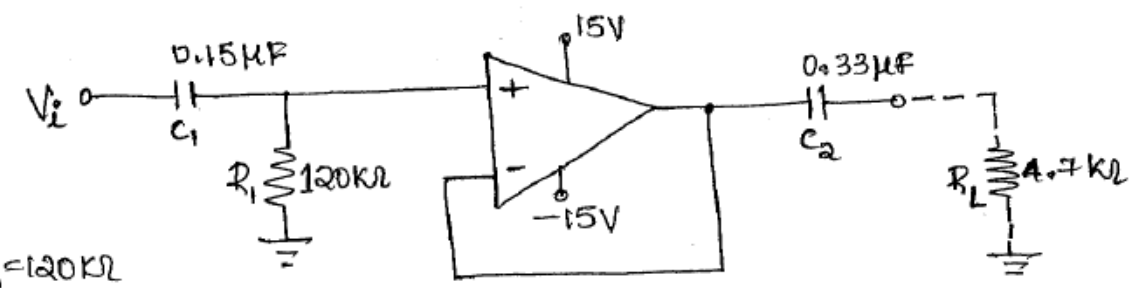
* $X_{C1} = \frac{R_1}{10}$ at f_1.

$C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)} = \frac{1}{2\pi \times 100 \times \left(\frac{120K\Omega}{10}\right)} = 0.132\mu F$

choose $C_1 = 0.15\mu F$

* $X_{C2} = R_L$ at f_1.

$C_2 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 100 \times 4.7K\Omega} = 0.33\mu F$



NOTE:-

$Z_{in} = R_1 = 120K\Omega$

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* A capacitor coupled voltage follower is to be designed to have a lower cut-off frequency of 120Hz. the load resistance is 8.2KΩ & the op-amp used has a maximum I/p bias current of 600nA. Design a suitable ckt.

Jan-05, 6M(EE)

Given:- $f_1 = 120Hz$, $R_L = 8.2K\Omega$, $I_{B(max)} = 600nA$.

Sol:

* $R_{1(max)} = \frac{0.1V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7V}{600nA} = 116.667K\Omega$

choose $R_{1(max)} = 120K\Omega$

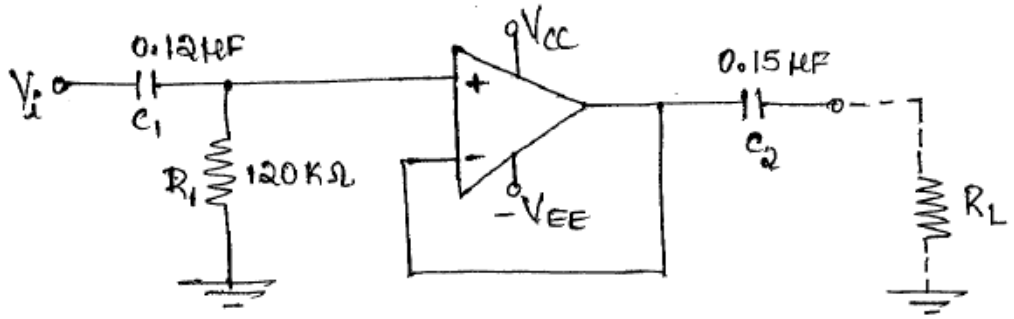
* $C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)} = \frac{1}{2\pi \times 120 \times \left(\frac{120K\Omega}{10}\right)} = 0.11\mu F$

choose $C_1 = 0.12\mu F$

* $C_2 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 120 \times 8.2K\Omega}$

$C_2 = 0.1617\mu F$

choose, $C_2 = 0.15\mu F$



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High Z_{in} capacitor - coupled voltage follower :-

* Sketch the circuit of a high Z_{in} capacitor coupled voltage follower. Briefly explain its operation & show that the I/p impedance is very high compared to the capacitor coupled voltage follower.

June -10, 6M

* Explain the operation of a high I/p impedance capacitor-coupled voltage follower, with a neat circuit diagram. Obtain the expression for I/p impedance of the circuit.

June - 09, 8M

* Sketch the ckt of a high Z_{in} capacitor coupled voltage follower. Obtain the expression for I/p impedance of the circuit.

Jan -10, 8M(EE) | June-09, 8M(EE) | June-06, 6m(EE)

Jan -05, 6m | DEC-10, 8M

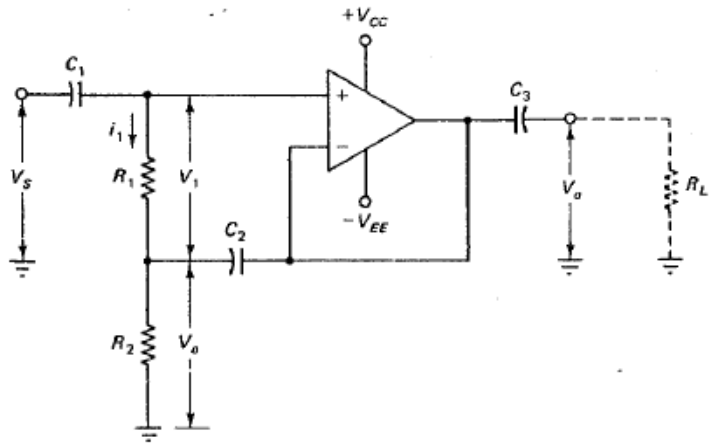

Figure High input impedance capacitor-coupled voltage follower. Feedback via C_2 to the junction of R_1 and R_2 gives an input impedance of $Z_{in} = (1 + M)R_1$.

ARUNKUMAR G M.Tech, *Lecturer in E&CE Dept. S.T.J.I.T., Ranebennur.*

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* The I/p Impedance of the capacitor-coupled voltage follower is set by the value of resistor R_1. This gives a much smaller I/p Impedance than the direct coupled voltage follower.

* Fig ① shows a method by which the I/p Impedance of the capacitor-coupled voltage follower can be substantially increased.

* Capacitor C_2 couples the circuit o/p voltage to the junction of resistors R_1 & R_2.

C_2 behaves as an ac short circuit. so that 'V_0' is developed across R_2.

* Applying KVL from source, R_1 & R_2,

$$V_s - V_1 - V_0 = 0.$$

The voltage across R_1 is V_1 & is given by

$$\boxed{V_1 = V_s - V_0} \rightarrow ①$$

WKT open-loop gain is given by $M = \frac{V_0}{V_1}$

$$\boxed{V_0 = MV_1} \rightarrow ②$$

Sub eq ② in eq ①, we get

$$V_1 = V_s - MV_1$$

$$MV_1 + V_1 = V_s.$$

$$V_1(1+M) = V_s$$

$$\boxed{V_1 = \frac{V_s}{(1+M)}} \rightarrow ③$$

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* The current i_1 is given by :

$$i_1 = \frac{V_1}{R_1} \rightarrow (4)$$

sub eq (3) in eq (4), we get

$$i_1 = \frac{V_s}{(1+M)R_1} \rightarrow (5)$$

* I/p resistance

$$Z_{in} = \frac{V_s}{i_1} \rightarrow (6)$$

sub eq (5) in eq (6), we get

$$Z_{in} = \frac{V_s}{\frac{V_s}{(1+M)R_1}}$$

$$Z_{in} = (1+M)R_1 \rightarrow (7)$$

Since open-loop gain 'M' is very high, this modifies the ckt has very high I/p Impedance.

But if stray capacitance b/w the I/p & ground is present, then I/p Impedance reduces.

Design steps :-

1) $R_{1(max)} = \frac{0.1 V_{BE}}{I_{B(max)}}$

2) $R_{1(max)}$ is split into two equal resistors R_1 & R_2

$$\therefore R_1 = R_2 = \frac{R_{1(max)}}{2}$$

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3) $\therefore C_2 = \frac{1}{2\pi f_1 \left(\frac{R_2}{10}\right)}$

4) $\boxed{C_1 = C_2}$

5) $C_3 = \frac{1}{2\pi f_1 R_L}$

6) $Z_{in} = (1+M)R_1$

PROBLEMS

1) Design a high Z_{in} capacitor coupled voltage follower using 741 op-amp having lower cut-off frequency 50Hz & the load resistance is $R_L = 3.9K\Omega$. Also determine the minimum theoritical I/p impedance of the ckt.

June -10, 6M (EE)

Given:- $f_1 = 50Hz$, $R_L = 3.9K\Omega$

For op-amp 741: $I_{B(max)} = 500nA$, Assume $\boxed{V_{BE} = 0.7V}$

$M(min) = 50000$

Sol:-

* $R_1(max) = \frac{0.1 V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7V}{500\,nA} = \underline{140K\Omega}$

* $R_1 = R_2 = \frac{R_1(max)}{2} = \frac{140K\Omega}{2} = \underline{70K\Omega}$ choose $\boxed{R_1 = R_2 = 68K\Omega}$

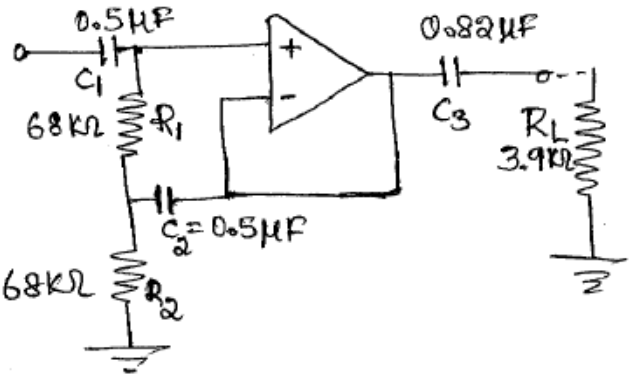
* $C_2 = \frac{1}{2\pi f_1 \left(\frac{R_2}{10}\right)} = \frac{1}{2\pi \times 50Hz \times \left(\frac{68K\Omega}{10}\right)} = \underline{0.5\mu F}$

* $C_3 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 50 \times 3.9K} = \underline{0.082\mu F}$

* $Z_{in(min)} = (1 + M_{(min)})R_1$

$= (1 + 50000)\,68K\Omega$

$\boxed{Z_{in(min)} = 3400K\Omega}$



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2) A capacitor coupled voltage follower using a 709 op-amp is to be designed to have I/p Impedance and to have a lower cut-off frequency of 80Hz. The load resistance is 10kΩ. Design the circuit and find minimum theoritical I/p Impedance of the ckt. [Assume $M = 70,000$ & $I_{B(max)} = 200nA$ for 709 op-amp).

Given :- $f_1 = 80Hz$, $R_L = 10\,k\Omega$

$I_{B(max)} = 200nA$, $M = 70,000$. Assume : $V_{BE} = 0.7V$.

Sol :-

* $R_{i(max)} = \frac{0.1\,V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7V}{200nA} = 350k\Omega$

* $R_1 = R_2 = \frac{R_{i(max)}}{2} = \frac{350\,k\Omega}{2} = 175\,k\Omega$

Choose : $\boxed{R_1 = R_2 = 180\,k\Omega}$

* $C_2 = \frac{1}{2\pi f_1 \left(\frac{R_2}{10}\right)} = \frac{1}{2\pi \times 80 \times \left(\frac{180k\Omega}{10}\right)} = 0.11\,\mu F$

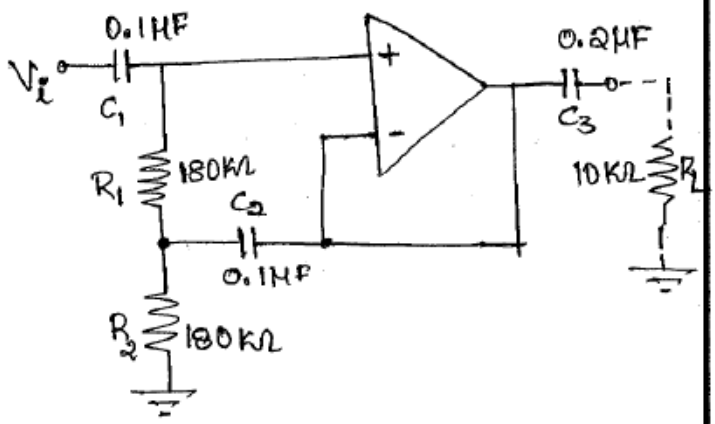
Choose $\boxed{C_2 = 0.1\,\mu F.}$

* $\boxed{C_1 = C_2 = 0.1\,\mu F}$

* $C_3 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 80 \times 10k\Omega} = 0.198\,\mu F$

Choose $\boxed{C_3 = 0.2\,\mu F.}$

* $Z_{in.} = (1+M)R_i =$
$= (1 + 70000)\,180k\Omega$
$= 1.26 \times 10^6\,\Omega.$



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3) Design high Z_{in} capacitor coupled voltage follower using an op-amp having lower cut-off frequency of 50Hz and maximum I/p bias current of 500nA. The load resistance is 3.3KΩ If open loop gain of op-amp is 10^5, find Ideal value of I/p impedance of the ckt.

Given :- $f_1 = 50Hz$, $I_{B(max)} = 500nA$, $R_L = 3.3K\Omega$, $M = 10^5$. Assume $V_{BE} = 0.7V$.

Sol :-

* $R_{i(max)} = \frac{0.1 V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7V}{500nA} = 140K\Omega$

* $R_1 = R_2 = \frac{R_{i(max)}}{2} = \frac{140K\Omega}{2} = 70K\Omega$

choose $\boxed{R_1 = R_2 = 68K\Omega}$

* $C_2 = \frac{1}{2\pi f_1 \left(\frac{R_2}{10}\right)} = \frac{1}{2\pi \times 50 \times \left(\frac{68K\Omega}{10}\right)} = 0.468\mu F$

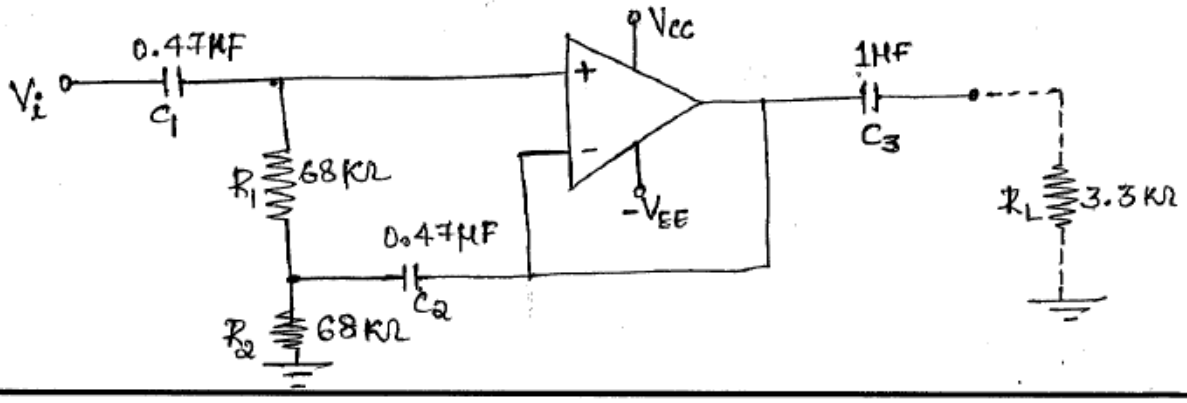
choose $\boxed{C_2 = 0.47\mu F}$

* $\boxed{C_1 = C_2 = 0.47\mu F}$

* $C_3 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 50 \times 3.3K\Omega} = 0.964\mu F$

choose $\boxed{C_3 = 1\mu F}$

* $Z_{in} = (1+M) R_1 = (1+10^5) \times 68K\Omega = 6800M\Omega$



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4) Design Z_{in} capacitor coupled voltage follower using an op-amp having lower cut-off frequency of 50Hz & maximum I/p bias current of 500nA. The load resistance is 3.6KΩ. If the open loop gain is 2×10^5, find Ideal value of I/p Impedance of the ckt. **June-10, 8M**

Given :- $f_1 = 50\,Hz$, $I_{B(max)} = 500\,nA$, $R_L = 3.6K\Omega$, $M = 2\times10^5$

Sol :- $R_{1(max)} = \dfrac{0.1\,V_{BE}}{I_{B(max)}} = \dfrac{0.1\times0.7V}{500nA} = \underline{140K\Omega}$

* $R_1 = R_2 = \dfrac{R_{max}}{2} = \dfrac{140K\Omega}{2} = 70K\Omega$ choose $\boxed{R_1 = R_2 = 68K\Omega}$ ← (2M)

* $C_2 = \dfrac{1}{2\pi f_1\left(\frac{R_2}{10}\right)} = \dfrac{1}{2\pi\times50\times\left(\frac{68K}{10}\right)} = 0.468\,\mu F$

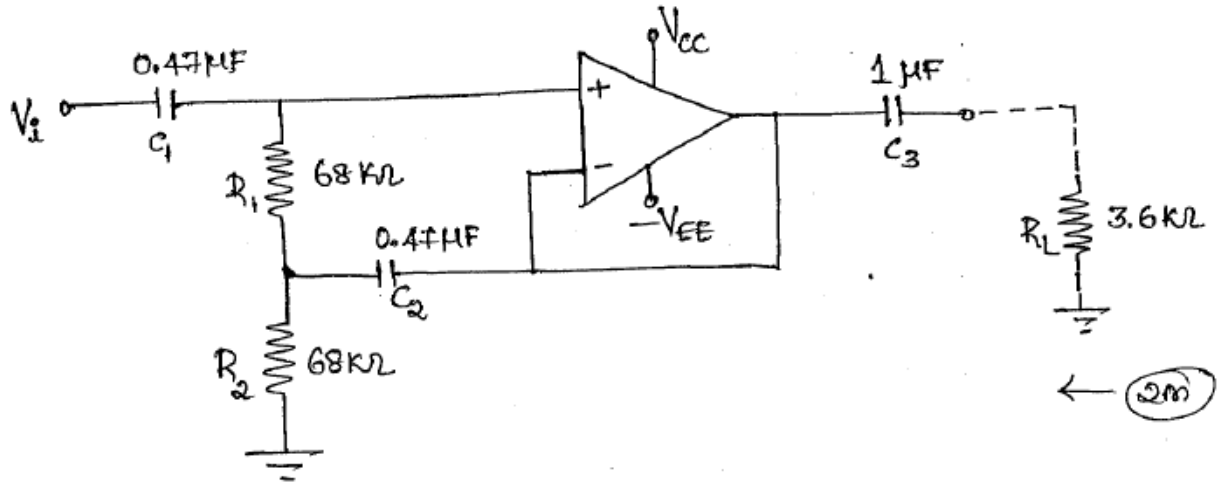
choose $\boxed{C_2 = 0.47\,\mu F}$

* $\boxed{C_1 = C_2 = 0.47\,\mu F}$ ← (2M)

* $C_3 = \dfrac{1}{2\pi f_1 R_L} = \dfrac{1}{2\pi\times50\times3.6K\Omega} = \underline{0.884\,\mu F}$

choose $\boxed{C_3 = 1\,\mu F}$

* $Z_{in} = (1+M)R_1 = (1+2\times10^5)\times68K\Omega = \underline{13600M\Omega}$ ← (2M)



← (2M)

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Capacitor Coupled NON-INV amplifier :-

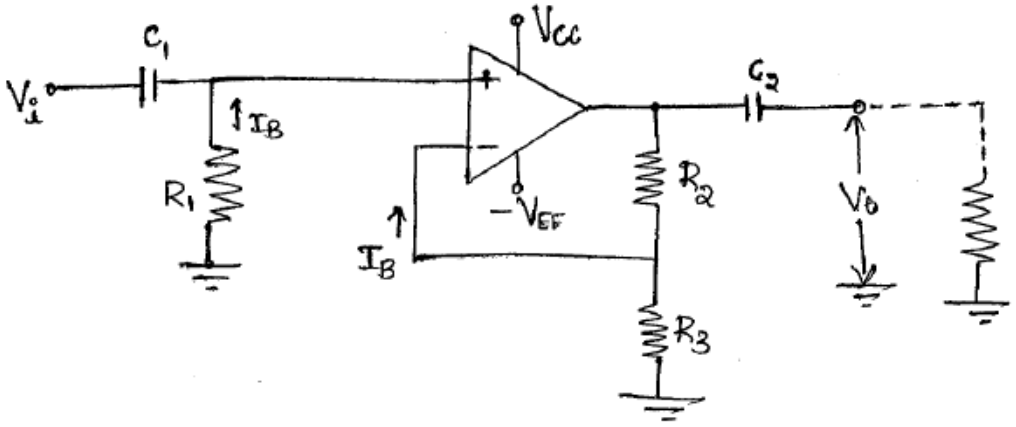

fig ①: capacitor - coupled Non-INV amplifier.

* In capacitor - coupled NON-INV amplifier, the NON-INV I/p terminal is grounded via a resistor to provide a path for the I/p bias current.

* the resistor R_1 may be made equal to $R_2 \parallel R_3$ to compensate for the dc offset voltage at the o/p.

Since the o/p is also capacitor coupled, it is not of much importance.

* The I/p Impedance is given by $\boxed{Z_{in} = R_1}$

Design steps :-

1) $R_1 = R_{1(max)} = \dfrac{0.1\, V_{BE}}{I_{B(max)}}$

2) $X_{C1} = \dfrac{R_1}{10}$ at f_1.

$$C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)}$$

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3) $X_{C2} = R_L$ at f_1.

$$C_2 = \frac{1}{2\pi f_1 R_L}$$

4) $I_2 = 100\, I_{B(max)}$

5) $R_3 = \frac{V_i}{I_2}$

6) $A_V = \frac{V_o}{V_i}$ &.

$$V_o = A_V V_i$$

7) $R_2 + R_3 = \frac{V_o}{I_2}$

$$R_2 = \frac{V_o}{I_2} - R_3$$

OR

$$A_V = 1 + \frac{R_2}{R_3}$$

$$\frac{R_2}{R_3} = (A_V - 1)$$

$$R_2 = R_3(A_V - 1)$$

8) I/p Impedance $Z_{in} = R_1$

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PROBLEMS

1) Using a 741 op-amp, design a capacitor coupled Non-INV amplifier to have a voltage gain of approximately 66. The signal amplitude is to be 15mV. The load resistor is 2.2KΩ and the lower cut-off frequency is to be 120Hz. Make the necessary modifications to give the highest I/p Impedance & determine the required capacitor values.

Given :- $A_V = 66$, $R_L = 2.2K\Omega$, $f = 120Hz$, $V_i = 15mV$.

for 741 op-amp : $\boxed{I_{B(max)} = 500nA}$

Assume $V_{BE} = 0.7V$

Sol :-

1) $R_{1(max)} = \dfrac{0.1 V_{BE}}{I_{B(max)}} = \dfrac{0.1 \times 0.7V}{500 \times 10^{-9}} = \underline{140K\Omega}$

Choose $\boxed{R_1 = R_{1(max)} = 120K\Omega}$

2) $C_1 = \dfrac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)} = \dfrac{1}{2\pi \times 120 \times \left(\frac{120K\Omega}{10}\right)} = \underline{0.11\mu F}$

choose $\boxed{C_1 = 0.12\mu F}$

3) $C_2 = \dfrac{1}{2\pi f_1 R_L} = \dfrac{1}{2\pi \times 120 \times 2.2K\Omega} = \underline{0.6\mu F}$

Choose $\boxed{C_2 = 0.68\mu F}$

4) $I_2 = 100 \times I_{B(max)} = 100 \times 500nA = \underline{50\mu A}$

5) $R_3 = \dfrac{V_i}{I_2} = \dfrac{15mV}{50\mu A} = \underline{300\Omega}$ choose $\boxed{R_3 = 270\Omega}$

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Now. I_2 becomes. $I_2 = \frac{V_i}{R_3} = \frac{15mV}{270\Omega}$

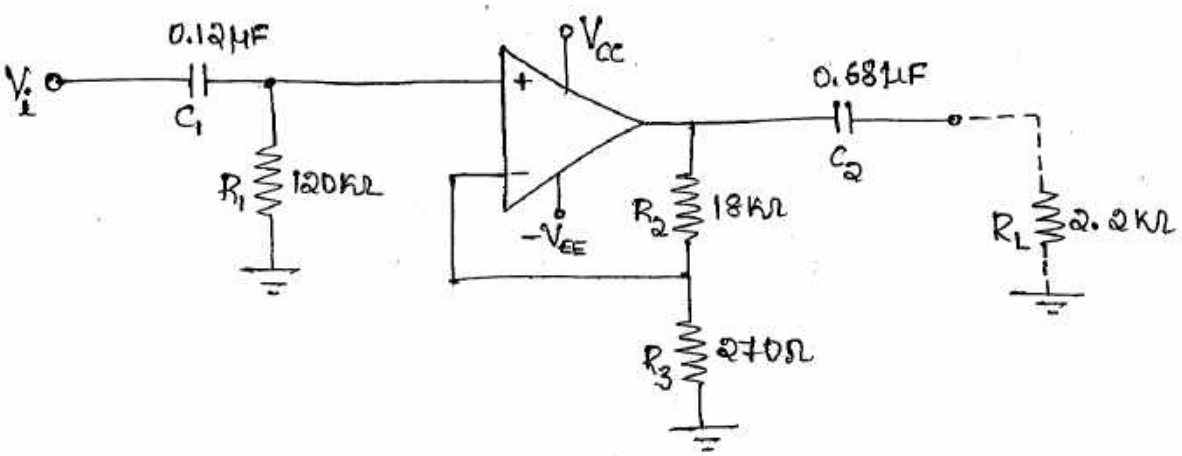
$$\boxed{I_2 = 55.6\mu A}$$

6) WKT $V_o = A_V V_i = 66 \times 15mV$

$$\boxed{V_o = 990mV}$$

7) $R_2 = \left(\frac{V_o}{I_2} - R_3\right) = \left(\frac{990mV}{50\mu A} - 270\Omega\right)$

$$\boxed{R_2 = 17.53K\Omega}$$ Choose $\boxed{R_2 = 18K\Omega}$



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2) A capacitor - coupled Non-INV amplifier is to be used with $A_V = 120$ and $V_L = 4.2$ volts. The load resistance is 8.2 KΩ and the lower cut-off frequency is to be 60Hz. Design a suitable circuit using 715 op-amp for which $I_{B(max)} = 1.5\mu A$.

Given :- $A_V = 120$, $V_L = V_o = 4.2V$, $R_L = 8.2K\Omega$, $f_1 = 60Hz$, $I_{B(max)} = 1.5\mu A$.

Sol :-

1) $R_{1(max)} = \dfrac{0.1 V_{BE}}{I_{B(max)}} = \dfrac{0.1 \times 0.7V}{1.5\mu A} = 46.67 K\Omega$

Choose. $\boxed{R_1 = R_{1(max)} = 47K\Omega}$

2) $C_1 = \dfrac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)} = \dfrac{1}{2\pi \times 60 \times 47K\Omega} = 0.564\mu F$

Choose. $\boxed{C_1 = 0.56\mu F}$

3) $C_2 = \dfrac{1}{2\pi f_1 R_L} = \dfrac{1}{2\pi \times 60 \times 8.2 \times 10^3} = 0.323\mu F$.

Choose. $\boxed{C_2 = 0.33\mu F}$

4) $I_2 = 100 \times I_{B(max)} = 100 \times 1.5\mu A = 0.15mA$.

5) $R_3 = \dfrac{V_i}{I_2}$.

WKT $A_V = \dfrac{V_o}{V_i} \Rightarrow V_i = \dfrac{V_o}{A_V} = \dfrac{4.2V}{120} = 35mV$

$R_3 = \dfrac{35mV}{0.15mA} = 233.33\Omega$. choose $\boxed{R_3 = 220\Omega}$

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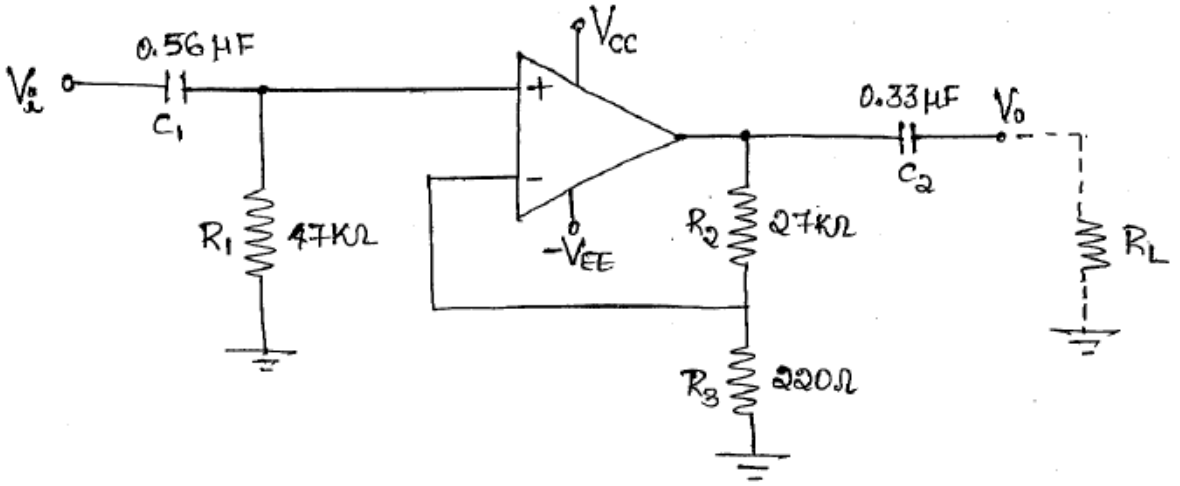
Now I_2 becomes

$$I_2 = \frac{V_i}{R_3} = \frac{35mV}{220\Omega} = 0.159\,mA$$

6) $$R_2 = \left(\frac{V_o}{I_2} - R_3\right) = \left(\frac{4.2V}{0.159\,mA} - 220\Omega\right)$$

$R_2 = 26.19K\Omega$

choose $R_2 = 27K\Omega$



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3) Design a capacitor coupled Non-INV amplifier having Voltage gain of about 75 and the source voltage is 10mV. use following data for the op-amp used.
For op-amp used : $I_{B(max)} = 500nA$, lower-cutoff freq = 100Hz, the load resistance is 3.3kΩ.

Given :- $A_V = 75$, $V_i = 10\,mV$, $I_{B(max)} = 500nA$, $f_1 = 100\,Hz$.
$R_L = 3.3k\Omega$.

Sol :-

1) $R_{1(max)} = \dfrac{0.1\,V_{BE}}{I_{B(max)}} = \dfrac{0.1 \times 0.7\,V}{500\,nA} = 140k\Omega$

choose. $\boxed{R_1 = R_{1(max)} = 120\,K\Omega}$

2) $C_1 = \dfrac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)} = \dfrac{1}{2\pi \times 100 \times \left(\frac{120k\Omega}{10}\right)} = 0.132\mu F$

choose. $\boxed{C_1 = 0.15\mu F}$

3) $C_2 = \dfrac{1}{2\pi f_1 R_L} = \dfrac{1}{2\pi \times 100 \times 3.3k\Omega} = 0.482\mu f$

choose. $\boxed{C_2 = 0.5\,\mu F}$

4) $I_2 = 100 \times I_{B(max)} = 100 \times 500nA$

$\boxed{I_2 = 50\,\mu A}$

5) $R_3 = \dfrac{V_i}{I_2} = \dfrac{10\,mV}{50\,\mu A} = 200\Omega$

$\boxed{R_3 = 200\Omega}$

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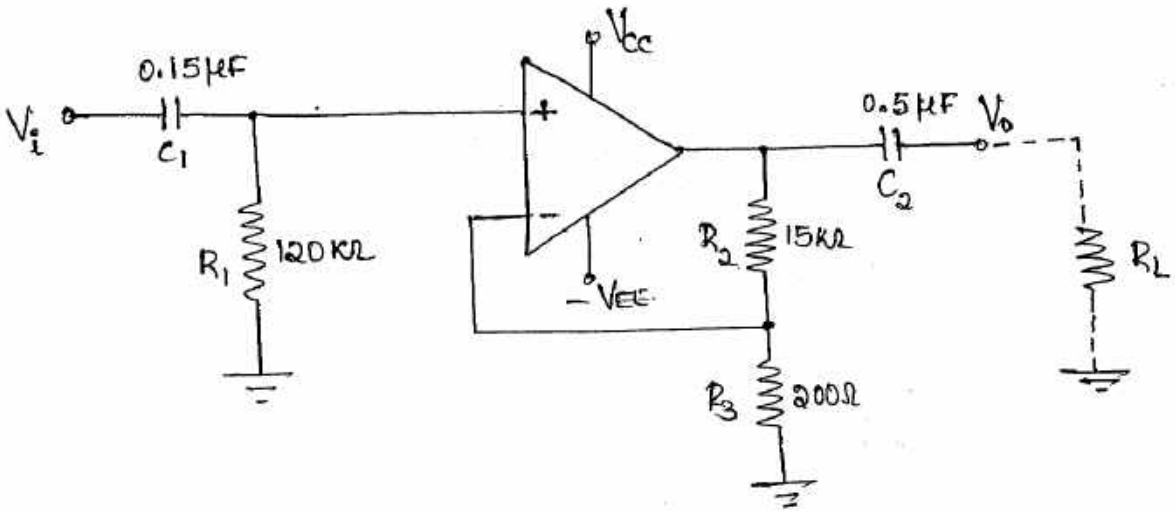
6) $R_2 = \left(\frac{V_o}{I_2} - R_3 \right)$

$= \left(\frac{750\ mV}{50\ \mu A} - 200\Omega \right)$

$V_o = A_V \times V_i = 75 \times 10mV = 750mV.$

$\boxed{R_2 = 14.8\ K\Omega}$

choose $\boxed{R_2 = 15\ K\Omega}$



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4) A capacitor coupled Non-INV amplifier using op-amp is to have $A_V = 100$ and $V_o = 5V$. The load resistance is 10 KΩ and the lower cut-off frequency is to be 100 Hz. Design a suitable ckt.

June-08, 8M

Given :- $A_V = 100$, $V_o = 5V$, $R_L = 10\,K\Omega$, $f_1 = 100\,Hz$.

For 741 op-amp : $I_{B(max)} = 500\,nA$.

Sol :-

* $R_1(max) = \dfrac{0.1\,V_{BE}}{I_{B(max)}} = \dfrac{0.1 \times 0.7V}{500\,nA} = 140\,K\Omega$

choose. $R_1 = 120K\Omega$

* $C_1 = \dfrac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)} = \dfrac{1}{2\pi (100Hz) \times \left(\frac{120\,K\Omega}{10}\right)} = 0.132\,\mu F$

choose. $C_1 = 0.15\,\mu F$

* $C_2 = \dfrac{1}{2\pi f_1 R_L} = \dfrac{1}{2\pi \times 100 \times 10K\Omega} = 0.159\,\mu F$

choose $C_2 = 0.15\,\mu F$

* $I_2 = 100 \times I_{B(max)} = 100 \times 500\,nA = 50\,\mu A$

* $R_3 = \dfrac{V_i}{I_2}$.

WKT $A_V = \dfrac{V_o}{V_i}$

$V_i = \dfrac{V_o}{A_V} = \dfrac{5V}{100} = 50\,mV$

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* $R_3 = \frac{50mV}{50\mu A} = 1K\Omega$

* $R_2 = \left(\frac{V_0}{I_2} - R_3\right) = \left(\frac{5V}{50\mu A} - 1K\Omega\right)$

$R_2 = 99K\Omega$

choose · $R_2 = 1M\Omega$

OR

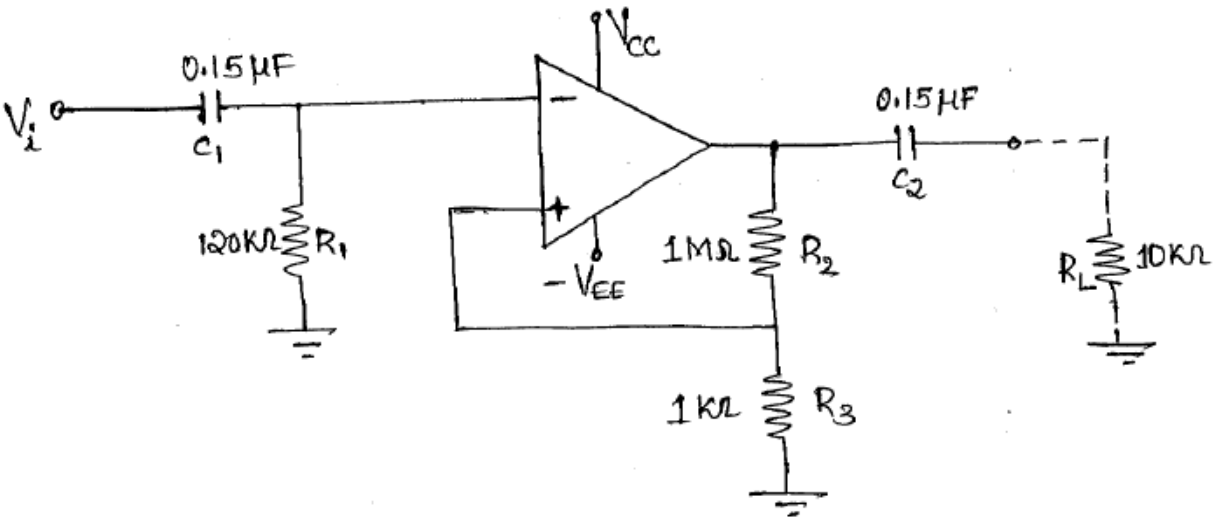
$A_V = 1 + \frac{R_2}{R_3}$

$\frac{R_2}{R_3} = (A_V - 1)$

$R_2 = R_3(A_V - 1)$

$= 1K\Omega(100-1)$

$R_2 = 99K\Omega$



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5) A Non-INV amplifier as in fig ① has the following components $R_1 = 33K\Omega$, $R_2 = 150K\Omega$, $R_3 = 1.5K\Omega$, $R_L = 4.7K\Omega$, $C_1 = 0.39\mu F$, $C_2 = 0.27\mu F$. Determine the ckt Voltage gain, I/p Impedance, and lower cut off freq.

Jan-10, 6M(EE)

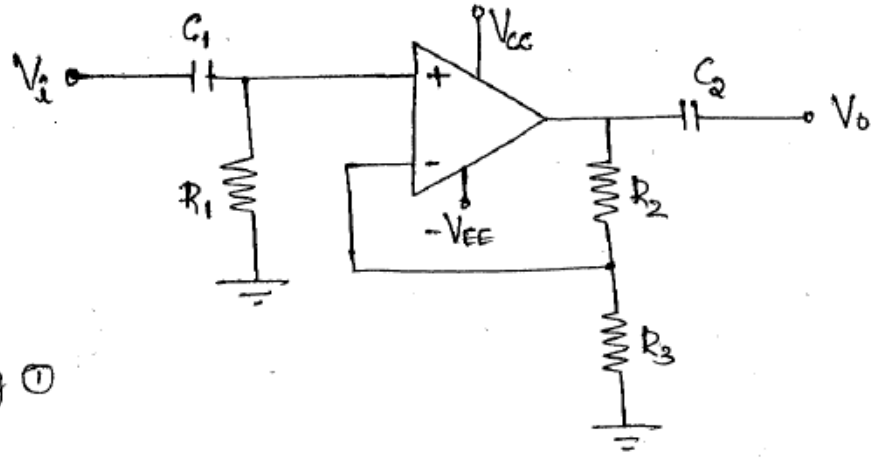

fig ①

Sol :-

i) $A_V = 1 + \frac{R_2}{R_3} = 1 + \frac{150K\Omega}{1.5K\Omega} = .$

ii) $Z_{in} = R_1 = 33K\Omega$

iii) WKT $C_2 = \frac{1}{2\pi f_1 R_L}$

$$f_1 = \frac{1}{2\pi R_L C_2} = \frac{1}{2\pi \times 4.7K\Omega \times 0.27\mu F}$$

$$\boxed{f_1 = 125.41Hz}$$

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High Z_{in} capacitor - coupled Non - INV amplifier :-

1) With a neat ckt diagram, explain the operation of a high I/p Impedance capacitor coupled Non-INV amplifier. Develope the expression for I/p Impedance of the ckt.

June - 08, 8m (EE) | June - 07, 8m (EE) | June - 10, 8M (EE) | Jan - 06, 6m (EE)

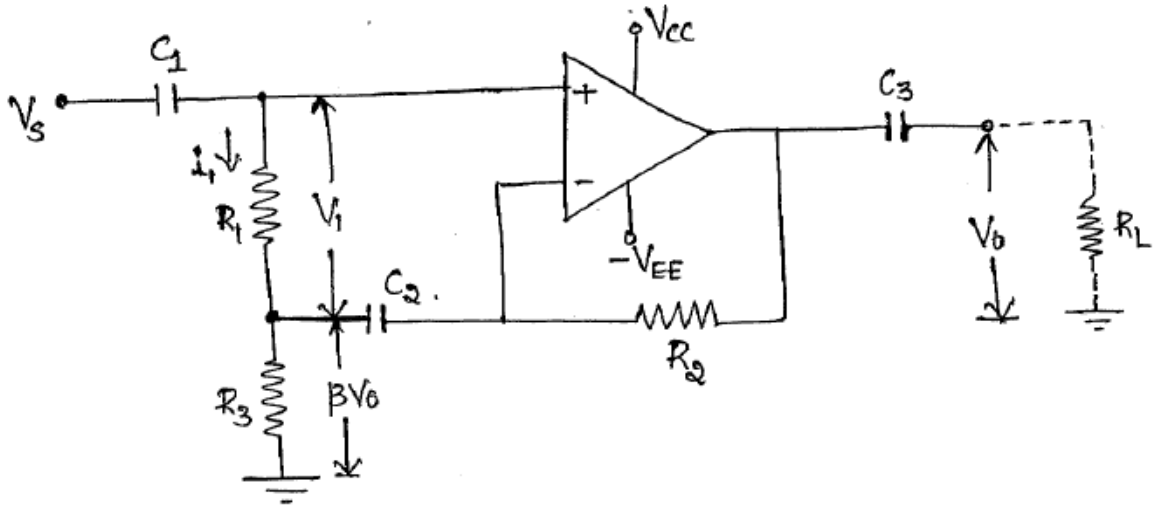

fig ① : High I/p Impedance capacitor-coupled Non-INV amplifier.

* The I/p Impedance of Non-INV amplifier can be improved by using capacitor C_2. The voltage is fed back from the o/p to the I/p via R_2, C_2 and R_3.

∴ The feedback factor 'β' is given by

$$\beta = \frac{R_3}{R_2 + R_3}$$

Applying KVL from V_s, R_1 & R_3, we get :

$$V_s - V_1 - \beta V_o = 0$$

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$$V_1 = V_s - \beta V_0 \rightarrow (1)$$

F/B factor

$$\beta = \frac{V_{R3}}{V_0}$$

$$V_{R3} = \beta V_0.$$

WKT $M = \frac{V_0}{V_1}$

$$V_0 = MV_1 \rightarrow (2)$$

sub. eq (2) in eq (1), we get

$$V_1 = V_s - \beta M V_1$$

$$V_1 + \beta M V_1 = V_s$$

$$V_1 [1 + \beta M] = V_s$$

$$V_1 = \frac{V_s}{(1+\beta M)} \rightarrow (3)$$

* The current $i_1 = \frac{V_1}{R_1}$

$$i_1 = \frac{V_s}{(1+\beta M) R_1} \rightarrow (4)$$

* I/p Impedance is given by:

$$Z_{in} = \frac{V_s}{i_1} \rightarrow (5)$$

Sub eq(4) in eq (5) we get

$$Z_{in} = \frac{V_s}{\frac{V_s}{(1+\beta M) R_1}}$$

$$\therefore Z_{in} = (1+M\beta) R_1$$

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Design steps :-

1) $R_1 + R_3 = R_1(max)$.

$$R_1 + R_3 = R_1(max) = \frac{0.1 V_{BE}}{I_{B(max)}}$$

2) $R_1 + R_3 \approx R_2$

3) $R_1 \approx R_2$

4) $A_V = 1 + \frac{R_2}{R_3}$. $\therefore R_3 = \frac{R_2}{A_V - 1}$.

5) $R_1 + R_3 \approx R_1(max)$

$$\boxed{R_1 = R_1(max) - R_3}$$

6) $X_{C2} = \frac{R_2}{10}$. at f_1

$$C_2 = \frac{1}{2\pi f_1 R_3}$$

7) choose $\boxed{C_1 = 1000pF}$ (To be much larger than stray capacitance)

8) $X_{C3} = R_L$ at f_1

$$C_3 = \frac{1}{2\pi f_1 \left(\frac{R_L}{10}\right)}$$

9) I/p Impedance. $\boxed{Z_{in} = (1+M\beta)R_1}$

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High Z_{in} capacitor coupled Non-INV amplifier :-

Design steps for LF 353 BIFET op-amp :

1) For a BIFET op-amp

Select : $\boxed{R_2 = 1M\Omega}$

2) WKT $A_V = \frac{V_o}{V_i}$

$\therefore A_V = \frac{R_2 + R_3}{R_3}$.

$$\boxed{A_V = 1 + \frac{R_2}{R_3}}$$

3) WKT $A_V = 1 + \frac{R_2}{R_3}$.

$\frac{R_2}{R_3} = A_V - 1$

$$\boxed{R_3 = \frac{R_2}{A_V - 1}}$$

4) $\boxed{R_1 = R_2 - R_3}$

5) $X_{C2} = R_3$ at f_1 , $\boxed{C_2 = \frac{1}{2\pi f_1 R_3}}$

6) $X_{C3} = \frac{R_L}{10}$ at f_1 , $\boxed{C_3 = \frac{1}{2\pi f_1 \left(\frac{R_L}{10}\right)}}$

7) Select $C_1 = 1000\,pf$ (To be much larger than stray capacitance).

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PROBLEMS

1). Design a high I/p Impedance capacitor-coupled Non-INV amplifier using 741 op-amp to have a gain of $A_V = 140$ and $f_1 = 120\,Hz$. The I/p signal is 40mV and the load resistance varies from 1.8 KΩ to 20 KΩ Assume $I_{B(max)} = 500nA$.

Given :-

$A_V = 140$, $f_1 = 120\,Hz$, $R_L = 1.8\,K\Omega$ to $20\,K\Omega$,

$I_{B(max)} = 500nA$, $V_i = 40mV$.

Sol :-

* $R_1 + R_3 = R_{1(max)} \simeq \dfrac{0.1\,V_{BE}}{I_{B(max)}} \simeq \dfrac{0.1 \times 0.7V}{500nA} = \underline{140\,K\Omega}$

Choose $\boxed{R_{1(max)} = 150\,K\Omega}$

* $R_1 + R_3 \approx R_2 = R_{1(max)} = 150\,K\Omega$

* $R_3 = \dfrac{R_2}{A_V - 1} = \dfrac{150\,K\Omega}{140 - 1} = \underline{1.08\,K\Omega}$

Choose $\boxed{R_3 = 1K\Omega}$

* WKT $R_1 + R_3 = R_{1(max)}$

$R_1 = R_{1(max)} - R_3$

$= 150K\Omega - 1K\Omega$

$R_1 = 149K\Omega$

Choose $\boxed{R_1 = 150\,K\Omega}$

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* $R_1 \approx R_2 = 150\,K\Omega$

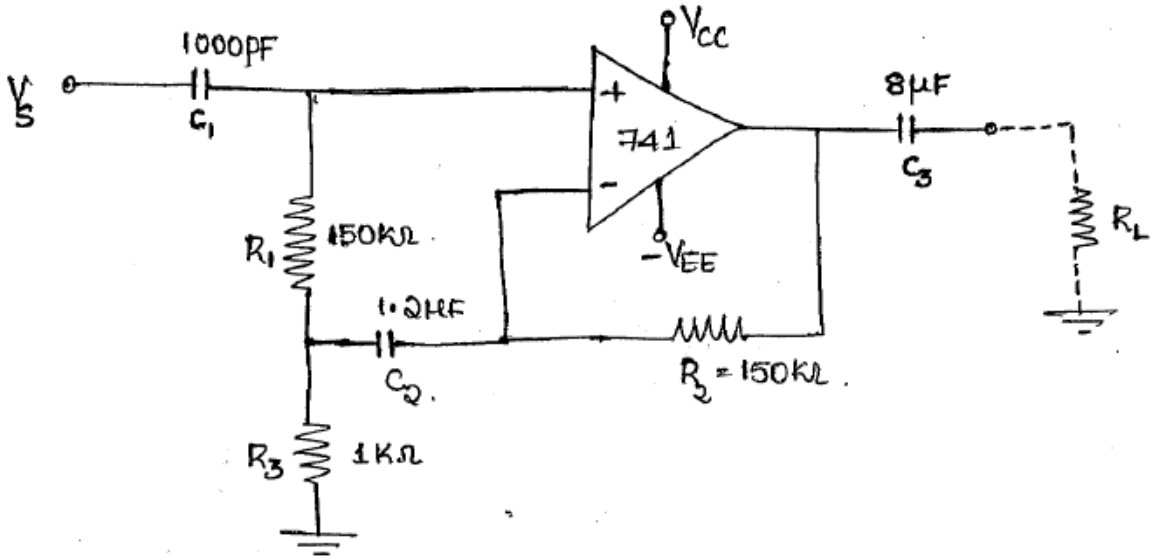
* $C_2 = \dfrac{1}{2\pi f_1 R_3} = \dfrac{1}{2\pi \times 120 \times 1K\Omega} \simeq 1.33\,\mu F.$

Choose. $C_2 = 1.2\,\mu F$

* $C_1 = 1000\,pF.$

* $C_3 \geq \dfrac{1}{2\pi f_1 \left(\frac{RL}{10}\right)} = \dfrac{1}{2\pi \times 120 \times \left(\frac{1.8\times10^3}{10}\right)} \geq 7.36\,\mu F$

Choose. $C_3 = 8\,\mu F$



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BIFET — LF 353 op-amp.

1) Using a LF 353 BIFET op-amp, design a high Z_{in} capacitor-coupled Non-INV amplifier to have a low cut-off frequency of 200 Hz. The I/p & O/p voltages are to be 15 mV and 3V respectively, and the minimum load resistance is 12 KΩ.

Given :- $f_1 = 200Hz$, $V_i = 15mV$, $V_o = 3V$, $R_L = 12K\Omega$

Sol :- $A_V = \frac{V_o}{V_i} = \frac{3V}{15mV}$ $\boxed{A_V = 200}$

* For BIFET op-amp, select $\boxed{R_2 = 1M\Omega}$

* $R_3 = \frac{R_2}{A_V - 1} = \frac{1M\Omega}{200-1} = 5K\Omega$ choose $\boxed{R_3 = 4.7K\Omega}$

* $R_1 = R_2 - R_3 = 1M\Omega - 4.7K\Omega = 995.3K\Omega$, choose $\boxed{R_1 = 1M\Omega}$

* $C_2 = \frac{1}{2\pi f_1 R_3} = \frac{1}{2\pi \times 200 \times 4.7K\Omega} = 0.17\mu F$

choose $\boxed{C_2 = 0.18\mu F}$

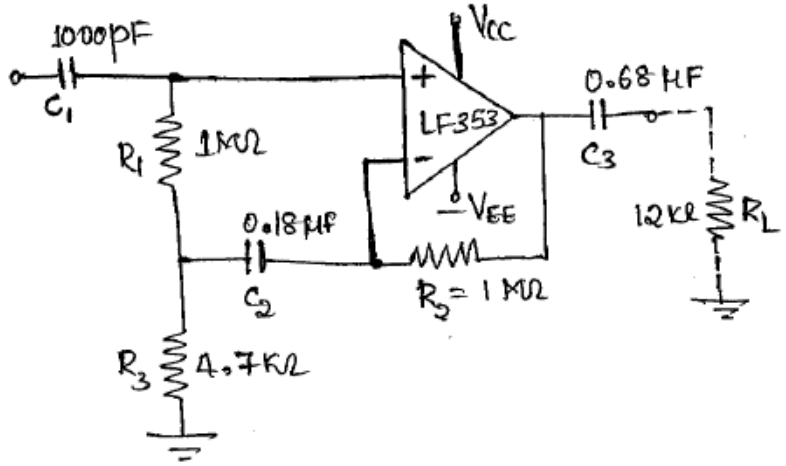
* choose $\boxed{C_1 = 1000pF}$

* $C_3 = \frac{1}{2\pi f_1 \left(\frac{R_L}{10}\right)}$

$= \frac{1}{2\pi \times 200 \times \left(\frac{12K\Omega}{10}\right)}$

$= 0.66\mu F$

choose $\boxed{C_3 = 0.68\mu F}$



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2) A capacitor coupled NON-INV amplifier is to be designed to have high I/p Impedance with a gain of 40dB. If the open loop gain of op-amp is 2×10^5 and I/p Impedance $1.5\times10^6\,\Omega$, calculate the various ckt elements. The required cut-off frequency is 100Hz. The load resistance is 2.2KΩ and I/p parasitic capacitance 15pf. Also calculate the I/p Impedance.

Jan-09, 8M

Given:-

$A_V = 40dB$, $M = 2\times10^5$, $R_L = 2.2K\Omega$

$Z_i = 1.5\times10^6\,\Omega$, $f_1 = 100Hz$, $C_{id} = 15pf$

For op-amp 741 : $I_{B(max)} = 500nA$

Sol:- Gain is given in dB. Convert it to normal gain.

$$(A_V)_{dB} = 20\log_{10}(A_V)$$

$$A_V = \log_{10}^{-1}\left(\frac{A_{V(dB)}}{20}\right)$$

$$\boxed{A_V = 100}$$

* $R_1 + R_3 = R_2$ &

$$R_1 + R_3 = R_{1(max)} = \frac{0.1\,V_{BE}}{I_{B(max)}} = \frac{0.1\times0.7V}{500nA}$$

$\boxed{R_{1(max)} = 140K\Omega}$ choose $\boxed{R_{1(max)} = 150K\Omega}$

* $R_1 + R_3 \approx R_2 = R_{1(max)} = 150K\Omega$ $\therefore$ $\boxed{R_2 = 150K\Omega}$

* $R_3 = \frac{R_2}{A_V - 1} = \frac{150K\Omega}{100-1} = \underline{1.5K\Omega}$

$\boxed{R_3 = 1.5K\Omega}$

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* WKT $R_1 + R_3 = R_1(max)$

$R_1 = R_1(max) - R_3 = 150\,K\Omega - 1.5\,K\Omega$.

$\boxed{R_1 = 148.5\,K\Omega}$ choose $\boxed{R_1 = 150\,K\Omega}$

* i.e. $\boxed{R_1 \approx R_2 = 150\,K\Omega}$

* $C_2 = \frac{1}{2\pi f_1 R_3} = \frac{1}{2\pi \times 100 \times 1.5K\Omega} = 1.06\,\mu F$; choose $\boxed{C_2 = 1\mu F}$

* $C_3 = \frac{1}{2\pi f_1 \left(\frac{R_L}{10}\right)} = \frac{1}{2\pi \times 100 \times \left(\frac{2.2K\Omega}{10}\right)} = 7.2\,\mu F$; choose $\boxed{C_3 = 6.8\mu F}$

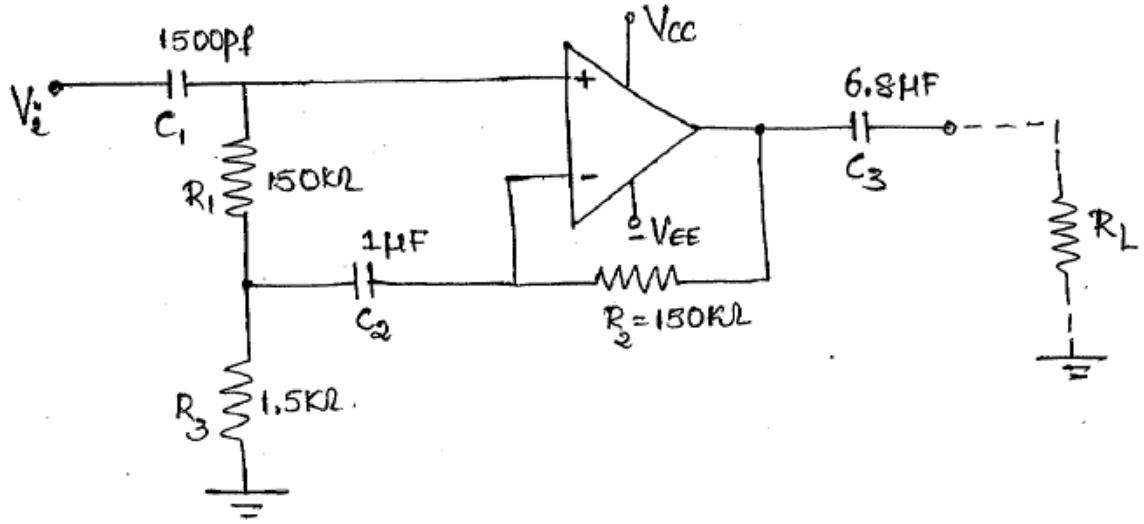
* $C_1 \gg C_{id}$, Let $C_1 = 100 \times C_{id} = 100 \times 15\,pf$, $\boxed{C_1 = 1500pf}$

* $\beta = \frac{R_3}{R_2 + R_3}$

$\beta = \frac{1.5K\Omega}{150K\Omega + 1.5K\Omega} = 0.09 \rightarrow \boxed{\beta \approx 0.01}$

* $Z_{in} = (1 + A\beta) Z_i = (1 + 2 \times 10^5 \times 0.01)\, 1.5 \times 10^6\,\Omega$

$\boxed{Z_{in} = 3 \times 10^9\,\Omega}$



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3) A high I/p Impedance capacitor coupled Non-INV amplifier is to be designed to have $A_V = 120$ and $f_L = 100Hz$ The I/p signal is 50mV & the load resistance ranges from 2.7KΩ to 27KΩ. Design a suitable ckt using a 741 op-amp.

Jan-08, 8M (EE)

Given :- $A_V = 120$, $f_L = 100Hz$, $V_i = 50mV$,

$R_L = 2.7K\Omega$ to $27K\Omega$ i.e Take $\boxed{R_L = 2.7K\Omega}$

For op-amp 741 : $I_{B(max)} = 500nA$

Sol :-

* $R_{1(max)} = \frac{0.1 V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7V}{500nA} = 140K\Omega$

choose $\boxed{R_{1(max)} = 150K\Omega}$

* $(R_1 + R_3) \approx R_2 = R_{1(max)} = 150K\Omega$ $\therefore \boxed{R_2 = 150K\Omega}$

* $R_3 = \frac{R_2}{A_V - 1} = \frac{150K\Omega}{120 - 1} = 1.26K\Omega$

choose $\boxed{R_3 = 1.2K\Omega}$

* WKT $R_1 + R_3 = R_{1(max)}$

$R_1 = R_{1(max)} - R_3 = 150K\Omega - 1.2K\Omega$

$\boxed{R_1 = 148.8K\Omega}$

choose $\boxed{R_1 = 150K\Omega}$ i.e $\boxed{R_1 \approx R_2}$

* $C_2 = \frac{1}{2\pi f_1 R_3} = \frac{1}{2\pi \times 100 \times 1.2K\Omega} = 1.32\mu F$

choose $\boxed{C_2 = 1.5\mu F}$

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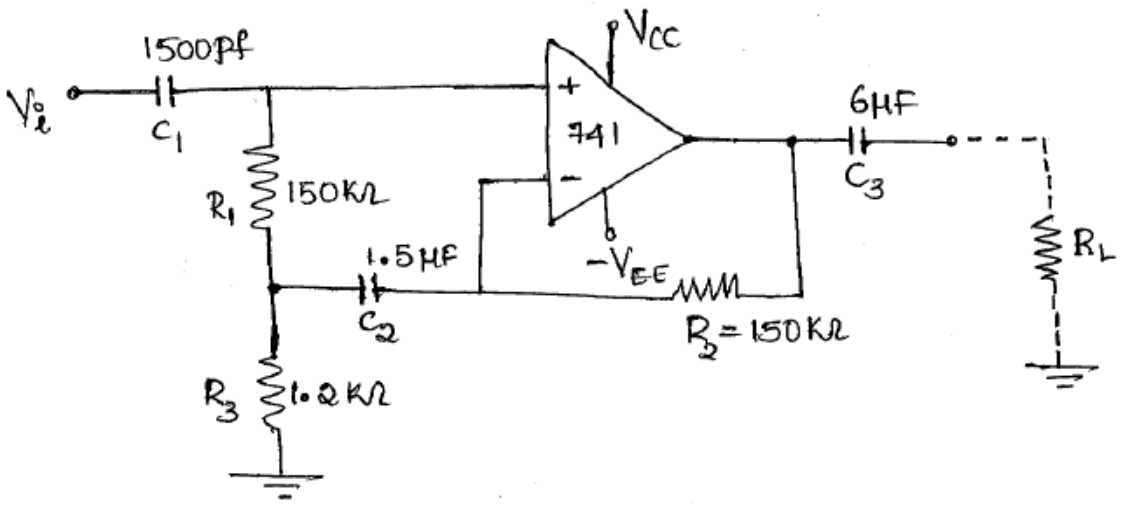
* Select $C_1 = 1500pf$



4) Using a 741 op-amp, design a high Z_{in} Non-INV amplifier to operate with a +36V power supply. The load resistance is 12 KΩ. The lower cut-off frequency is to be 150Hz & the voltage gain is to be 7.

Given :- $R_L = 12K\Omega$, $f_1 = 150Hz$, $A_V = 7$.

For op-amp 741 : $I_{B(max)} = 500nA$

Sol :-

* $$R_1(max) = \frac{0.1V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7V}{500nA} = 140K\Omega$$

Choose $\boxed{R_1(max) = 150K\Omega}$

* $R_1 + R_3 \approx R_2 = R_1(max) = 150K\Omega$

$\boxed{R_2 = 150K\Omega}$

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* $R_3 = \frac{R_2}{A_V - 1}$

$= \frac{150K\Omega}{7-1} = 25\,K\Omega$, choose $\boxed{R_3 = 27K\Omega}$

* WKT $R_1 + R_3 = R_{1(max)}$

$R_1 = R_{1(max)} - R_3 = 150K\Omega - 27K\Omega$

$\boxed{R_1 = 123\,K\Omega}$ choose $\boxed{R_1 = 120\,K\Omega}$

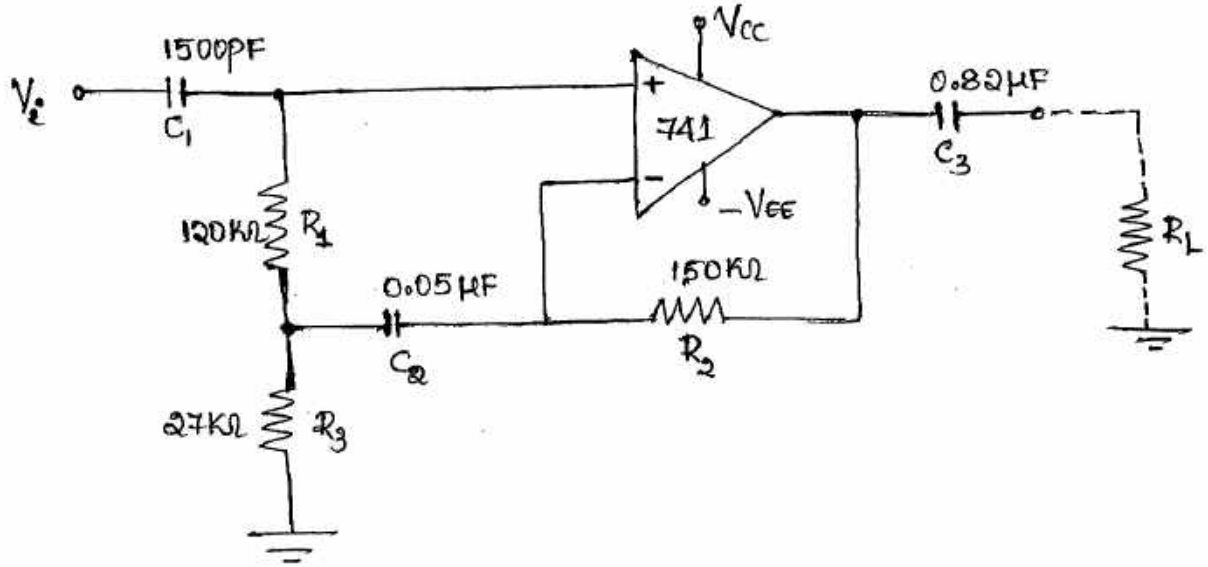
* $C_2 = \frac{1}{2\pi f_1 R_3} = \frac{1}{2\pi \times 150 \times 27K\Omega} = 0.039\mu F$

choose, $\boxed{C_2 = 0.05\mu F}$

* $C_3 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)} = \frac{1}{2\pi \times 150 \times \left(\frac{12K\Omega}{10}\right)} = 0.884\,\mu F$

choose, $\boxed{C_3 = 0.82\,\mu F}$

* Choose $\boxed{C_1 = 1500pf}$



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Capacitor - Coupled INVERTING Amplifier :-

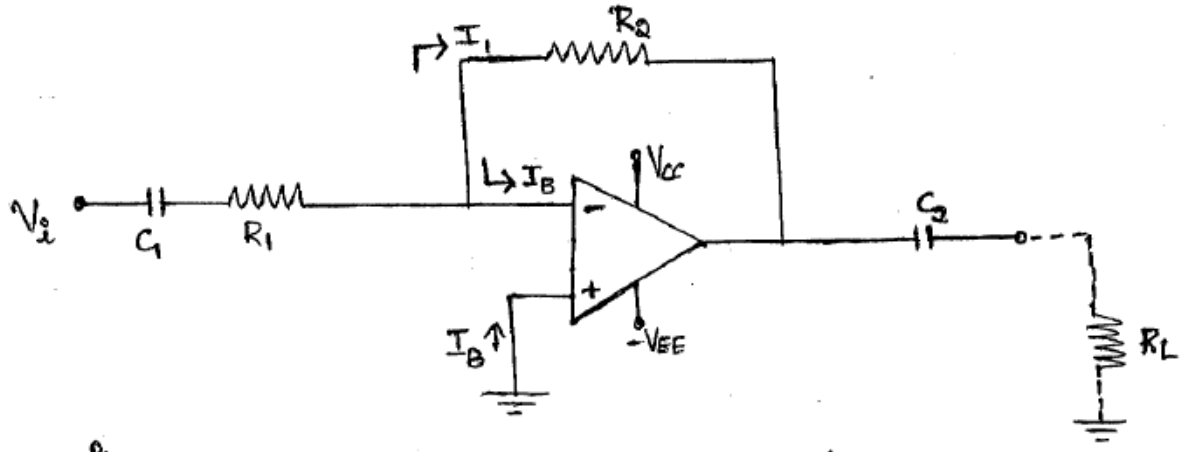

fig ① : Capacitor - coupled INV - amplifier.

* In capacitor coupled INV amplifier, the bias current to the op-amp. INV terminal flows via R_2, so coupling capacitor C_1 does not interrupt the I/p bias current.

* No resistor is included in series with the Non-INV I/p terminal because of a <u>small dc offset</u> is unimportant with a <u>capacitor coupled</u> o/p.

* The I/p Impedance $\boxed{Z_{in} = R_1}$

Design steps :-

1) Let $I_1 = 100 \times I_{B(max)}$.

2) $R_1 = \frac{V_i}{I_1}$

3) $R_2 = \frac{V_o}{I_1}$

4) $X_{C1} = \frac{R_1}{10}$ at f_1 $\qquad \boxed{C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)}}$

5) $X_{C2} = R_L$ at f_1. $\qquad \boxed{C_2 = \frac{1}{2\pi f_1 R_L}}$

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PROBLEMS.

1) A capacitor - coupled INV amplifier has the following components: $R_1 = 2.7K\Omega$, $R_2 = 100K\Omega$, $R_L = 1.5K\Omega$, $C_1 = 3.9\mu F$, $C_2 = 0.68\mu F$. Determine the ckt voltage gain, lower cut-off frequency and Impedance of C_1 at f_1. Draw the ckt & insert the given values.

June-08, 6M(EE)

Given:- $R_1 = 2.7K\Omega$, $R_2 = 100K\Omega$, $R_L = 1.5K\Omega$, $C_1 = 3.9\mu F$, $C_2 = 0.68\mu F$.

Sol:- * Voltage gain:

$$A_V = -\frac{R_2}{R_1} = -\frac{100K\Omega}{2.7K\Omega} = -37$$

$$|A_V| = 37$$

* $C_2 = \frac{1}{2\pi f_1 R_L}$

$$f_1 = \frac{1}{2\pi R_L C_2} = \frac{1}{2\pi \times 1.5K\Omega \times 0.68\mu F}$$

$$f_1 = 156.03\,Hz$$

$$X_{C1} = \frac{1}{2\pi f_1 C_1} = \frac{1}{2\pi \times 156.03 \times 3.9\mu F}$$

$$X_{C1} = 261.54\,\Omega$$

NOTE:-

I/p Impedance.

$$Z_{in} = R_1 = 2.7K\Omega$$

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2) A capacitor coupled INV amplifier uses the following components: $R_1 = 3.9K\Omega$, $R_2 = 120K\Omega$, $R_L = 2.2K\Omega$, $C_1 = 4.7\mu F$, $C_2 = 0.82\mu F$. Find the

i) ckt voltage gain (ii) I/p Impedance

iii) Lower cut-off freq: f_1 (iv) Impedance of C_1 at f_1.

Sol:-

i) $|A_V| = \frac{R_2}{R_1} = \frac{120K\Omega}{3.9K\Omega}$ $\boxed{|A_V| = 30.77}$

ii) $\boxed{Z_{in} = R_1 = 3.9K\Omega}$

iii) $f_1 = \frac{1}{2\pi C_1 \left(\frac{R_1}{10}\right)} = \frac{1}{2\pi \times 4.7\mu F \times \left(\frac{3.9K\Omega}{10}\right)}$

$\boxed{f_1 = 86Hz}$

iv) $X_{C1} = \frac{1}{2\pi f_1 C_1} = \frac{1}{2\pi \times 86 \times 4.7\mu F}$

$\boxed{X_{C1} = 393.75\Omega}$

Design for BIFET op-amp:-

1) Select $\boxed{R_2 = 1M\Omega}$ for BIFET op-amp.

2) WKT $|A_V| = \frac{R_2}{R_1}$

$\boxed{R_1 = \frac{R_2}{|A_V|}}$

3) $C_1 = \frac{1}{2\pi f_1 (R_1/10)}$

4) $C_2 = \frac{1}{2\pi f_1 R_L}$

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1) A capacitor coupled INV amplifier is to be designed using BIFET op-amp, having gain $A_V = -180$ & lower dB frequency $f_1 = 75\,Hz$. The I/p signal available is 40mV & the load resistance $R_L = 1.8\,K\Omega$. Design the ckt

Given :- $|A_V| = 180$, $f_1 = 75\,Hz$, $R_L = 1.8\,K\Omega$, $V_i = 40\,mV$

Sol :- For BIFET op-amp.

* choose $\boxed{R_2 = 1M\Omega}$

* $|A_V| = \frac{R_2}{R_1}$

$$R_1 = \frac{R_2}{|A_V|} = \frac{1M\Omega}{180} = 5.55K\Omega,$$

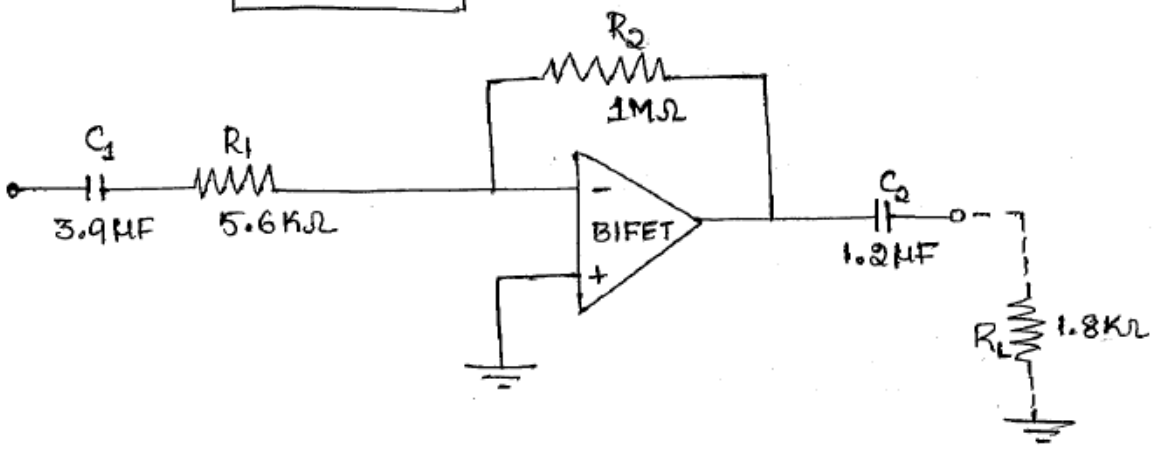
choose $\boxed{R_1 = 5.6K\Omega}$

* $C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)} = \frac{1}{2\pi \times 75 \times \left(\frac{5.6K\Omega}{10}\right)} = 3.79\mu F$

choose $\boxed{C_1 = 3.9\mu F}$

* $C_2 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 75 \times (1.8 \times 10^3)} = 1.18\mu F$

Choose $\boxed{C_2 = 1.2\mu F}$



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* Design capacitor coupled INV amplifier using op-amp 741 to have voltage gain of 100. Assume signal voltage of 10mV and load of 4.7KΩ.

Given: $A_V = 100$, $V_i = 10mV$, $R_L = 4.7K\Omega$

Sol:- For op-amp 741 : $I_{B(max)} = 500nA$

* Let $I_1 = 100 \times I_{B(max)} = 100 \times 500nA$

$$\boxed{I_1 = 50\mu A}$$

* $R_1 = \frac{V_i}{I_1} = \frac{10mV}{50\mu A} = 200\Omega$

WKT $A_V = \frac{R_2}{R_1}$

$R_2 = A_V R_1 = 100 \times 200\Omega$

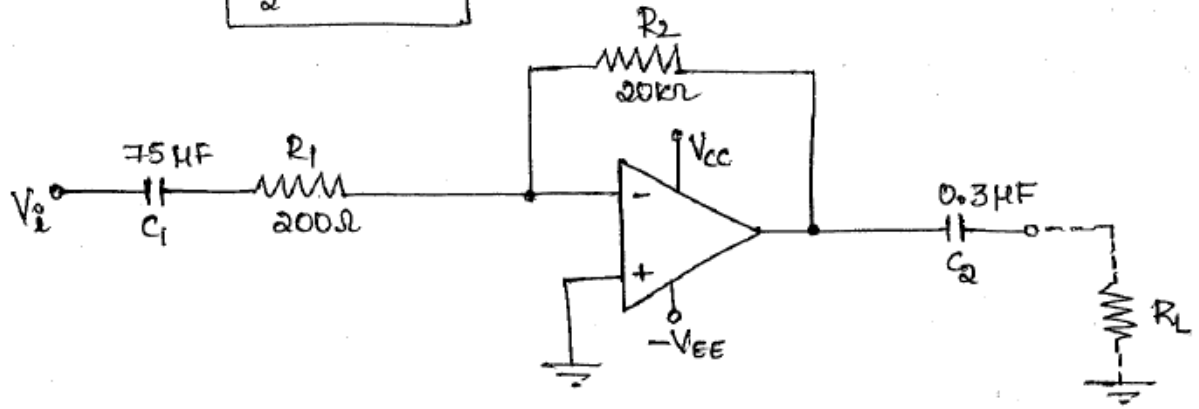
$$\boxed{R_2 = 20K\Omega}$$

* $C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)} = \frac{1}{2\pi \times 120 \times \left(\frac{200}{10}\right)} = 66.31\mu F$

choose $\boxed{C_1 = 75\mu F}$

* $C_2 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 120 \times 4.7 \times 10^3} = 0.2821\mu F$

Choose $\boxed{C_2 = 0.3\mu F}$



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Setting the upper cut-off frequency :-

* Briefly discuss the upper cut-off frequency of an op-amp ckt. show how the cut-off frequency can be set for inverting and NON-INV amplifiers.

Jan-06, 8m(EE) | June-09, 6M

* How upper cut-off frequency is decided in an op-amp & when is it necessary? Jan-09, 6M

* Explain how the upper cut-off frequency can be set for inverting & Non-INV amplifiers. June-10, 6M

* Briefly discuss the upper cut-off frequency of an op-amp ckt & show how the cut-off frequency can be set for INV amplifier. Jan-10, 6M(EE)

⇒

* The highest signal frequency that can be processed by an op-amp ckt depends on the op-amp selected (for eg 741, LF353 etc).

for example : If very low frequency signals are to be amplified, as there would be interference from high frequency noise voltages, since these also get amplified.

* If these high frequency noise voltages are to be eliminated, there must be a provision for their effective attenuation.

This can be achieved by setting the upper cut-off frequency just above the highest desired signal frequency.

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This is done by connecting a feedback capacitor C_f from the op-amp o/p to its INV I/p terminal as shown in fig (a) & (b) below.

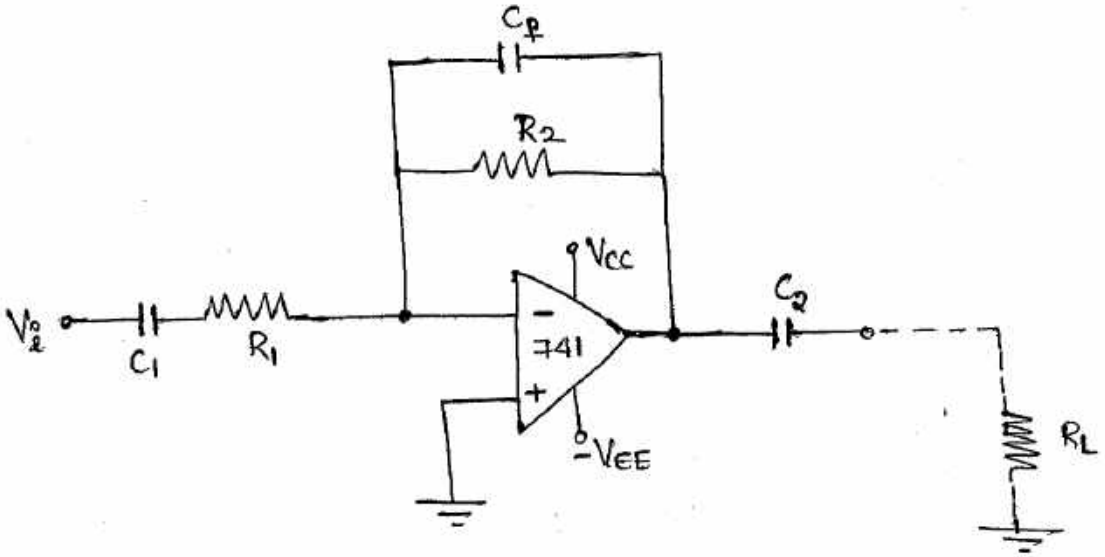

fig (a) : INV amplifier with feedback capacitor C_f to set the upper cut-off frequency.

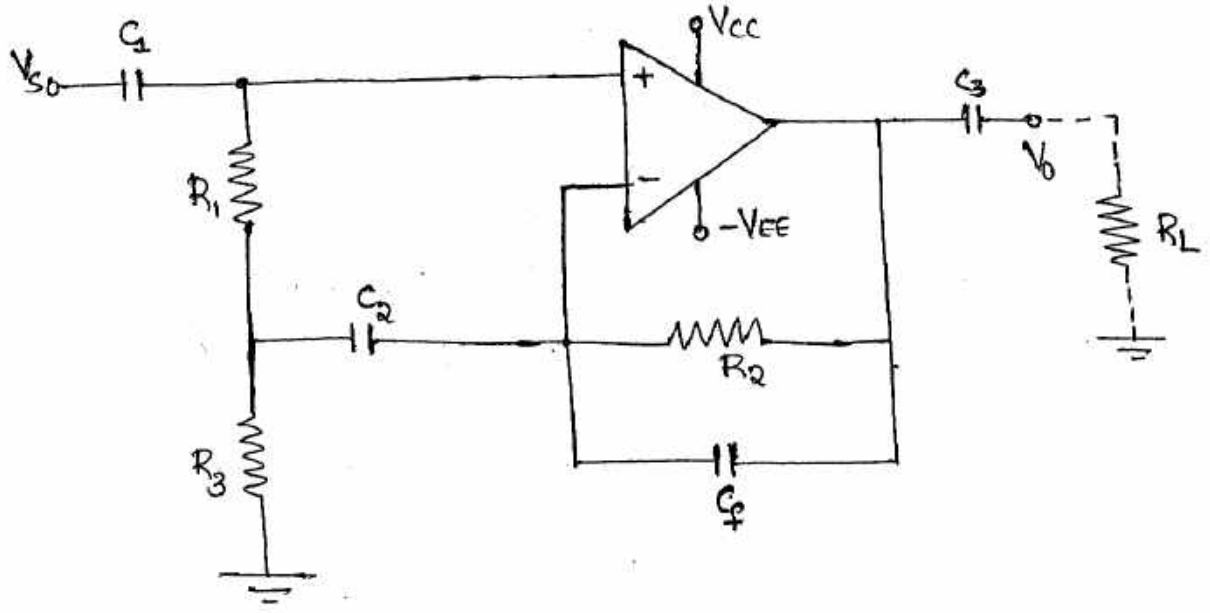

fig (b) : Non-INV amplifier with feedback capacitor C_f to set the upper cut-off frequency.

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* For INV amplifier, the voltage gain is.

$$A_V = \frac{R_2 \parallel X_{cf}}{R_1}$$

$$A_V = \frac{R_2 \cdot X_{cf}}{R_1 (R_2 + X_{cf})}$$

$$A_V = \frac{1}{R_1 \left[\frac{R_2}{R_2 X_{cf}} + \frac{X_{cf}}{R_2 X_{cf}} \right]}$$

$$A_V = \frac{1}{R_1 \left[\frac{1}{X_{cf}} + \frac{1}{R_2} \right]}$$

{ $\left(A_V = \frac{R_2}{R_1} \right)$

In fig @ C_f is in parallel with R_2 so again. becomes.

$\left(\frac{R_2 \parallel X_{cf}}{R_1} \right)$ }.

Magnitude of A_V i.e.

$$A_V = \frac{1}{R_1 \sqrt{\left(\frac{1}{X_{cf}}\right)^2 + \left(\frac{1}{R_2}\right)^2}}$$

When $X_{cf} = R_2$

$$A_V = \frac{1}{R_1 \sqrt{\left(\frac{1}{R_2}\right)^2 + \left(\frac{1}{R_2}\right)^2}}$$

$$= \frac{1}{R_1 \sqrt{2\left(\frac{1}{R_2}\right)^2}}$$

$$= \left(\frac{1}{\frac{R_1}{R_2} \sqrt{2}} \right.$$

$$\boxed{A_V = \frac{1}{\sqrt{2}} \left(\frac{R_2}{R_1} \right)} \rightarrow (1)$$

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The equation ① indicates that the gain is 3dB down the normal voltage gain.

{ ∵ Normal Vltg gain is $A_V = \frac{R_2}{R_1}$ }.

Thus upper cut-off frequency f_2 (or f_H) for the ckt can be set to the desired frequency f_2 by making

$\boxed{X_{cf} = R_2}$ at f_2.

This analysis is applicable to Non-INV amplifier also (Fig ⑥).

Capacitor coupled INV amplifier :-

Design steps :-

1) $I_1 = 100 \times I_{B(max)}$

2) $R_1 = \frac{V_i}{I_1}$

3) $A_V = \frac{R_2}{R_1}$

$\boxed{R_2 = A_V R_1}$

4) $C_1 = \frac{1}{2\pi f_1 (R_1/10)}$ Where $f_1 = f_L$ = lower freq.

5) $C_2 = \frac{1}{2\pi f_2 (R_L)}$ Where $f_2 = f_H$ = Higher frequency.

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PROBLEMS

1) The INV - amplifier is to be capacitor - coupled and to have a signal frequency range of 10Hz to 1KHz. If the load resistance is 250Ω, calculate the required capacitor value. The voltage gain is to be 50 & the o/p vtg amplitude is to be 2.5V.

Given :- $f_1 = 10Hz$, $f_2 = 1KHz$, $R_L = 250\Omega$, $A_V = 50$ & $V_o = 2.5V$.

Sol :-

For op-amp 741 : $I_{B(max)} = 500nA$

* $I_1 = 100 \times I_{B(max)} = 100 \times 500nA$, $\boxed{I_1 = 50\mu A}$

* $A_V = \frac{V_o}{V_i} \Rightarrow V_i = \frac{V_o}{A_V} = \frac{2.5V}{50}$, $\boxed{V_i = 50mV}$

* $R_1 = \frac{V_i}{I_1} = \frac{50mV}{50\mu A}$, $\boxed{R_1 = 1K\Omega}$

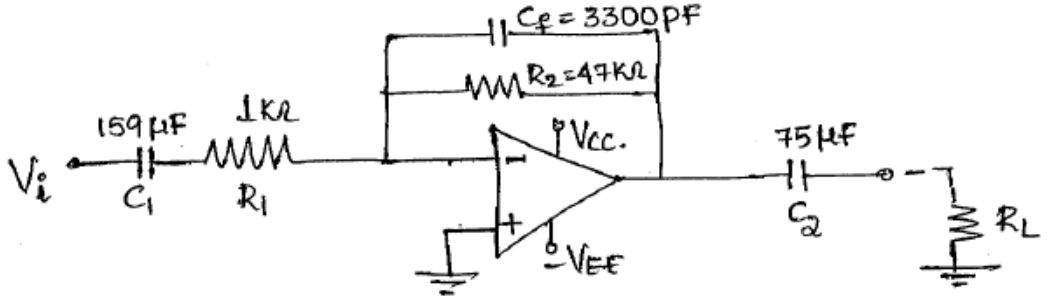
* WKT $A_V = \frac{R_2}{R_1} \Rightarrow R_2 = A_V R_1 = 50 \times 1K\Omega = \underline{50K\Omega}$

choose, $\boxed{R_2 = 47K\Omega}$

* $C_1 = \frac{1}{2\pi f_1 (R_1/10)} = \frac{1}{2\pi \times 10 \times (1K\Omega/10)} = \underline{159\mu F}$

* $C_2 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 10 \times 250\Omega} = \underline{64\mu F}$, choose $\boxed{C_2 = 75\mu F}$

* $C_f = \frac{1}{2\pi f_2 R_2} = \frac{1}{2\pi \times 1KHz \times 47K\Omega} = 3386pF$, choose $\boxed{C_f = 3300pF}$



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2) Design a capacitor coupled INV-amp using μA-741 op-amp, with following specifications: voltage gain = 50, o/p voltage amplitude = 2.5V. The frequency range is 40Hz to 2KHz and load resistance = 250Ω.

June-09, 6M(EE)

Given :- $A_V = 50$, $V_o = 2.5V$, $f_1 = 40Hz$, $f_2 = 2KHz$, $R_L = 250\Omega$

Sol :- For op-amp 741 : $I_{B(max)} = 500nA$

* $I_1 = 100 \times I_{B(max)} = 100 \times 500nA$ $\boxed{I_1 = 50\mu A}$

* WKT $A_V = \frac{V_o}{V_i}$

$$V_i = \frac{V_o}{A_V} = \frac{2.5V}{50}$$

$\boxed{V_i = 50mV}$

* $R_1 = \frac{V_i}{I_1} = \frac{50mV}{50\mu A}$

$\boxed{R_1 = 1K\Omega}$

* WKT $A_V = \frac{R_2}{R_1}$

$R_2 = A_V R_1 = 50 \times 1K\Omega = 50K\Omega$.

Choose. $\boxed{R_2 = 47K\Omega}$

* $C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)} = \frac{1}{2\pi \times 40 \times \left(\frac{1K\Omega}{10}\right)} = 39.78\mu F$

Choose. $\boxed{C_1 = 39\mu F}$

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* $C_2 = \frac{1}{2\pi f_1 R_L}$

$= \frac{1}{2\pi \times 40 \times 250\Omega}$

$C_2 = 15.91\ \mu F$

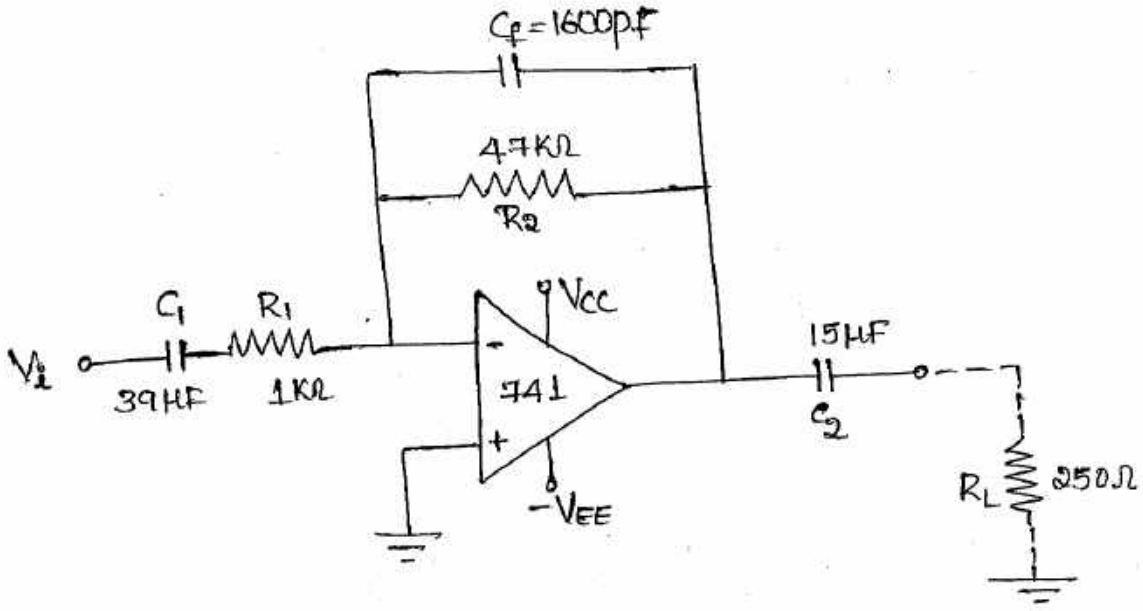
Choose $C_2 = 15\mu F$

* $C_f = \frac{1}{2\pi f_2 R_2}$

$= \frac{1}{2\pi \times 2KHz \times 47K\Omega}$

$C_f = 1693.13\ pF$

Choose $C_f = 1600\ pF$



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3) Design a capacitor coupled INV-amplifier using 741 with a gain of 50 & the o/p amplitude is 2.5 volts. The signal frequency range is 10Hz to 1KHz. The load resistance is 250Ω.

June - 06, 8M(EE)

Given:- $A_V = 50$, $V_o = 2.5V$, $R_L = 250\Omega$

$f_1 = 10Hz$, $f_2 = 1KHz$.

Sol:- For 741 op-amp : $I_{B(max)} = 500nA$

* Let $I_1 = 100 \times I_{B(max)} = 100 \times 500nA$

$$\boxed{I_1 = 50\mu A}$$

* WKT $A_V = \frac{V_o}{V_i}$

$$V_i = \frac{V_o}{A_V} = \frac{2.5V}{50}$$

$$\boxed{V_i = 50mV}$$

* $R_1 = \frac{V_i}{I_1} = \frac{500mV}{50\mu A}$

$$\boxed{R_1 = 1K\Omega}$$

* WKT $A_V = \frac{R_2}{R_1}$

$$R_2 = A_V R_1 = 50 \times 1K\Omega$$

$$\boxed{R_2 = 50K\Omega}$$

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* $C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)} = \frac{1}{2\pi \times 10 \times \left(\frac{1K\Omega}{10}\right)} = 159\,\mu F$

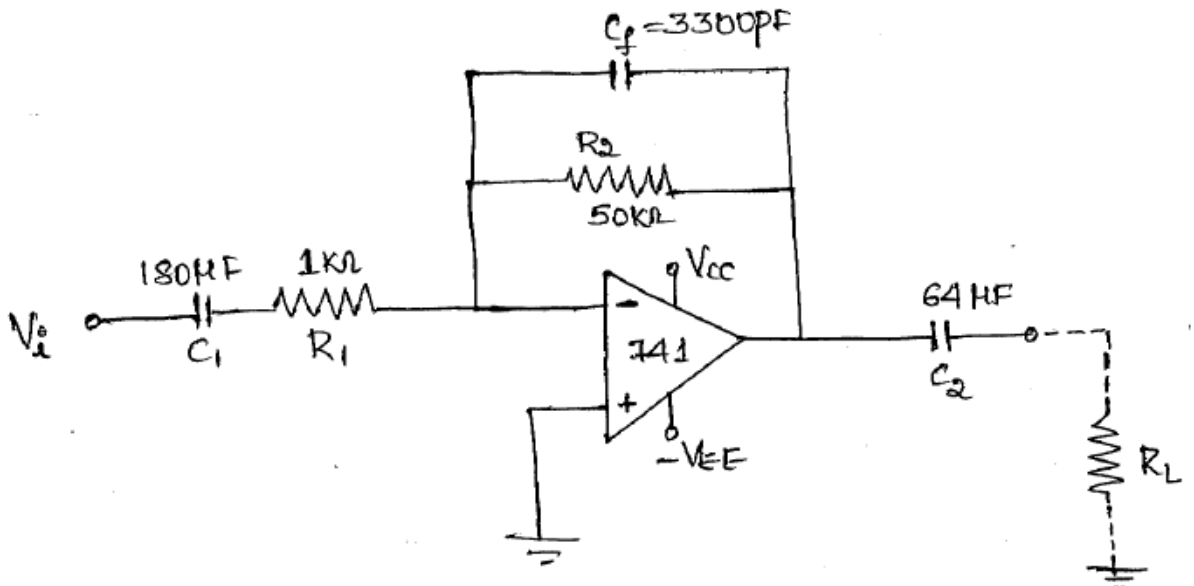
choose $\boxed{C_1 = 180\mu F}$

* $C_2 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 10 \times 250\Omega} = 64\,\mu F$

choose $\boxed{C_2 = 75\mu F}$

* $C_f = \frac{1}{2\pi f_2 R_2} = \frac{1}{2\pi \times 1 \times 10^3 \times 50\,K\Omega} = 3386\,pF$

choose. $\boxed{C_f = 3300pF}$



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4) Design the INV amplifier to operate in a frequency range of 25Hz to 2KHz. The load resistance is 470Ω the required voltage gain is 100 while signal voltage is 10mV. Use op-amp 741.

Given: $f_1 = 25Hz$, $f_2 = 2KHz$, $R_L = 470\Omega$, $A_V = 100$.

$V_i = 10\ mV$.

Sol:- For op-amp 741, $I_{B(max)} = 500nA$

* Let $I_1 = 100 \times I_{B(max)} = 100 \times 500nA$

$\boxed{I_1 = 50\ \mu A}$

* $R_1 = \frac{V_i}{I_1} = \frac{10mV}{50\mu A}$, $\boxed{R_1 = 200\Omega}$

* WKT $R_2 = A_V R_1 = 100 \times 200\Omega = 20K\Omega$, $\boxed{R_2 = 20K\Omega}$

* $C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)} = \frac{1}{2\pi \times 25 \times \left(\frac{200}{10}\right)} = 318.309\ \mu F$

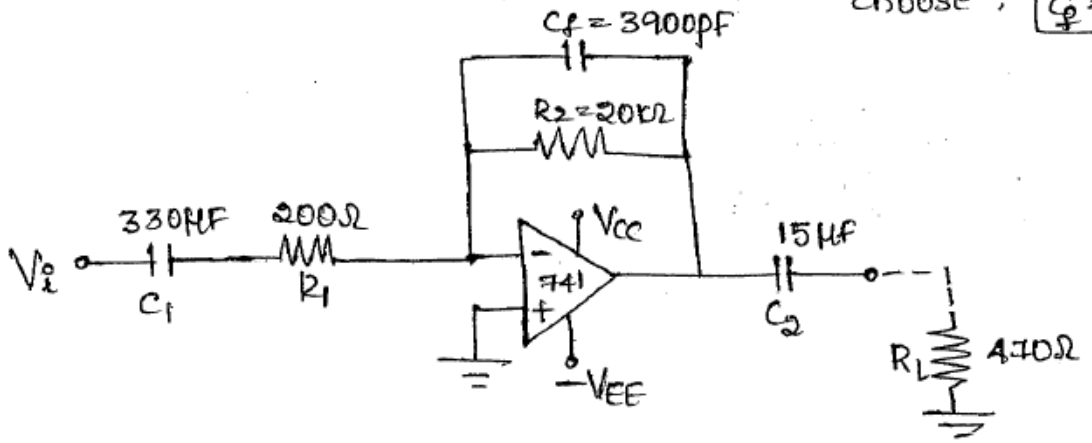
choose, $\boxed{C_1 = 330\mu F}$

* $C_2 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 25 \times 470} = 13.545\ \mu F$

choose $\boxed{C_2 = 15\mu F}$

* $C_3 = \frac{1}{2\pi f_2 R_2} = \frac{1}{2\pi \times 2KHz \times 20K\Omega} = 3978.87\ pf$

choose, $\boxed{C_f = 3900pF}$



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5) Design a capacitor coupled INV amplifier using a 741 op-amp to have a voltage gain of −75, output voltage amplitude of 3 volts and a signal frequency range of 20Hz to 12KHz. The load resistance is 470Ω and $I_{B(max)} = 500nA$.

Given:- $A_V = 75$, $V_o = 3V$, $f_1 = 20Hz$, $f_2 = 12KHz$,
$I_{B(max)} = 500nA$, $R_L = 470\Omega$.

Sol:-

* Let $I_1 = 100 \times I_{B(max)} = 100 \times 500nA$

$$\boxed{I_1 = 50\mu A}$$

* WKT $A_V = \frac{V_o}{V_i}$

$$V_i = \frac{V_o}{A_V} = \frac{3V}{75}$$

$$\boxed{V_i = 40mV}$$

* $R_1 = \frac{V_i}{I_1} = \frac{40mV}{50\mu A} = 800\Omega$

choose. $\boxed{R_1 = 820\Omega}$

* $R_2 = A_V \times R_1 = 75 \times 820\Omega = 61.5K\Omega$

Choose. $\boxed{R_2 = 68K\Omega}$

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* $C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)} = \frac{1}{2\pi \times 20 \times \left(\frac{820\Omega}{10}\right)} = 97.05\ \mu F$

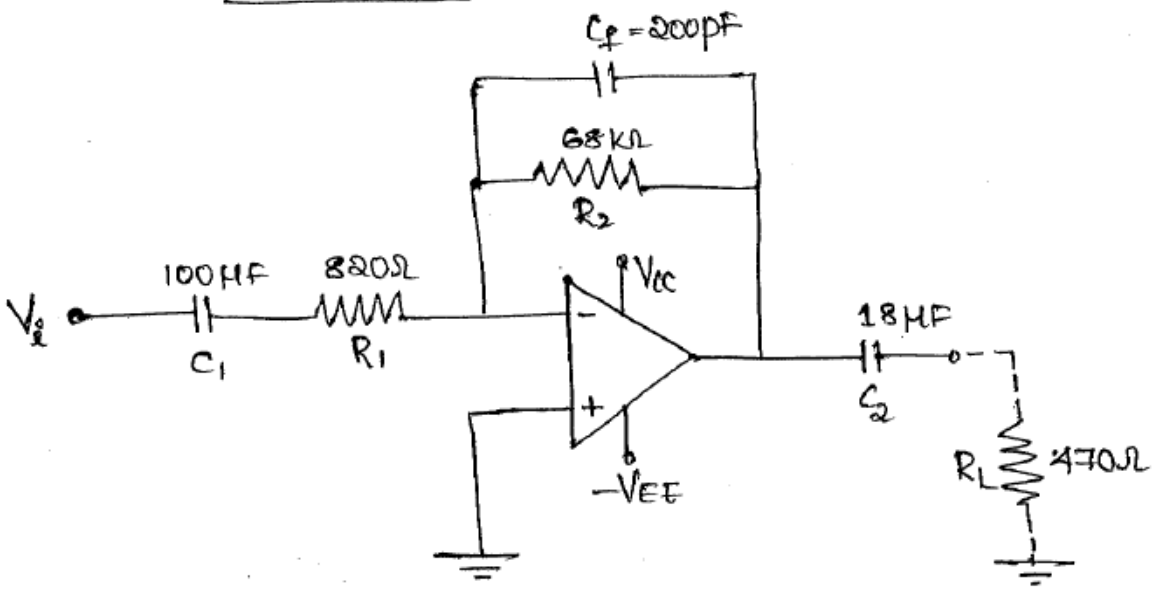
choose $\boxed{C_1 = 100\ \mu F}$

* $C_2 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 20 \times 470\Omega} = 16.93\ \mu F$

choose $\boxed{C_2 = 18\ MF}$

* $C_f = \frac{1}{2\pi f_2 R_2} = \frac{1}{2\pi \times 12 \times 10^3 \times 68 \times 10^3} = 195\ pf$

choose $\boxed{C_f = 200pF}$



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* Design a C-Coupled INV amplifier for a pass-band gain of 100, $f_1 = 120\,Hz$ & $f_2 = 5\,KHz$. Assume $R_L = 2K\Omega$ and use the LF353 BIFET op-amp.

Dec-10, 8M

Given :- $A_V = 100$, $f_1 = 120Hz$, $f_2 = 5KHz$, $R_L = 2K\Omega$

Sol :-

For BIFET op-amp

* Choose $\boxed{R_2 = 1M\Omega}$ ← (1M)

* WKT $A_V = \frac{R_2}{R_1}$

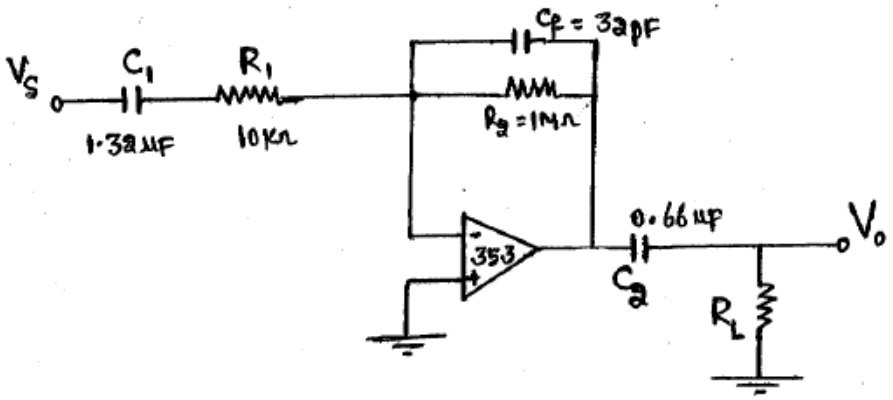
$$R_1 = \frac{R_2}{A_V} = \frac{1M\Omega}{100}$$

$\therefore \boxed{R_1 = 10K\Omega}$ ← (1M)

* $C_1 = \frac{1}{2\pi f_1 (R_1/10)} = \frac{1}{2\pi \times 120 \times \left(\frac{10K\Omega}{10}\right)} = 1.32\,\mu F$ ← (1M)

* $C_2 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 120 \times 2K\Omega} = 0.66\,\mu F$ ← (1M)

* $C_f = \frac{1}{2\pi f_2 R_2} = \frac{1}{2\pi \times 5KHz \times 1M\Omega} = 32pF$ ← (2M)



← (2M)

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Capacitor - Coupled difference amplifier :-

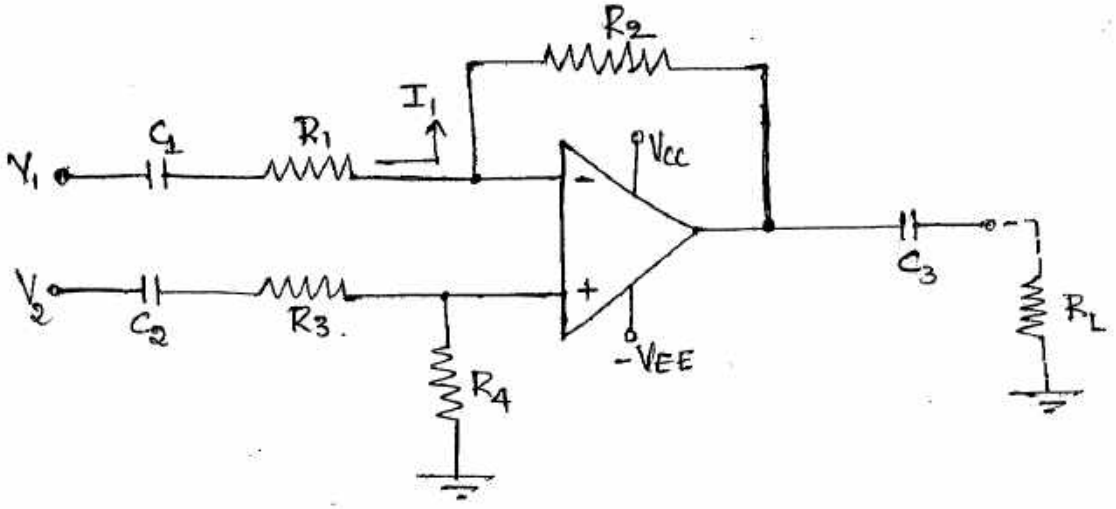

fig ① : Capacitor - coupled difference amplifier.

fig ① shows a capacitor - coupled difference amplifier. this ckt amplifies the difference between two signals applied at the Non-INV and INV terminals of the op-amp.

* The o/p voltage is given by

$$V_0 = (V_2 - V_1)$$

Design steps :-

1) Let $I_1 = 100 \times I_{B(max)}$

2) $R_1 = \frac{V_1}{I_1}$

3) $R_3 = R_1$

4) $R_2 = \frac{V_0}{I_1}$

5) $R_4 = R_2$

6) $X_{C1} = \frac{R_1}{10}$ at R_1, $\quad C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)}$

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7) $X_{C2} = (R_3 + R_4) / 10$ at f_1.

$$C_2 = \frac{1}{2\pi f_1 \left(\frac{R_3 + R_4}{10}\right)}$$

8) $X_{C3} = R_L$ at f_1.

$$C_3 = \frac{1}{2\pi f_1 R_L}$$

9) $V_0 = A_V (V_2 - V_1)$

Where, $A_V = \frac{R_2}{R_1}$

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Design steps for LF 353 BIFET op-amp :-

1) Select $R_2 = 1M\Omega$

2) WKT. $A_V = \frac{R_2}{R_1}$

$$\boxed{R_1 = \frac{R_2}{A_V}}$$

3) $R_3 = R_1$

4) $R_4 = R_2$

5) $C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)}$

6) $C_2 = \frac{1}{2\pi f_1 \left(\frac{R_3 + R_4}{10}\right)}$

7) $C_3 = \frac{1}{2\pi f_1 R_L}$

8) $A_V = \frac{R_2}{R_1}$

$V_0 = A_V V_i$

$$\boxed{V_0 = A_V (V_2 - V_1)}$$

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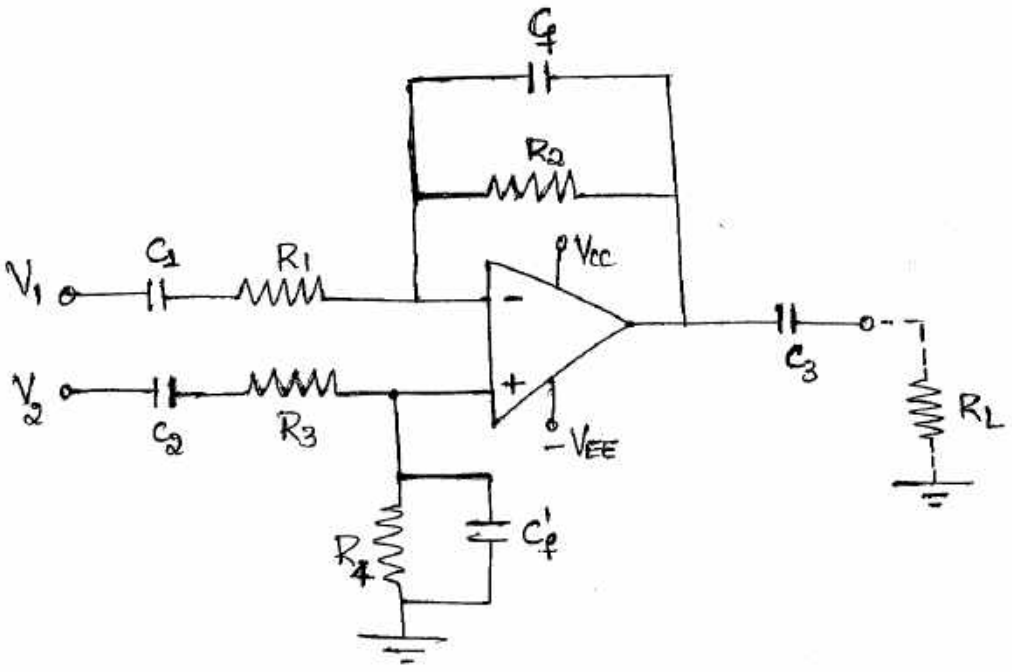
Setting upper cut-off frequency for Difference amplifier :-



Design steps :-

i) For 741 op-amp :

1) Let $I_1 = 100 \times I_{B(max)}$

2) $R_1 = \frac{V_1}{I_1}$

3) $R_3 = R_1$

4) $R_2 = \frac{V_0}{I_1}$

5) $R_4 = R_2$.

6) $C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)}$

7) $C_2 = \frac{1}{2\pi f_1 \left(\frac{R_3 + R_4}{10}\right)}$

8) $C_3 = \frac{1}{2\pi f_1 R_L}$

9) $C_f = \frac{1}{2\pi f_2 R_2}$

10) $C'_f = \frac{1}{2\pi f_2 R_4}$

11) $V_0 = A_V V_i$

where $A_V = \frac{R_2}{R_1}$ &

$V_i = (V_2 - V_1)$

$$\boxed{V_0 = \frac{R_2}{R_1}(V_2 - V_1)}$$

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ii) FOR BIFET LF 353 op-amp :-

1) select $R_2 = 1\,M\Omega$

2) $R_4 = R_2$

3) WKT $A_V = \frac{R_2}{R_1}$

$$\boxed{R_1 = \frac{R_2}{A_V}}$$

4) $R_3 = R_1$

5) $C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)}$

6) $C_2 = \frac{1}{2\pi f_1 \left(\frac{R_3 + R_4}{10}\right)}$

7) $C_3 = \frac{1}{2\pi f_1 R_L}$

8) $A_V = \frac{R_2}{R_1}$

$V_0 = A_V V_i$

$$\boxed{V_0 = A_V (V_2 - V_1)}$$

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1) A difference amplifier has following components $R_1 = R_3 = 6.8\,K\Omega$, $R_2 = R_4 = 68\,K\Omega$, $C_1 = 2.2\,\mu F$, $C_2 = 0.2\,\mu F$ & o/p capacitor $C_3 = 1\,\mu F$. Determine the ckt lower cut-off frequency and maximum differential I/p voltage that can be applied if the o/p is not to exceed 5 volts.

June - 09, 6M
June - 06, 6M

Given :- $V_o = 5V$

Sol :-

* $X_{C1} = \frac{R_1}{10}$

$$C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)}$$

$$C_1 = \frac{10}{2\pi f_1 R_1}$$

$$f_1 = \frac{10}{2\pi C_1 R_1} = \frac{10}{2\pi \times 2.2\,\mu F \times 6.8\,K\Omega}$$

$$\boxed{f_1 = 106\,Hz}$$

NOTE :-
Differential I/p
$V_d = V_i = (V_2 - V_1)$

* $A_V = \frac{R_2}{R_1} = \frac{68\,K\Omega}{6.8\,K\Omega}$

$$\boxed{A_V = 10}$$

* $A_V = \frac{V_o}{V_i} = \frac{V_o}{V_d}$

$$V_d = \frac{V_o}{A_V} = \frac{5V}{10}$$

$\boxed{V_d = 0.5V}$ ← Differential I/p voltage.

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Use of a single - polarity supply :-

Voltage follower :-

June - 08, 6M(EE)

i) capacitor coupled voltage follower using single polarity supply :-

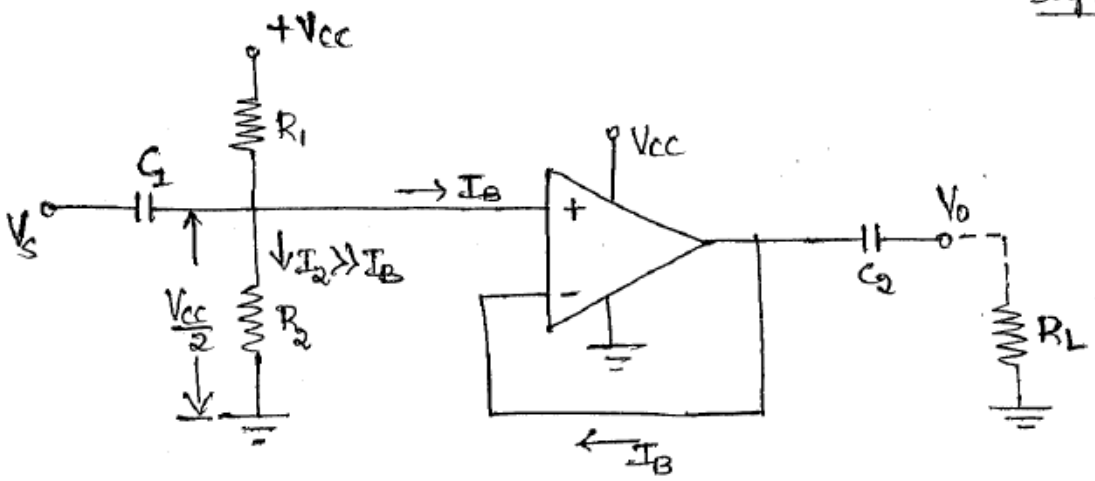

fig @ : Capacitor - coupled voltage follower using a single - polarity supply.

* The capacitors block the dc bias voltages at the I/p & the o/p. If the op-amp data sheet lists the minimum supply voltage as ±9V, then a minimum of 18V should be used in a single polarity supply.

* The potential divider R_1 & R_2 sets the bias. Voltage at the Non-INV I/p terminal as Vcc/2 i.e the dc o/p voltage & the INV input are also at $\frac{Vcc}{2}$. (∵ Voltage follower).

* I/p Impedance is $\boxed{Z_{in} = (R_1 \parallel R_2)}$

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Design steps :-

1) Let $I_1 = 100 \times I_{B(max)}$

2) $R_1 = R_2 = \frac{V_{CC}}{2I_1}$

3) $Z_{in} = (R_1 \parallel R_2)$

4) $X_{C1} = \frac{(R_1 \parallel R_2)}{10}$ at f_1 , $\boxed{C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1 \parallel R_2}{10}\right)}}$

5) $X_{C2} = R_L$ at f_1

$$\boxed{C_2 = \frac{1}{2\pi f_1 R_L}}$$

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Non - INVERTING Amplifier :-

i) Capacitor - coupled Non-INV amplifier using a single polarity supply :-

Jan-08, 8m (EE)
Jan-05, 8m (EE)
DEC-10, 4M

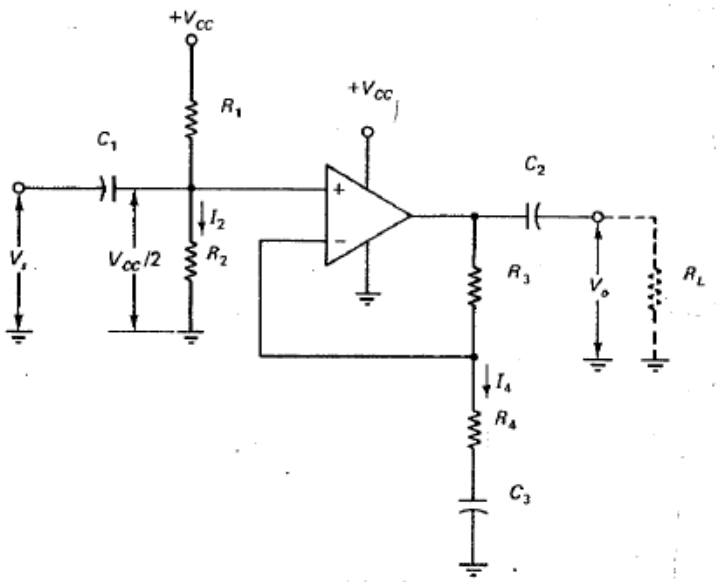

fig @ : Capacitor coupled Non-INV amplifier using a single polarity supply.

* fig shows the ckt of a capacitor-coupled Non-INV amplifier using a single-polarity supply.

Two resistors R_1 & R_2 form the voltage divider ckt setting the bias voltage at $V_{cc}/2$.

The bottom of resistor R_4 is grounded through a capacitor 'c' as shocon in fig @.

If this capacitor is not used, then the dc voltage developed across $R_4 = V_{cc}/2$ will be amplified by the gain Av, resulting in an o/p. $V_0 = A_V \times V_{cc}/2$. This large voltage saturates the o/p to a level equal to. $(V_{cc} - 1)$ Volts.

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Design steps :-

1) Let $I_2 = 100 \times I_{B(max)}$

2) Let $I_4 = 100 \times I_{B(max)}$

3) $R_1 = R_2 = \dfrac{V_{CC}/2}{I_2}$

4) WKT $A_V = \dfrac{V_o}{V_i}$

$$V_i = A_V . V_o$$

5) $R_4 = \dfrac{V_i}{I_4}$

6) $R_3 + R_4 = \dfrac{V_o}{I_4}$

Then Calculate R_3

7) $C_1 = \dfrac{1}{2\pi f_1 \left(\dfrac{R_1 \| R_2}{10}\right)}$

8) $C_2 = \dfrac{1}{2\pi f_1 \dfrac{R_L}{10}}$

9) $C_3 = \dfrac{1}{2\pi f_1 R_4}$

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(ii) High I/p Impedance capacitor coupled NON-INV amplifier using Single polarity supply:-

June -10, 6M (EE)

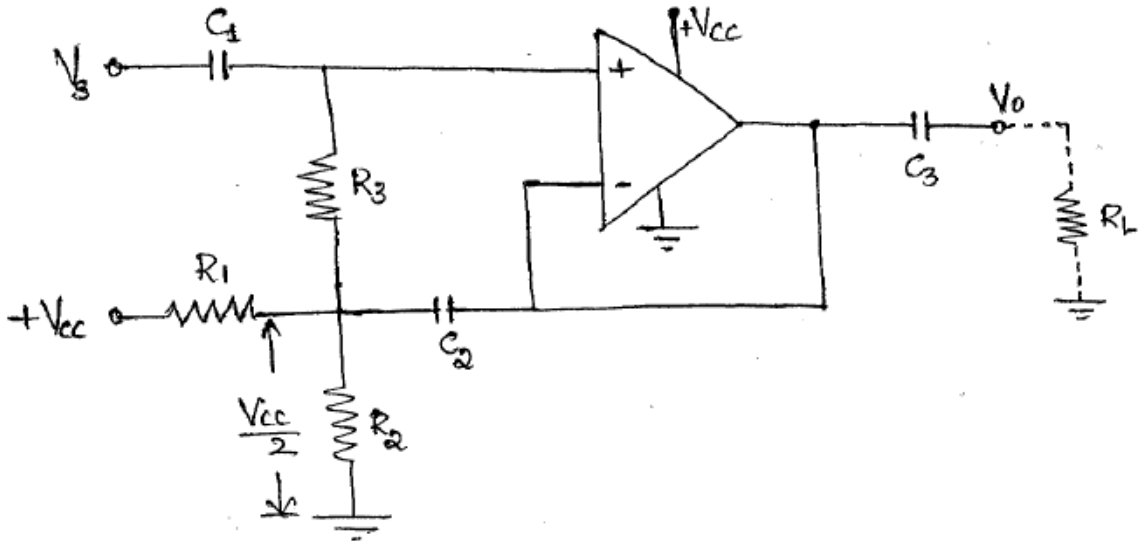

fig (b): High I/p Impedance capacitor-coupled voltage follower using a single-polarity supply

fig (b) shows a high I/p Impedance voltage follower using a single polarity supply.

* Two resistors R_1 & R_2 from the voltage divider ckt setting the bias voltage at Vcc/2.

The resistor 'R_3' is included to increase the I/p impedance by providing feedback through the capacitor. 'C_2'.

* The I/p Impedance is given by

$$Z_{in} = (1+M)R_3$$

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* $X_{C2} = \dfrac{(R_1 \parallel R_2)}{10}$ at f_1

$$C_2 = \frac{1}{2\pi f_1 \left(\frac{R_1 \parallel R_2}{10}\right)}$$

* $X_{C1} = \dfrac{R_3}{10}$ at f_1

$$C_1 = \frac{1}{2\pi f \left(\frac{R_3}{10}\right)}$$

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PROBLEM

1) A capacitor-coupled Non-INV amplifier is to have a +24 supply, a voltage gain of 100, an o/p amplitude of 5V, a lower cut-off frequency of 75Hz, and a minimum load resistance of 5.6kΩ. Using a 741 op-amp design a suitable ckt

June-05, 12M

Given :-

$V_{CC} = +24V$, $A_V = 100$, $V_0 = 5V$, $f_1 = 75Hz$, $R_L = 5.6k\Omega$

for 741 op-amp $I_{B(max)} = 500nA$

Sol :-

* Let $I_2 = 100 \times I_{B(max)} = 100 \times 500nA$

$$I_2 = 50\mu A$$

* Let $I_4 = 100 \times I_{B(max)} = 100 \times 500nA$

$$I_4 = 50\mu A$$

* $R_1 = R_2 = \frac{V_{CC}/2}{I_2} = \frac{24/12}{50\mu A} = 240k\Omega$

choose $R_1 = R_2 = 220k\Omega$

* $V_i = \frac{V_0}{A_V} = \frac{5V}{100}$

$$V_i = 50mV$$

* $R_4 = \frac{V_i}{I_4} = \frac{50mV}{50\mu A}$

$$R_4 = 1k\Omega$$

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* $R_3 + R_4 = \frac{V_o}{I_4} = \frac{5V}{50\mu A}$

$\boxed{R_3 + R_4 = 100\,K\Omega}$

$R_3 = 100\,K\Omega - R_4$

$= 100\,K\Omega - 1K\Omega$

$\boxed{R_3 = 99K\Omega}$ choose $\boxed{R_3 = 100K\Omega}$

* $C_1 = \frac{1}{2\pi f_1 \left(R_1 \| R_2 / 10 \right)} = \frac{1}{2\pi \times 75 \times \left(\frac{220K\Omega \| 220\,K\Omega}{10} \right)}$

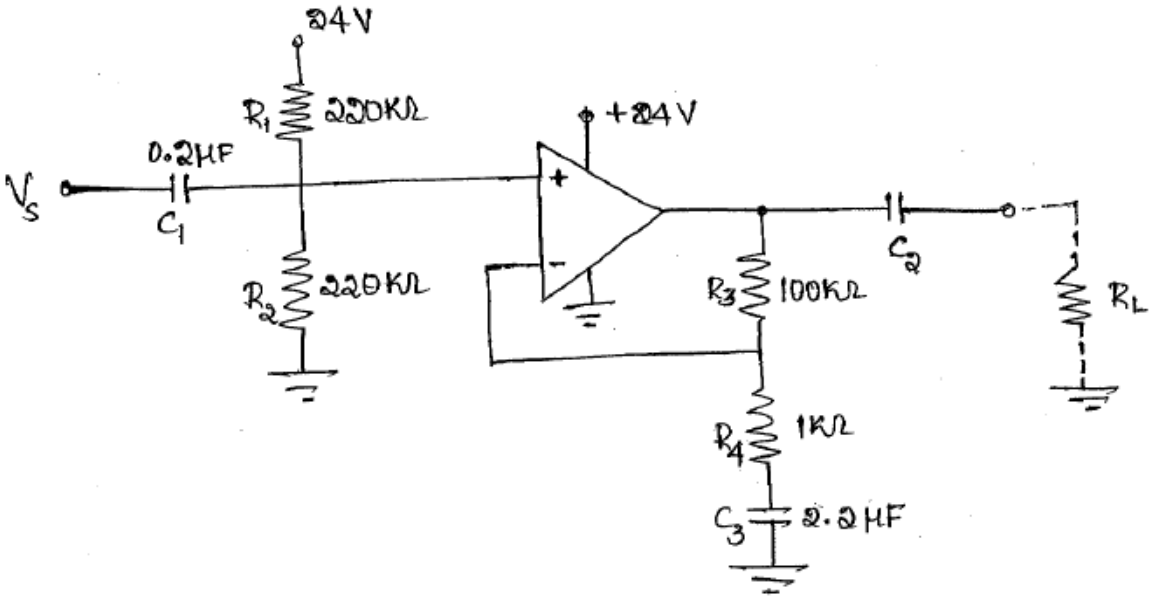
$\boxed{C_1 = 0.2\,\mu F}$

* $C_2 = \frac{1}{2\pi f_1 \left(\frac{R_L}{10} \right)} = \frac{1}{2\pi \times 75 \times \left(\frac{5.6K\Omega}{10} \right)} = 3.8\mu F$

choose $\boxed{C_2 = 3.9\mu F}$

* $C_3 = \frac{1}{2\pi f_1 R_4} = \frac{1}{2\pi \times 75 \times 1K\Omega} = 2.12\,\mu F$

choose $\boxed{C_3 = 2.2\,\mu F}$



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Capacitor - coupled INV amplifier using a single polarity supply :-

* Draw the ckt diagram of a capacitor coupled INV amplifier using a single polarity supply and briefly explain.

Jan-10, 8M | June-08, 6M

* Sketch the ckt of a capacitor coupled INV amplifier using a single polarity power supply. Briefly explain its operation.

Jan-09, 6M (EE)

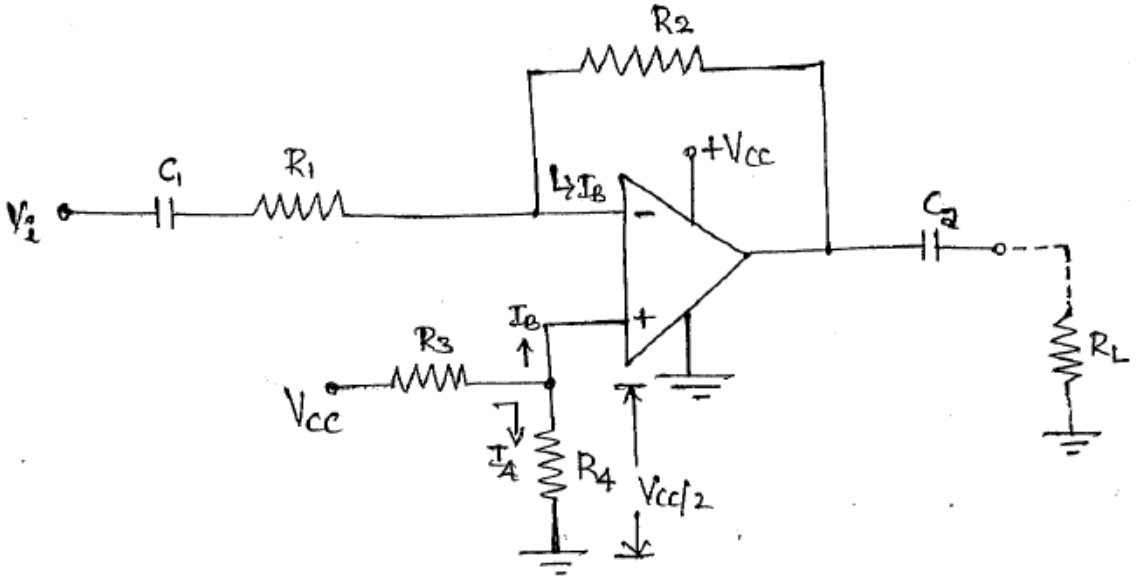

fig ①: capacitor - coupled INV - amplifier using a single -polarity supply.

fig ① shows the ckt of capacitor -coupled INV amplifier using a single polarity supply.

Two resistors R_3 & R_4 form the voltage divider ckt setting the bias voltage to $V_{cc}/2$ at the Non-INV terminal. This makes the INV I/p & o/p voltage equal to $V_{cc}/2$.

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* I/p Impedance $Z_{in} = R_1$

Design steps :-

* Let $I_1 = I_4 = 100 \times I_{B(max)}$

* $R_1 = \frac{V_i}{I_1}$

* WKT $A_V = \frac{V_o}{V_i}$

$$\boxed{V_o = A_V V_i}$$

* $R_2 = \frac{V_o}{I_1}$

* WKT $A_V = \frac{R_2}{R_1}$

$$\boxed{R_2 = A_V R_1}$$

* $R_3 = R_4 = \frac{V_{cc}/2}{I_4}$

* $C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)}$

* $C_2 = \frac{1}{2\pi f_1 R_L}$

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1) Design a capacitor-coupled INV amplifier to operate with a +20V supply. The minimum I/p signal level is 50mV, the voltage gain is to be 68, the load resistance is 500Ω, and the lower cut-off frequency is to be 200Hz. Use 741 op-amp.

June-09, 6M
Jan-09, 6M (EE)

Given:- $V_{CC} = +20V$, $V_i = 50mV$, $A_V = 68$

$R_L = 500\Omega$, $f_1 = 200Hz$

For op-amp 741 : $I_{B(max)} = 500nA$

Sol:-

* Let $I_1 = I_4 = 100 \times I_{B(max)} = 100 \times 500nA$

$$\boxed{I_1 = I_4 = 50\mu A}$$

* $R_1 = \frac{V_i}{I_1} = \frac{50mV}{50\mu A}$

$$\boxed{R_1 = 1K\Omega} \leftarrow (1m)$$

* WKT $A_V = \frac{V_o}{V_i}$

$V_o = A_V V_i = 68 \times 50mV$

$$\boxed{V_o = 3.4V}$$

* $R_2 = \frac{V_o}{I_1} = \frac{3.4V}{50\mu A}$ (OR) $R_2 = A_V \times R_1$

$= 68 \times 1K\Omega$

$$\boxed{R_2 = 68k\Omega} \leftarrow (1M)$$

$$\boxed{R_2 = 68K\Omega}$$

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* $R_3 = R_4 = \frac{V_{CC}/2}{I_4} = \frac{20/2}{50\,\mu A} = 200\,K\Omega$

choose $\boxed{R_3 = R_4 = 180\,K\Omega}$ ← (1m)

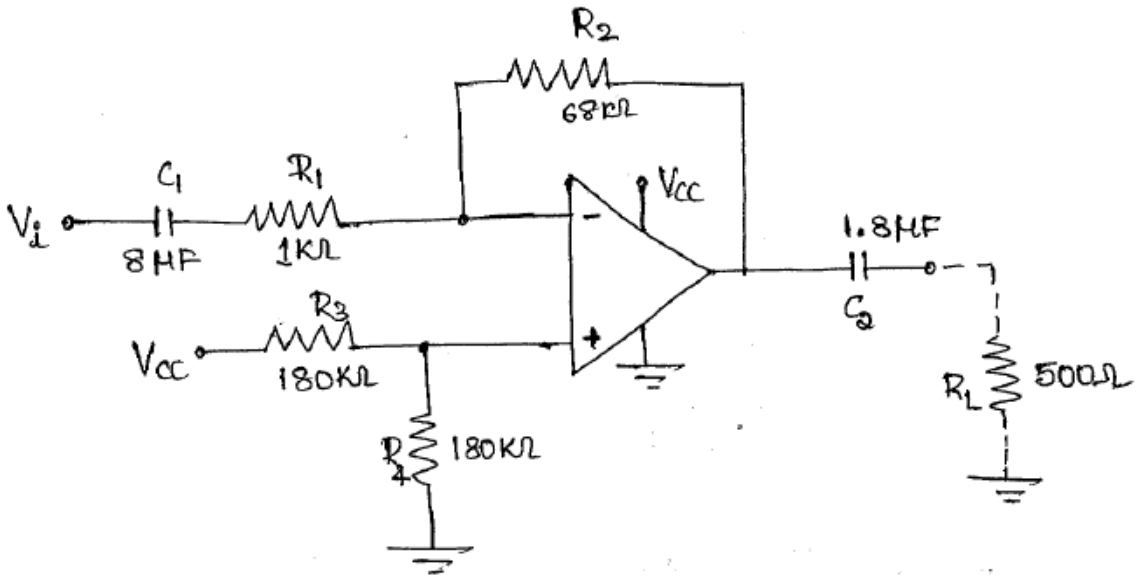
* $C_1 = \frac{1}{2\pi f_1 \left(\frac{R_L}{10}\right)}$

$= \frac{1}{2\pi \times 200 \times \left(\frac{1K\Omega}{10}\right)}$

$C_1 = 7.95\,\mu F$, choose $\boxed{C_1 = 8\,\mu F}$ ← (1m)

* $C_2 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 200 \times 500} = 1.59\,\mu F$

choose $\boxed{C_2 = 1.8\,\mu F}$ ← (1m)



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2) Design a capacitor coupled INV amplifier to operate with a single +24V supply. The minimum I/p signal level is 40mV, the voltage gain is −47, the load resistance is 680Ω & the lower 3dB frequency is 150Hz. Using a 741 op-amp for which $I_{B(max)} = 500nA$.

Given :-

$V_{CC} = 24V$, $V_i = 40mV$, $A_V = 47$, $R_L = 680\Omega$,

$f_1 = 150Hz$, $I_{B(max)} = 500nA$.

Sol :-

* Let $I_1 = I_4 = 100 \times I_{B(max)} = 100 \times 500nA$

$$\boxed{I_1 = I_4 = 50\mu A}$$

* $R_1 = \frac{V_i}{I_1} = \frac{40mV}{50\mu A} = 800\Omega$

choose $\boxed{R_1 = 820\Omega}$

* $V_o = A_V V_i = 47 \times 40mV$

$$\boxed{V_o = 1.88V}$$

* $R_2 = \frac{V_o}{I_1} = \frac{1.88V}{50\mu A} = 37.6K\Omega$ OR $R_2 = A_V R_1$.

$= 47 \times 820\Omega$

choose $\boxed{R_2 = 39K\Omega}$ $\boxed{R_2 = 38.5K\Omega}$

* $R_3 = R_4 = \frac{V_{CC}/2}{I_4} = \frac{24/2}{50\mu A} = 240K\Omega$

choose $\boxed{R_3 = R_4 = 220K\Omega}$

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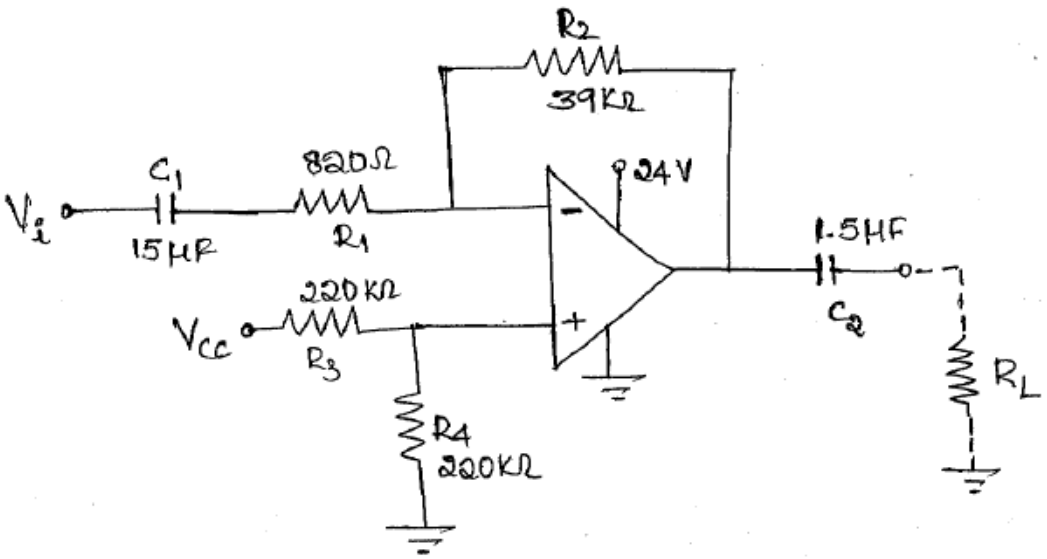
* $C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)} = \frac{1}{2\pi \times 150 \times \left(\frac{820\Omega}{10}\right)} = 12.93\,\mu F$

Choose $\boxed{C_1 = 15\,\mu F}$

* $C_2 = \frac{1}{2\pi f_1 R_L}$

$= \frac{1}{2\pi \times 150 \times 680\Omega} = 1.56\,\mu F$

Choose $\boxed{C_2 = 1.5\,\mu F}$



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* Derive the condition under which an NON-INV amplifier can be used as a voltage follower. What will be the I/p Impedance ?

Jan-09, 6M

Sol :-

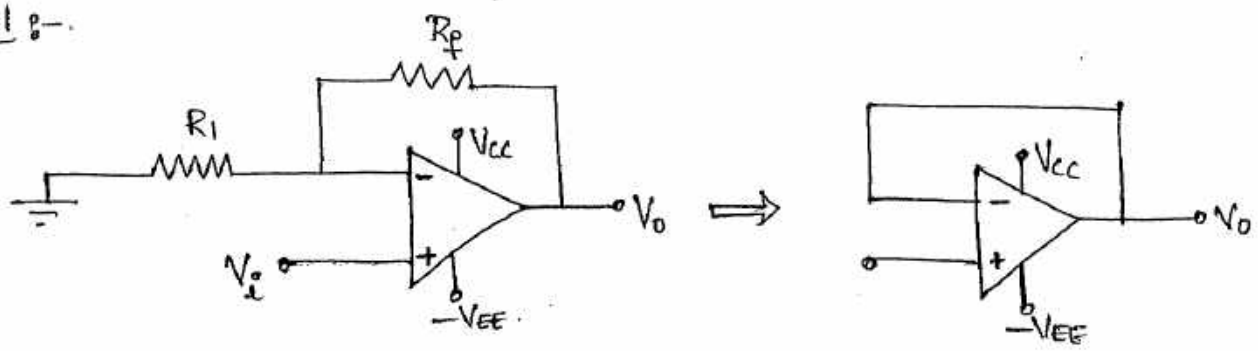

fig ① Non-INV amplifier. fig ② : Voltage follower.

Case i :-

WKT the gain of the NON-INV amplifier is given by

$$A_V = 1 + \frac{R_f}{R_1} \rightarrow ①$$

In eq ①, If $R_1 \rightarrow \infty$ & $R_f = 0$, then eq ① becomes

$$A_V = 1 + 0$$

$$\boxed{A_V = 1}$$

WKT. $A_V = \frac{V_o}{V_i}$

$\therefore A_V = \frac{V_o}{V_i} = 1$

$$\boxed{V_o = V_i}$$

Now the CKt behaves as voltage follower.

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Case ii)

WKT for NON-INV amplifier

$$A_V = \frac{V_o}{V_i} = 1 + \frac{R_f}{R_1} \quad \rightarrow (2)$$

If $R_1 \gg R_f$, then $\frac{R_f}{R_1} \ll 1$ & eq (2) becomes

$$A_V = \frac{V_o}{V_i} \approx 1$$

$$\therefore V_o \approx V_i$$

Now ckt behaves as voltage follower.

* I/P Impedance of NON-INV amp is

$$Z_{in} = (1 + M\beta) Z_i$$

The I/p Impedance of voltage follower is

$$Z_{in} = R_1$$

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Op-Amps Frequency Response and Compensation

Introduction :-

op-amp introduces phase-shift when ac signal is applied to its I/p. When frequency of ac signal increases, the phase shift introduced by op-amp also increases.

At some particular frequency the total phase shift can be upto 360°.

When the loop voltage gain "$A\beta \geq 1$" and the total phase shift from I/p to o/p through op-amp & from o/p to I/p through feedback path, approaches 360°, then the op-amp circuit becomes unstable and breaks into oscillation.

To avoid instability, compensation capacitors and resistors are used either to reduce voltage gain or to minimize the phase shift.

* The upper cut-off frequency of an op-amp ckt depends upon the particular op-amp employed (741 or LF353 etc) and upon the compensating components (R & C).

* The frequency response is also limited by the op-amp Slew rate.

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NOTE :-

Loop voltage gain :-

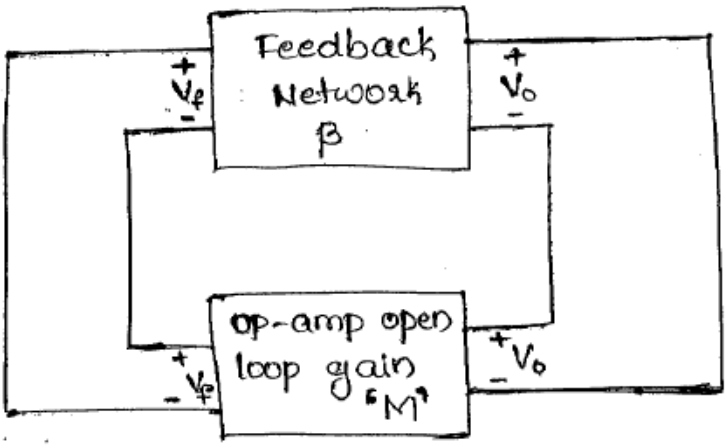
Loop voltage gain of the op-amp is defined as the product of the voltage gain 'M' & the feedback factor 'β' i.e, "Mβ".

op-amp circuit stability :-

* Discuss the op-amp ckt stability and show how feedback in an INVERTING amplifier can produce instability. Explain the conditions necessary for oscillations to occur in an op-amp ckt. Jan-10,8M

⇒

* Due to the presence of feedback network, op-amp circuits are bound to become unstable and breaks into oscillations.



$V_f = \beta V_o$

* When loop gain ie $M\beta = 1$ & total phase shift around the loop is 360°, then op-amp become unstable & break into oscillation. To prevent this, frequency compensation ckt's are used.

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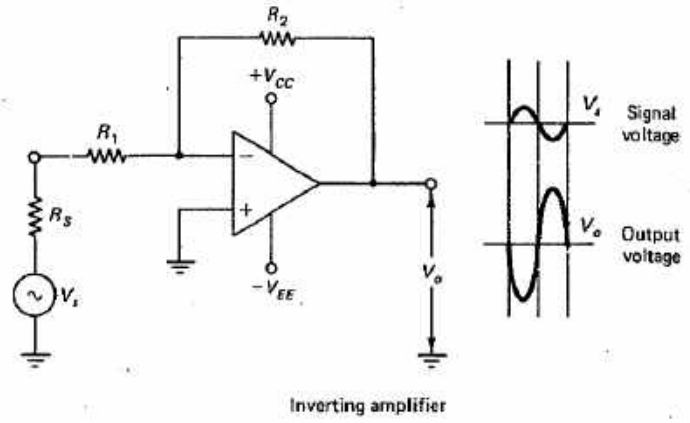
INVERTING Amplifier:-



Inverting amplifier

fig ① : INV amplifier

* In INVERTING amplifier I/p signal 'V_S' is amplified by a factor $\frac{R_2}{R_1}$ and phase shifted by 180°.

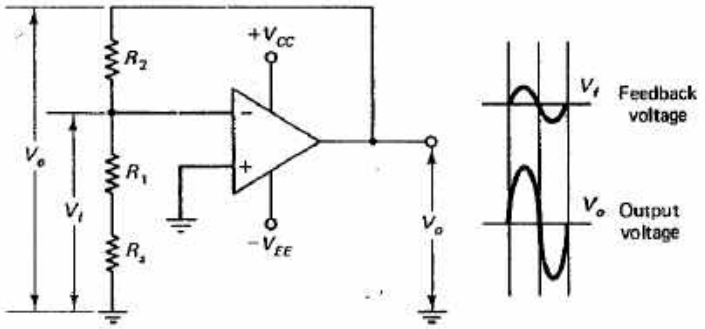


Fig ② Inverting amplifier oscillating

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* The circuit of fig ① can be redrawn with input voltage V_s grounded and is shown in fig ②.

The o/p voltage 'V_o' is divided by the feedback network to produce feedback voltage 'V_f'. This feedback voltage V_f is amplified by open loop gain M of the op-amp to produce an o/p voltage 'V_o' which inturn generates the feedback voltage 'V_f'.

∴ o/p voltage $\boxed{V_o = MV_f}$ (∵ I/p is 'V_f')

* The feedback voltage V_f is given by

$$V_f = IR_1$$

Where $I = \frac{V_o}{R_1 + R_2}$

$$V_f = \frac{R_1}{R_1 + R_2} \cdot V_o$$

$$\boxed{V_f = \beta V_o}$$

Where $\beta = \frac{R_1}{R_1 + R_2}$ & is called feedback factor.

(Neglecting signal source resistance R_s).

* If βV_o is exactly equal to V_f in both magnitude and phase, the circuit is supplying its own ac I/p and a state of continuous oscillation exists.

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* The conditions necessary for oscillations to occur in an op-amp ckt are:

1) The loop gain should be equal to or greater than one. i.e $A\beta = 1$

2) The phase shift around the loop should be equal to 360°.

The above two conditions are known as "Barkhausen Criteria."

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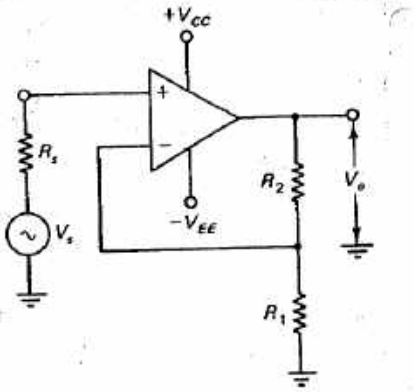
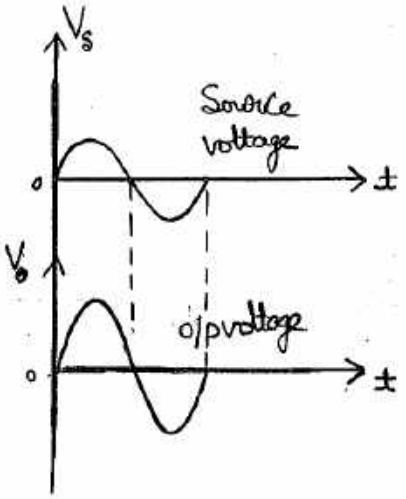
NON - INVERTING op-amp :-

* Shoco hoco feedback in an Non - INV amplifier ckt can produce instability.

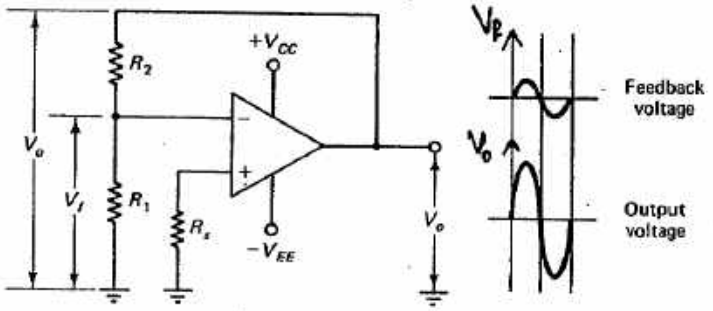
June -07, 6M(EE)



Noninverting amplifier



* In Non - INV amplifier I/p Signal 'V_s' is amplified by a factor $\left(1+\frac{R_2}{R_1}\right)$ without any phase-Shift.



Noninverting amplifier oscillating

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* The ckt of fig ① can be redrawn with I/p voltage 'V_s' grounded and is shown in fig ②.

* The o/p voltage 'V_o' is divided by the feedback network to produce feedback voltage 'V_f'. This feedback voltage V_f is amplified by open-loop gain 'M' of the op-amp to produce an o/p voltage 'V_o' which intern generates the feedback voltage 'V_f'.

∴ o/p voltage $\boxed{V_o = MV_f}$ ($\because$ I/p is 'V_f')

* The feedback voltage V_f is given by

$$V_f = IR_1$$

Where $I = \frac{V_o}{R_1 + R_2}$

$$V_f = \frac{R_1}{R_1 + R_2} V_o.$$

$$\boxed{V_f = \beta V_o}$$

Where $\beta = \frac{R_1}{R_1 + R_2}$ & is called feedback factor.

* If βV_o is exactly equal to V_f in both magnitude & phase, the circuit is supplying its own ac I/p and a state of continuous oscillation exists.

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Frequency and phase response :-

1) Frequency & phase response of single-stage amplifier.

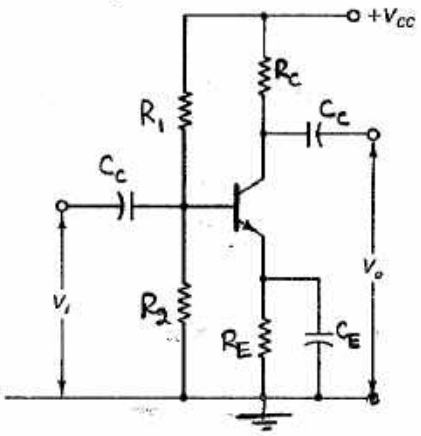

Fig 1: (a) Single-stage transistor amplifier

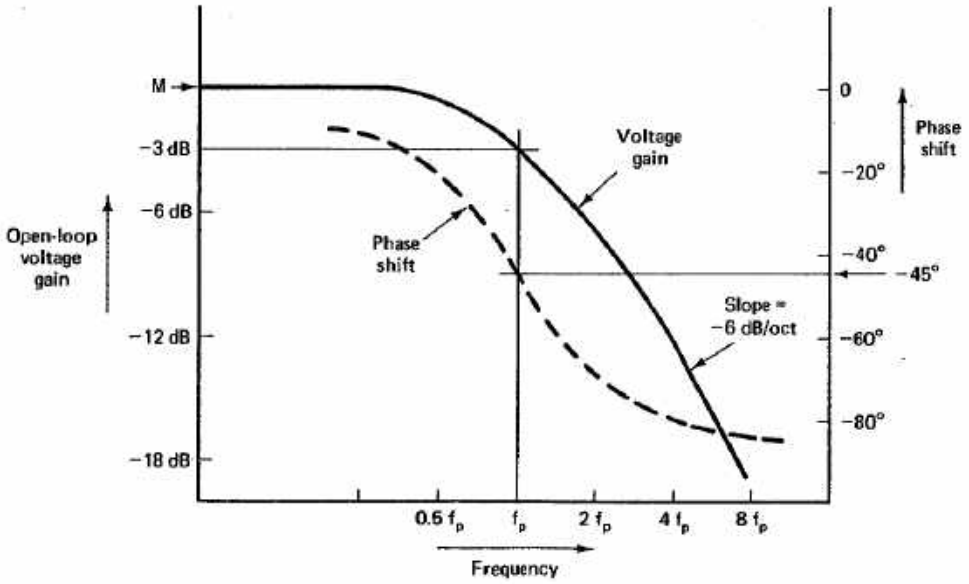

Fig 1: (b) High frequency ends of gain/frequency and phase/frequency responses

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* fig 1: (a) shows a single-stage transistor amplifier circuit while fig 1 (b) shows the high frequency ende of the gain/ frequency and phase/ frequency response of the circuit.

* The voltage gain of a single-stage amplifier starts to fall off at some high frequency. This may be due to junction capacitance of transistor and stray capacitance in the circuit.

* The frequency is plotted to a logarithmic base. The voltage gain falls off at a rate of 6dB. for each doupling of frequency (i.e -6dB per octave).

This can also be stated as -20dB/decade ie for each ten times increase in frequency.

* The pole frequency 'fp' is the frequency at which the voltage gain reduces to -3dB from the mid-band gain.

fig 1 (b) also shows the graph of phase shift versus frequency. At pole frequency 'fp' phase lag increases from 0° to -45°.

As the frequency increases, the phase lag continues to increase to a maximum of -90°.

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9) Frequency & phase response of op-amp :-

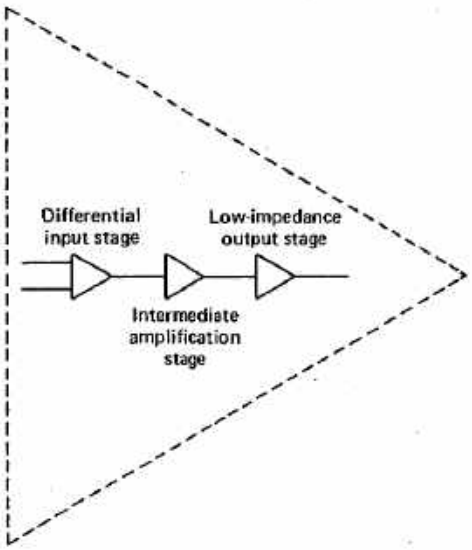

Fig 1 An operational amplifier has three stages of amplification

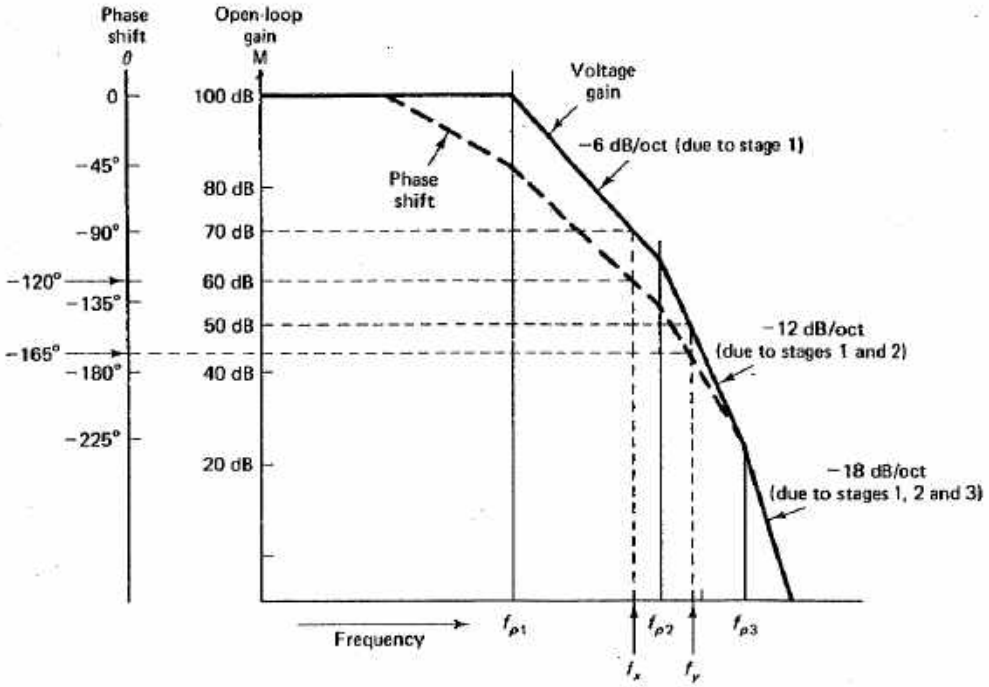

Fig 2 Straight-line approximation of op-amp open-loop gain/frequency and phase/frequency responses

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Fig ① shows the Internal block diagram of op-amp.

It has three stages of amplication.

Stage 1 :— Differential amplifier stage.
Stage 2 :— Intermediate amplification stage.
Stage 3 :— Low Impedance o/p stage.

* The f_{p1}, f_{p2} and f_{p3} are the pole frequencies of these three stages and are such that $f_{p3} > f_{p2} > f_{p1}$

A straight line approximation of the gain / frequency response graph for a typical op-amp is shown in fig ②. This graph is also known as Bode plot.

* From fig ②, we observe that the overall voltage gain 'M' decreases (falls off) at 6dB / octave or -20dB / decade - from f_{p1} when only the gain of stage 1 is decreasing.

* From f_{p2}, stage 2 gain is decreasing at 6 dB / octave, so the total fall rate is 12 dB / octave or -40dB / decade.

* Finally, when the frequency reaches f_{p3}, the gain of stage-3 is decreasing at 6dB / octave so that the overall fall off 'M' due to all 3 stages is 18 dB / octave or -60 dB / decade.

* The phase-shift of each stage also added together to give the total phase shift for the op-amp.

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* At f_{p1}, the stage-1 phase shift is $-45°$ while the phase shift from stage-2 & stage 3 is negligibly small, so the total phase shift is $-45°$.

* At f_{p2}, stage-2 adds another $-45°$.

At this point the stage-1 phase shift is at its maximum of $-90°$.

∴ The total phase shift at f_{p2} is

$\theta = -45° - 90°$ { ∵ Stage-1 → 90°, Stage-2 → −45° }

$\boxed{\theta = -135°}$

* When the frequency is f_{p3},

Stage-1 phase shift ⟶ $-90°$
Stage-2 phase shift ⟶ $-90°$
Stage-3 phase shift ⟶ $-45°$

∴ $\theta = -90° - 90° - 45°$

$\boxed{\theta = -225°}$

This open-loop phase shift is additional to the $-180°$ phase shift that normally occurs from the op-amp INV. I/p terminal to the o/p.

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Phase Margin :-

* WKT oscillations occur in an op-amp ckt when the loop gain $M\beta \geq 1$ and the loop phase shift is -360°.

In fact, the phase shift does not have to be exactly -360° for oscillation to occur.

For eg :- If $M\beta \geq 1$ & loop phase shift is -330°. makes the ckt unstable. To avoid oscillations the total loop phase shift must not be greater than -315° when $M\beta = 1$

* The difference between 360° and the actual phase shift at $M\beta = 1$ is referred to as the phase Margin.

To have stability

Minimum phase margin $= 360^\circ - 315^\circ = 45^\circ$

---

* What is the need of stability check in an op-amp From the frequency response. show how stability of an op-amp can be analyzed. When do you say an op-amp is stable ?

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High gain Amplifier stability :

OR.

stability of High gain Amplifier :-

* Explain why an op-amp with a higher closed loop gain is more likely to be stable.

⇒ WKT, the overall voltage gain of an amplifier with negative feedback is

$$A_V = \frac{1}{\beta}$$

$$\boxed{\beta = \frac{1}{A_V}} \rightarrow (1)$$

* The loop gain $= M\beta \rightarrow (2)$

substituting eq (1) in (2), we get $\boxed{M\beta = \frac{M}{A_V}}$

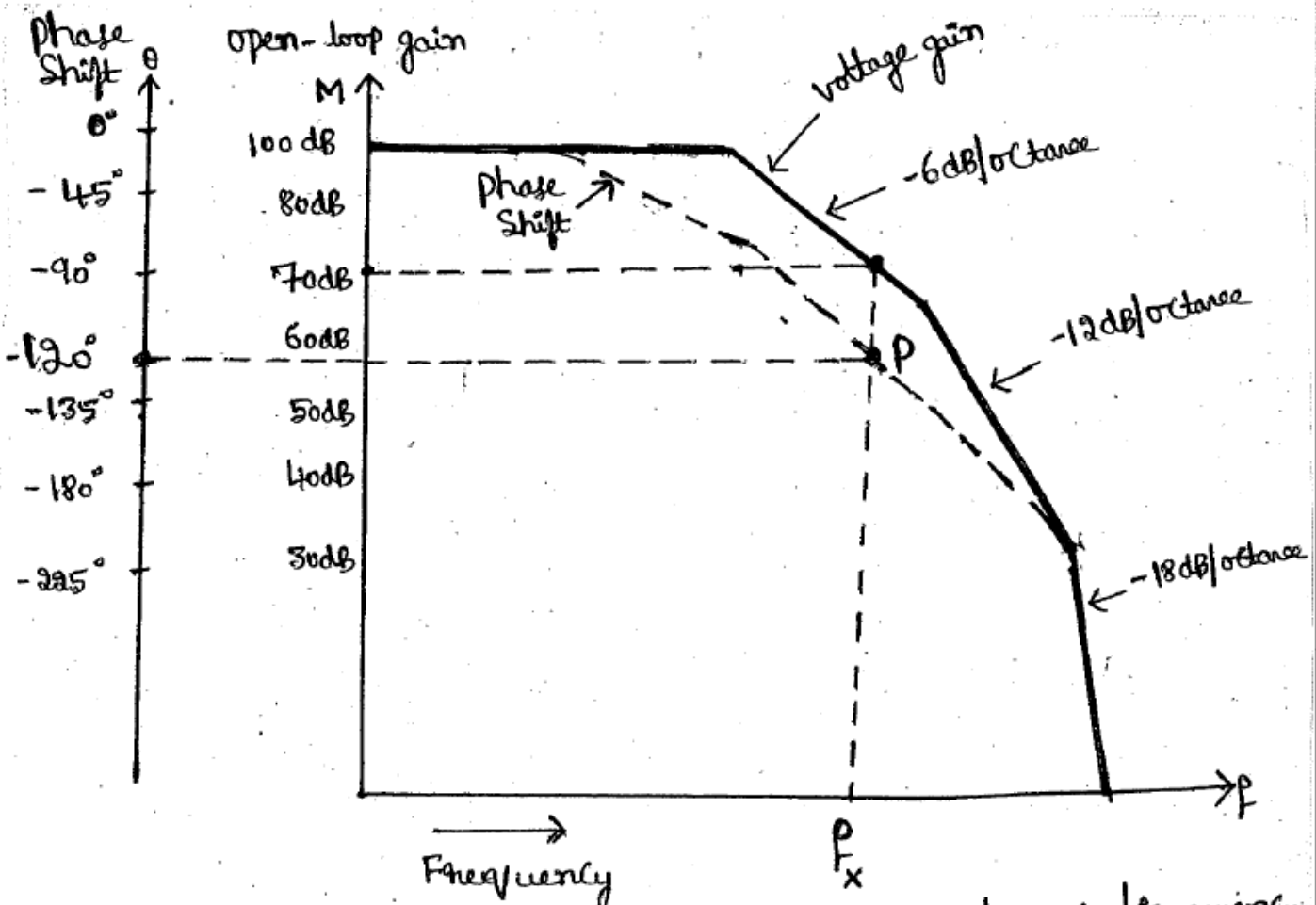

Fig (1): Straight-line approximation of op-amp open-loop gain / frequency and phase / frequency responses

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* Suppose an INVERTING op-amp with a frequency response as in fig ① is used with feedback to produce an amplifier with a closed loop gain of 70dB.

A horizontal line drawn on the frequency response graph at $A_V = 70\,dB$ intersects the open-loop gain / frequency graph at frequency f_x.

At this point $M = 70\,dB$.

$\therefore$ Loop gain $M\beta = \frac{M}{A_V} = \frac{70\,dB}{70\,dB}$

$$\boxed{M\beta = 1}$$

$\therefore$ At frequency 'f_x', the first condition of the ckt to become unstable is satisfied.

Now, let us calculate the loop phase shift at frequency 'f_x'. The vertical line at frequency f_x cuts the phase characteristics at point 'p'. A horizontal line drawn at p corresponds to -120° phase shift i.e $\boxed{\theta = -120^\circ}$

* The phase shift $\phi = -180^\circ + \theta = -180^\circ - 120^\circ$

$$\boxed{\phi = -300^\circ}$$

* The phase margin $= 360^\circ - \phi = 360^\circ - 300^\circ$

$\therefore \boxed{\text{phase margin} = 60^\circ}$

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* With $A_V = 70$ dB, at $M\beta = 1$, the phase margin is 60°.

Since the minimum phase margin for stability is 45°. ∴ The ckt is unlikely to oscillate & remains stable eventhough $M\beta = 1$.

* For frequencies lower than f_x, the loop gain '$M\beta > 1$' but the phase shift will be less than -120° and the ckt will not break into oscillations.

* For frequencies greater than f_x, the loop gain '$M\beta < 1$'. The total phase shift may be between -330° to -360°, but $M\beta < 1$. Thus the ckt will not break into oscillations at higher frequencies.

* With the help of frequency and phase response curves of a typical op-amp, discuss the concept of Circuit Stability for high gain and low gain amplifiers

Dec-10, 12M

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Stability of lower gain amplifiers :-

* Explain why an op-amp with a lower closed loop gain is more likely to be unstable.

Jan-05, 6M(EE)

⇒

* WKT, the overall voltage gain of an amplifier with negative feedback is

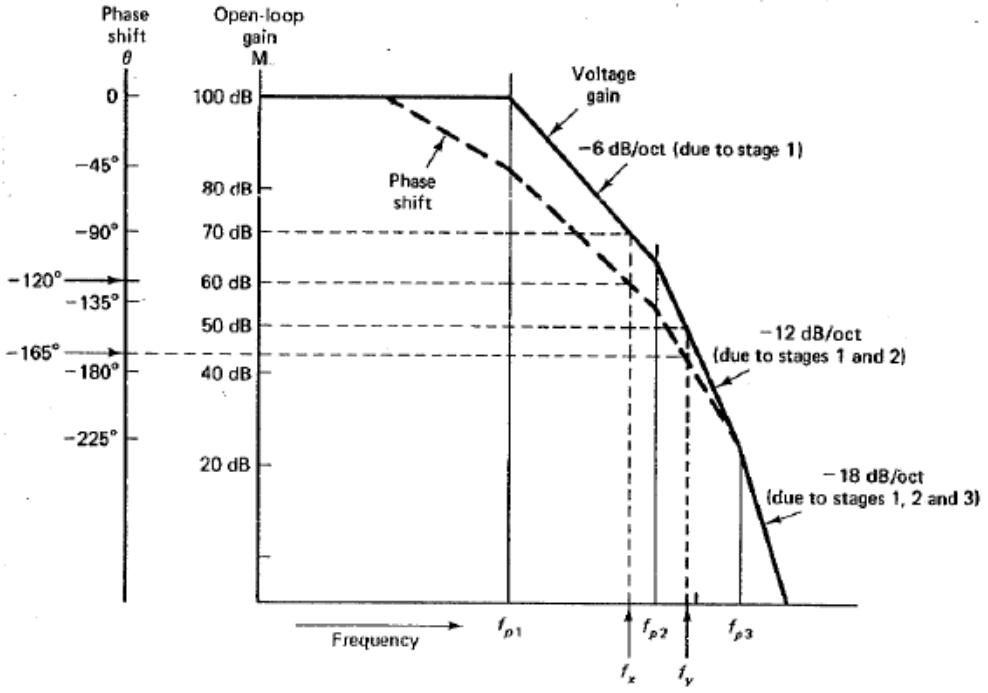
$$A_V = \frac{1}{\beta}$$

$$\boxed{\beta = \frac{1}{A_V}} \rightarrow (1)$$

* The loop gain = $M\beta \rightarrow (2)$

substituting eq (1) in eq (2) we get

$$\boxed{M\beta = \frac{M}{A_V}}$$



Straight-line approximation of op-amp open-loop gain/frequency and phase/frequency responses

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* Suppose an INVERTING op-amp with a frequency response as shown in fig ① is used with feedback to produce an amplifier with a closed loop gain of 50 dB.

* A horizontal line drawn on the frequency response graph at $A_V = 50$ dB intersects the open loop gain / freq graph at frequency f_x.

At this point $M = 50$ dB

$\therefore$ Loop gain $= M\beta = \frac{M}{A_V} = \frac{50\,dB}{50\,dB}$

$$\boxed{M\beta = 1}$$

$\therefore$ At frequency 'f_x', the first condition of the ckt to become unstable is satisfied.

* Now let us calculate the loop phase shift at frequency 'f_x'. The vertical line at frequency fx cuts the phase characteristics at point 'p'.

A horizontal line drawn at p corresponds to $-165°$ phase shift i.e. $\boxed{\theta = -165°}$

* The phase shift introduced by the INV amplifier is $-180°$.

$\therefore$ The total phase shift $\phi = -180° + \theta$

$= -180° - 165°$

$$\boxed{\phi = -345°}$$

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* The phase margin $= 360^\circ - \phi$

$= 360^\circ - 345^\circ$

$\therefore$ **phase margin $= 15^\circ$**

* With $A_V = 50$ dB, at $M\beta = 1$, the phase margin is 15° which is less than the minimum phase margin of 45°.

As both the conditions are satisfied, the ckt break into oscillations.

* With $A_V = 70$ dB, there is less feedback and the circuit is stable.

Whereas at $A_V = 50$ dB, there is more feedback and the circuit breaks into oscillations.

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Frequency Compensating Methods :-

* What is frequency compensation ? Mention different types of frequency compensation.

In order to stabilize op-amp circuit, frequency compensating networks are used.

These networks are R-C networks connected into the op-amp circuit.

The different frequency compensating networks are :-

1) phase lag compensation.
2) phase lead compensation
3) Miller effect compensation
4) Feed forward compensation.

---

* phase-Lag compensation :-

* With a neat sketch, explain the working of a lag compensation network. show how it affects the frequency response of an op-amp.

June-10, 8M | June-10, 6M(EE) | Jan-06, 6M(EE)

* Draco the ckt of a long compensation network Explain its operation & Show hoco it affects the frequency response of an op-amp. June-08, 6M

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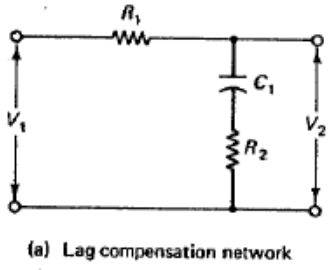
* What is frequency compensation ? Explain phase lag or phase lead compensation method.

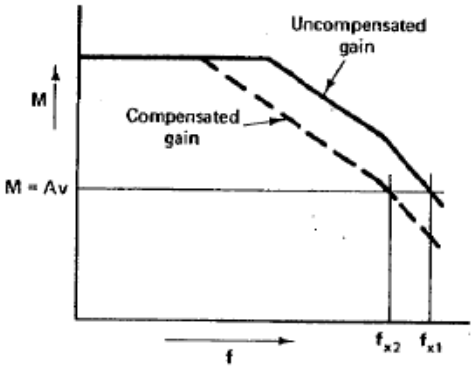
Jan -10, 8M(EE)

* Explain the frequency compensating methods, adopted to stabilize the op-amp ckt.

June -06, 6M(EE)



(a) Lag compensation network



(b) Effect of lag compensation on gain/frequency response

Fig ①

Fig 1 ⓐ shows a phase-lag compensation network consisting of two resistors and a capacitor.

* At lower frequencies, $X_{C1} \gg R_2$ then voltage V_2 lags V_1. A phase lag of $-90°$ might be introduced.

* At higher frequencies, $X_{C1} \ll R_2$ & the network becomes pure resistive network and no phase lag occurs. But at higher frequencies the phase lag network introduces only attenuation as shown in fig 1 ⓑ.

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* The components of the phase lag network (R_1, R_2 & C_1) are calculated to introduce additional phase lag at lower frequencies. At higher frequencies there is only attenuation without any additional phase lag.

* The effect of phase-lag network attenuation is to shift the frequency from f_{x1} to a lower frequency f_{x2} at which $M\beta = 1$

Since $f_{x2} < f_{x1}$, the phase shift introduced by op-amp at f_{x2} will be less than at f_{x1}. Due to this, the phase margin increases and the ckt is unlikely to break into oscillations.

Thus the phase lag network is used to attenuate the loop gain, so that $M\beta = 1$ occurs at frequency where the amplifier phase shift is too small to cause oscillations.

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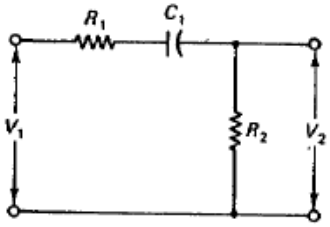
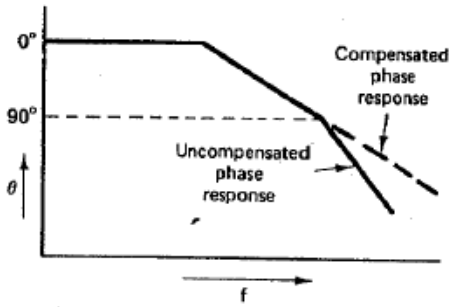
phase - lead compensation :-

* Explain the frequency compensation technique, using a phase-lead network [Dec-10, 4M]



a Lead compensation network

Fig ①



b Effect of lead compensation on phase/frequency response

* In fig 1 @, the RC network introduces a phase lead.

When $X_{C1} \gg R_1$, V_2 leads by V_1. The phase lead network is used to introduce a phase lead.

The phase lead network cancels some of the unwanted phase lag introduced by op-amp internal circuitry. This increases the phase margin at $M\beta = 1$ & improves the circuit stability.

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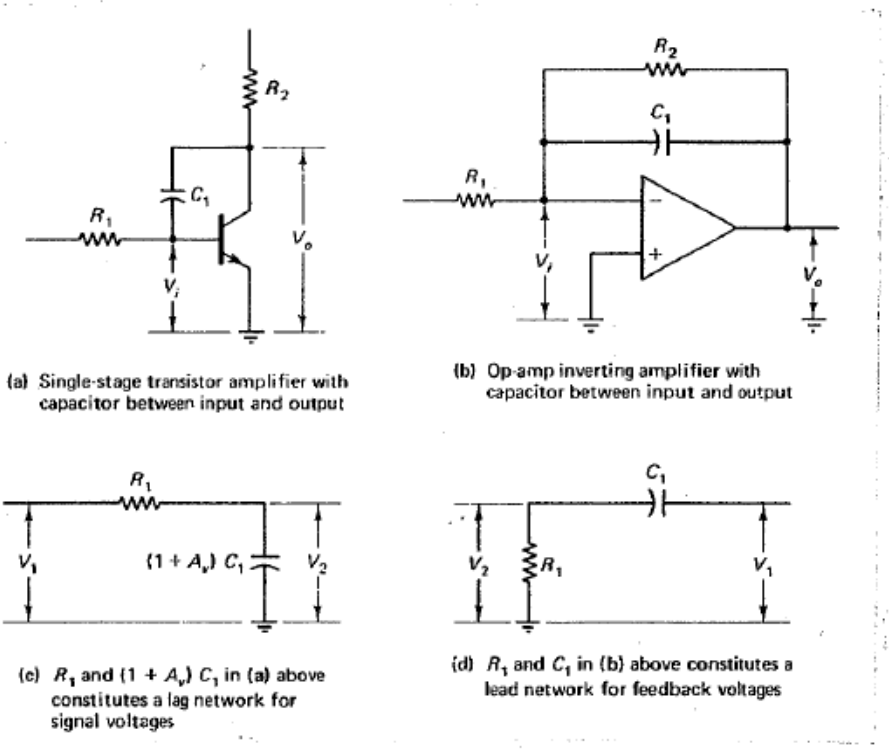
Miller - Effect compensation :-



(a) Single-stage transistor amplifier with capacitor between input and output

(b) Op-amp inverting amplifier with capacitor between input and output

(c) R_1 and $(1 + A_v)\, C_1$ in (a) above constitutes a lag network for signal voltages

(d) R_1 and C_1 in (b) above constitutes a lead network for feedback voltages

Fig ①

- consider a common-emitter transistor amplifier stage with a capacitor connected between its collector and base terminals as shown in fig ① @.

* When an I/p voltage V_i is applied, V_i is amplified and phase inversion occurs. The O/p voltage is given by

$$V_o = -A_V V_i \quad \rightarrow ①$$

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* When the base voltage goes up by V_i and the collector voltage goes down by $A_V V_i$, the voltage change across capacitor C_1 is.

$$\boxed{\Delta V_{C1} = V_i - V_o.} \rightarrow (2)$$

{ Applying KVL from V_i, V_c & V_o

$V_i - \Delta V_{C1} - V_o = 0.$

$\Delta V_{C1} = V_i - V_o$

sub eq (1) in eq (2) we get

$$\Delta V_{C1} = V_i - (-A_V V_i)$$

$$\Delta V_{C1} = V_i + A_V V_i$$

$$\boxed{\Delta V_{C1} = V_i [1 + A_V]}$$

∴ The charge supplied to the capacitor is

$$Q = C_1 \times \Delta V_{C1}$$

$$= C_1 \times V_i [1 + A_V]$$

$$\boxed{Q = C_1 [1 + A_V] V_i}$$

∴ When the base voltage increases by V_i, then at the o/p, the capacitance appears to have been amplified by an amount $(1 + A_V)$. This effect of capacitance amplification is called as "Miller effect."

* A capacitor and resistor connected in the same way as C_1 and R_1 in fig 1@ are used for the frequency compensation inside the 741 op-amp. This ckt behaves as a phase-lag network as shown in fig 1©.

* The advantage here is that the capacitance is amplified by the Miller effect, so very small capacitance is used inside the 741 op-amp.

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* In fig 1 (b) the combination of C_1 and R_1 behaves as a phase lead network within the feedback loop. Thus C_1 and R_1 introduce a phase lead to cancel some of the phase lag in the loop.

Feed Forward compensation :-

In feedforward compensation a capacitor is connected b/w the I/p & o/p terminals of the high-gain stage of the op-amp.

At high frequencies the high gain op-amp stage introduces large amount of phase shift to the I/p signal.

The capacitor connected across op-amp compensates this phase to some extent thereby reducing the large phase shift.

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Upper cut-off frequency of an op-amp :-

* Show that the upper cut-off frequency of an op-amp ckt occurs when the open-loop gain equals the closed-loop gain.

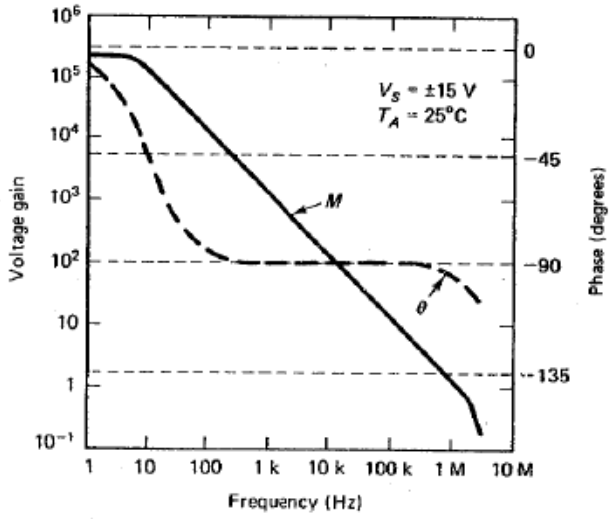

Figure 3 Open-loop gain/frequency and phase/frequency responses for a 741 operational amplifier. The phase shift remains approximately −90° for much of the frequency range.

* The upper cut-off frequency 'f_2' is the frequency at which the closed loop voltage gain falls to 3dB below the normal mid-frequency gain.

* The voltage gain of an amplifier with negative feedback is given by :

$$A_V = \frac{M}{1 + M\beta} \longrightarrow (1)$$

WKT the phase shift of the op-amp increases with increase in signal frequency.

Thus eq (1) becomes,

$$A_V \approx \frac{M\angle\theta}{1 + (M\angle\theta\,\beta)} \longrightarrow (2)$$

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from fig ① it is clear that the phase shift for the 741 remains at -90° for much of the frequency range during which the gain is falling by 20dB per decade.

Substituting -90° for θ in the eq ②

$$A_V \approx \frac{M\angle -90^\circ}{1+(M\angle -90^\circ \beta)}$$

$$A_V = \frac{-jM}{1-jM\beta}$$

$$\boxed{|A_V| = \frac{M}{\sqrt{1^2+(M\beta)^2}}} \rightarrow ③$$

When $M = A_V = \frac{1}{\beta}$, then eq ③ becomes

$$|A_V| = \frac{A_V}{\sqrt{1^2+\left(\frac{1}{\beta}\cdot\beta\right)^2}} = \frac{A_V}{\sqrt{1^2+1^2}}$$

$$|A_V| = \frac{A_V}{\sqrt{2}}$$

$$\therefore \boxed{|A_V|_{dB} = (A_V \cdot -3)\,dB}$$

∴ The upper cut-off frequency f_2 occurs at $M = A_V$.

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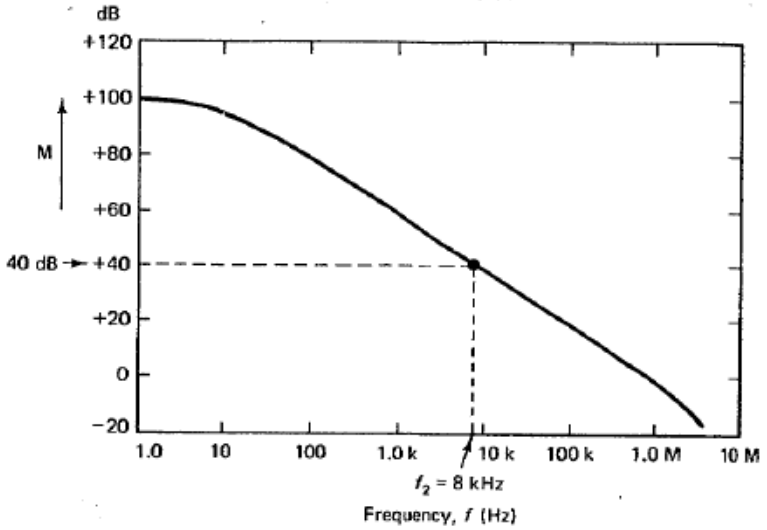
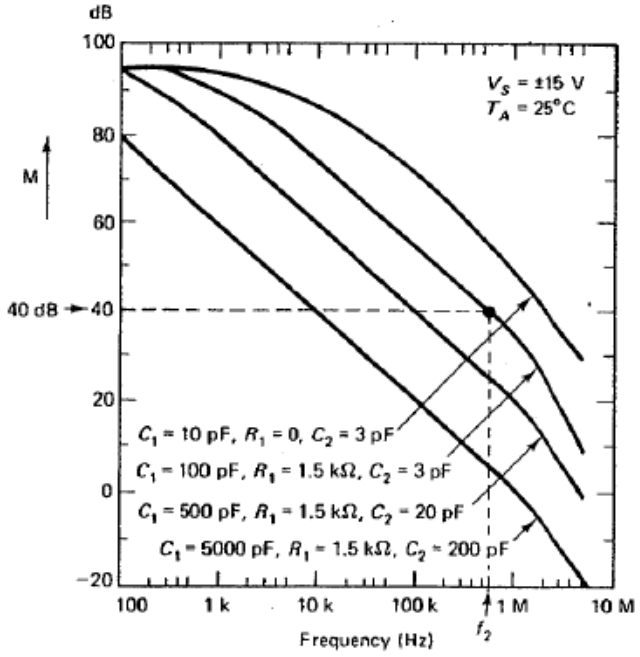
1) Determine the typical upper cut-off frequency for a NON-INV amplifier with $A_V = 100$, (a) when a 741 op-amp is used and (b) when a 709 is employed.



(a) Gain/frequency response for 741 operational amplifier



(b) Gain/frequency response for 709 operational amplifier using recommended compensation

Figure 6 Gain/frequency responses for 741 and 709 operational amplifiers. The upper cutoff frequency for any op-amp circuit is found by drawing a horizontal line at $M \approx A_o$.

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Sol :- $A_V = 100$

$$(A_V)_{dB} = 20 \log_{10}(100)$$

$$\boxed{(A_V)_{dB} = 40dB}$$

∴ Upper cut off frequency f_2 occurs at $\boxed{(A_V)_{dB} = 40\,dB}$

a) In fig ①, draw a horizontal line at M = 40dB. From the intersection of the line & the open-loop frequency response, $\boxed{f_2 \approx 8KHz}$

b) For the 709, refer to fig ②, draw a horizontal line at M = 40dB. The intersection of the M = 40dB line and the frequency response curve.

$$\boxed{f_2 = 600\,KHz}$$

Gain - Bandwidth product :- (GBW)

The gain - bandwidth product of an op-amp is the product of closed loop gain 'A_V' and the cut-off frequency for the gain.

ie. $\boxed{\text{Gain - bandwidth product} = A_V f_2}$

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* calculate the gain-bandwidth product.

i) For $A_V = 80\,dB$, $f_2 = 80\,Hz$

ii) For $A_V = 60\,dB$, $f_2 = 800\,Hz$

iii) For $A_V = 1$, $f_u = 800\,KHz$

Sol :- i) for $A_V = 80\,dB$, $f_2 = 80\,Hz$

$$(A_V)_{dB} = 20 \log_{10} (A_V)$$

$$A_V = \log_{10}^{-1} \left(\frac{80}{20}\right)$$

$$\boxed{A_V = 10000}$$

$$GBW = A_V f_2 = 10000 \times 80$$

$$\boxed{GBW = 800000}$$

ii) for $A_V = 60\,dB$, $f_2 = 800Hz$

$$A_V = \log_{10}^{-1} \left(\frac{60}{20}\right)$$

$$\boxed{A_V = 1000}$$

$$GBW = A_V f_2 = 1000 \times 800Hz$$

$$\boxed{GBW = 800000}$$

iii) for $A_V = 1$ & $f_2 = f_u = 800KHz$

$$GBW = A_V f_u = 1 \times 800 \times 10^3$$

$$\boxed{GBW = 800000}$$

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Unity - gain frequency (f_u) :-

The frequency at which $A_V = 1$ is called unit gain frequency denoted as 'f_u'.

Unity - gain bandwidth :-

$$f_u = A_V f_2$$

The gain bandwidth corresponding to f_u is also called unity gain bandwidth.

$$f_2 = \frac{f_u}{A_V}$$

* Determine the gain-bandwidth product, estimate the upper cut-off frequencies for the 741 op-amp with $A_V = 100$.

Given :- $A_V = 100$.

For 741 op-amp unity gain frequency $f_u = 800\,KHz$

i.e. $A_V = 1$ at $f_u = 800\,KHz$.

Sol : WKT $f_u = A_V f_2$

$$f_2 = \frac{f_u}{A_V} = \frac{800\,KHz}{100}$$

$$f_2 = 8\,KHz$$

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Using the gain-bandwidth product, estimate the upper cut-off frequencies for a Non-INV amplifier with $A_V = 100$ (a) When a 741 op-amp is used and.

Given :- $A_V = 100$

Sol :-

(a) For 741 op-amp : $\boxed{f_u = 800\,KHz}$

WKT $f_2 = \frac{f_u}{A_V} = \frac{800\,KHz}{100}$

$\boxed{f_2 = 8\,KHz}$

---

* Determine the upper cut off frequency for (a) a Voltage follower ckt using a 741 op-amp and (b) a unity gain INV amplifier using a 741 op-amp.

Sol :- a) In voltage follower gain $\boxed{A_V = 1}$

for 741 op-amp : $f_u = 800\,KHz$

WKT $f_u = f_2 \cdot A_V$

$f_2 = \frac{f_u}{A_V} = \frac{800\,KHz}{1}$

$\boxed{f_2 = 800\,KHz}$

(b) for unity gain INV amplifier $\boxed{R_1 = R_2}$

WKT the gain is given by

$A_V = \frac{R_1 + R_2}{R_1} = \frac{R_1 + R_1}{R_1} = \frac{2R_1}{R}$

$\boxed{A_V = 2}$

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for 741 op-amp $f_u = 800\,KHz$.

$$f_2 = \frac{f_u}{A_V} = \frac{800\,KHz}{2}$$

$$\boxed{f_2 = 400\,KHz}$$

NOTE :-

The calculation of upper cut-off frequency holds good only for small signals with o/p voltage being less than $\pm$ 1V.

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Slew Rate Effects :-

Define slew rate of an op-amp. Show how the slew rate of an op-amp can produce distortion in a sinusoidal o/p waveform. Also explain how the slew rate can limit the amplitude of the distortion free sinewave o/p for a given op-amp cut-off frequency.

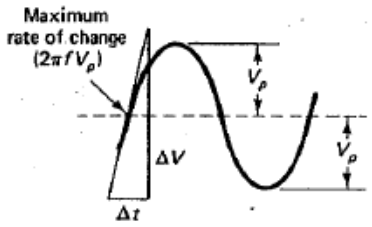
June-10, 6M (EE)

Sol :-

Slew rate : The slew rate 'S' of an op-amp is the maximum rate at which the o/p voltage can change.

i.e. $$S = \left.\frac{dV_o}{dt}\right|_{max.}$$

* For large signals, the upper cut-off frequency will be much lower than the small signal circuits. This is due to the op-amp slew rate.



(a) Sine wave maximum rate of change

P.T.O

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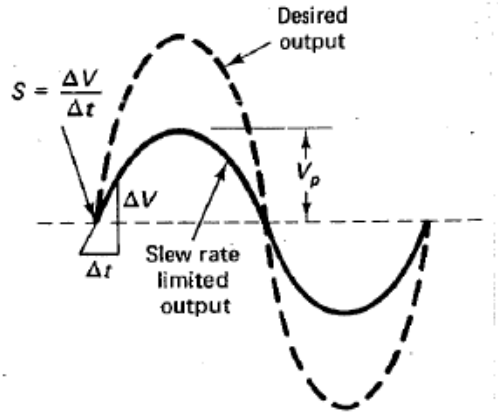
Fig 1 (b) shows a sinusoidal o/p voltage waveform from an op-amp. It is observed that the fastest rate of change of voltage occurs when the waveform crosses zero.

At this point, maximum rate of change is given by:

$$\text{Maximum rate of change} = 2\pi f V_p \text{ volts/sec}$$

Where $f \rightarrow$ frequency of the signal &
$V_p \rightarrow$ peak amplitude of the signal.



(b) Sine wave output amplitude can be limited by the op-amp slew rate

Fig 1 (b) shows the distorted waveform that occurs when the slew rate is too slow for the o/p amplitude & frequency.

* For a distortion-free o/p, the op-amp slew rate 'S' must be equal to, or greater than, the maximum rate of change of the waveform.

$$\therefore \boxed{S = 2\pi f V_p}$$

* The slew rate-limited frequency for a given o/p amplitude is.

$$\boxed{f_s = \frac{S}{2\pi V_p}}$$

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* the slew rate - limited o/p amplitude for a given cut-off frequency 'f_2' is

$$V_p = \frac{S}{2\pi f_2}$$

1) (a) calculate the slew-rate-limited cut off frequency for a voltage follower ckt using a 741 op-amp if the peak of sine wave o/p is to be 5V.

(b) Determine the maximum peak value of the sinusoidal o/p voltage that will allow the 741 voltage follower ckt to operate at the 800KHz unity gain cut off frequency.

(c) calculate the maximum peak value of sine wave o/p voltage that can be produced by the amplifier for op-amp 741 having upper cut-off frequency 8KHz.

NOTE:-
$S = 0.5\,V/\mu s$
i.e. $S = \frac{0.5\,V}{1\times10^{-6}}$.

Sol:-

(a) Given $V_p = 5V$, $f_s = ?$

for 741 op-amp: $S = 0.5\,V/\mu s$

WKT $f_s = \frac{S}{2\pi V_p} = \frac{0.5\,V/\mu s}{2\pi \times 5V} = \frac{0.5\,V}{2\pi \times 5V \times 10^{-6}}$

$f_s = 15.9KHz$

(b) $f_2 = 800KHz$, $V_p = ?$.

for 741 op-amp: $S = 0.5\,V/\mu s$

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WKT $V_p = \frac{S}{2\pi f_2} = \frac{0.5\,V/\mu s}{2\pi \times 800\,KHz} = \frac{0.5\,V}{2\pi \times 800\,KHz \times 10^{-6}}$

$\boxed{V_p = 99mV}$

(c) Given : $f_2 = 8\,KHz$

for 741 op-amp : $f_2 = 8\,KHz$ & $S = 0.5\,V/\mu s$.

WKT $V_p = \frac{S}{2\pi f_2} = \frac{0.5\,V/\mu s}{2\pi \times 8\,KHz} = \frac{0.5\,V}{2\pi \times 8KHz \times 10^{-6}}$

$\boxed{V_p = 9.9V}$

---

2) Determine

i) The slew-rate limited cut-off frequency for a voltage follower ckt using a LM 353 op-amp if the peak of sine wave o/p is to be 6.5 volts.

ii) The maximum peak value of the sinusoidal o/p voltage that will allow the LM 353-A voltage follower ciacuit to operate at the 4MHz unity-gain cutoff frequency.

iii) The maximum peak value of sinewave o/p voltage that can be produced by the amplifier having $f_2 = 250\,KHz$. Assume slew rate = $13\,V/\mu s$.

Sol:-

i) Given : $V_p = 6.5V$, $S = 13\,V/\mu s$.

WKT $f_s = \frac{S}{2\pi V_p} = \frac{13\,V}{2\pi \times 6.5 \times 10^{-6}}$

$\therefore \boxed{f_s = 318.31\,KHz}$

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ii) Given:

Unity gain cutoff frequency i.e. $f_2 = 4KHz$

WKT $V_p = \frac{S}{2\pi f_2} = \frac{13\,V}{2\pi \times 4KHz \times 10^6}$

$\therefore V_p = 0.52\,V$

iii) Given: $f_2 = 250\,KHz.$

WKT $V_p = \frac{S}{2\pi f_2} = \frac{13}{2\pi \times 250\,KHz \times 10^6}$

$\therefore V_p = 8.28$ volts.

---

3) Define the Slew rate and determine the Slew rate limited Cut-off Frequency for a 741 based voltage follower. The peak Sinewave o/p should be 10V. Given; Slew rate of 741 is 0.5 V/μsec.

Dec-10, 4M

The Slew rate 'S' of an op-amp is the maximum rate at which the o/p voltage can change.

$$S = \left.\frac{dV_o}{dt}\right|_{max} \longleftarrow (1M)$$

Given :- $S = 0.5\,V/\mu s$, $V_p = 10V.$

$$f_s = \frac{S}{2\pi V_p} = \frac{0.5\,V/\mu s}{2\pi \times 10}$$

$f_s = 7.95\,KHz$ ⟵ (3M)

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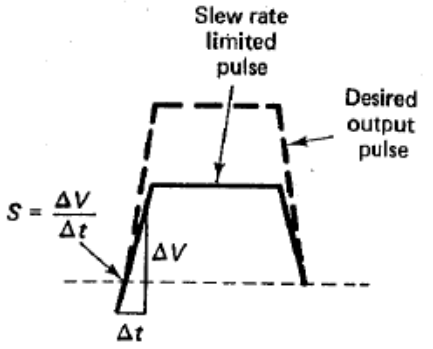
Slew rate effect on o/p pulse Rise time & amplitude :-



A pulse output waveform can be limited by the op-amp slew rate

cut-off frequency limited rise time :-

When a pulse-type signal is to be amplified the o/p rise time is related to the circuit cut-off frequency. The equation for cut-off frequency limited rise time is

$$t_{r(f_2)} = \frac{0.35}{f_2}$$

Slew rate limited rise time :

When a pulse waveform is distorted by the op-amp slew rate, the o/p rise time and the amplitude are directly related to the slew rate & is given by :

$$t_{r(s)} = \frac{V_p}{s}$$

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* (a) calculate the cut-off frequency - limited, rise time for a voltage follower ckt using a 741 op-amp. Also determine the slew rate - limited rise time if the o/p amplitude is to be 5V.

(b) Determine the maximum undistorted pulse o/p amplitude for the 741 voltage follower if the o/p rise time is not to exceed 1μs

(c) calculate the minimum o/p rise time & the maximum pulse amplitude at that rise time for a 741 amplifier with an upper cutoff frequency of 100 KHz.

Sol:-

a) For 741 op-amp : i) Upper cut-off frequency $f_2 = 800\,KHz$

ii) $S = 0.5\,\mu s/V$.

Given : $V_p = 5V$, $t_r(f_2) = ?$, $t_r(S) = ?$

WKT $t_r(f_2) = \frac{0.35}{f_2} = \frac{0.35}{800\,KHz}$

$$t_r(f_2) = 0.4\,\mu s$$

$$t_r(S) = \frac{V_p}{S} = \frac{5V}{0.5V/\mu s}$$

$$t_r(S) = 10\,\mu s$$

b) Given : $V_p = ?$, $t_r(S) = 1\,\mu s$, $S = 0.5\,V/\mu s$.

$$V_p = t_r(S) \cdot S = 1\,\mu s \times 0.5\,V/\mu s$$

$$V_p = 0.5V$$

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© Given : $f_2 = 100\,KHz$

WKT $t_r(f_2) = \frac{0.35}{f_2} = \frac{0.35}{100\,KHz}$

$$\boxed{t_r(f_2) = 3.5\,\mu s}$$

WKT. $V_p = t_{r(S)} \cdot S = 3.5\,\mu s \times 0.5\,V/\mu s$

$$\boxed{V_p = 1.75\,V}$$

* calculate the cut-off frequency limited rise time for a voltage follower ckt using a 741 op-amp. Also determine the slew rate limited rise time if the o/p amplitude is 4V.

Given : For 741 op-amp : $f_2 = 800\,KHz$, $S = 0.5\,V/\mu s$

$V_p = 4V$.

* cut off frequency limited rise time

$$t_r(f_2) = \frac{0.35}{f_2} = \frac{0.35}{800\,KHz}$$

$$\boxed{t_r(f_2) = 0.4\,\mu s}$$

* slew rate limited rise time.

$$t_{r(S)} = \frac{V_p}{S} = \frac{4}{0.5V/\mu s}$$

$$\boxed{t_{r(S)} = 8\,\mu s}$$

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* Calculate the slew rate - limited cut off frequency for a voltage follower ckt using a 741 op-amp, if the peak of sinewave o/p is to be 6V. Determine the maximum peak value of the sinusoidal o/p voltage that will allow the 741 voltage follower circuit to operate at 800KHz. Unity gain cut-off frequency.

Given: $S = 0.5\ V/\mu s$

June - 09, 4M

* Slew rate - limited cut-off frequency :-

$$WKT \quad f_s = \frac{S}{2\pi V_p} = \frac{0.5\ V/\mu s}{2\pi \times 6V} = \frac{0.5\ V}{2\pi \times 6V \times 10^{-6}}$$

$$\boxed{f_s = 13.26\ KHz} \leftarrow (2M)$$

* Maximum peak value :-

$$V_p = \frac{S}{2\pi f_2} = \frac{0.5\ V/\mu s}{2\pi \times 800KHz} = \frac{0.5\ V}{2\pi \times 800KHz \times 10^{6}}$$

$$\boxed{V_p = 99mV} \leftarrow (2M)$$

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* Determine the upper cut off frequency & the maximum distortion - free o/p amplitude for a voltage follower :

i) When a 741 op-amp is used and

ii) When an LF 353 op-amp is used.

For 741 : $f_2 = 800\ KHz$, $S = 0.5\ V/\mu s$.

For LF353 : $f_2 = 5MHz$, $S = 13\ V/\mu s$.

June -08, 6M

Sol :-

For 741 op-amp :

* $t_r(f_2) = \frac{0.35}{f_2} = \frac{0.35}{800\ KHz}$

$t_r(f_2) = 0.44\ \mu sec$ ← 1½ M

* $V_p = t_r(f_2) \times S = 0.44\ \mu sec \times 0.5\ V/\mu sec$

$V_p = 220\ mV$ ← 1½ M

* For LF353 op-amp :

* $t_r(f_2) = \frac{0.35}{f_2} = \frac{0.35}{5MHz}$

$t_r(f_2) = 70\ ns$ ← 1½ M

* $V_p = t_r(f_2) \times S = 70\ ns \times 13\ V/\mu sec.$

$= 70 \times 10^{-9} \times \frac{13\ V}{10^{-6}}$

$V_p = 910\ mV$ ← 1½ M

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* An op-amp has a unity cross-over frequency of 1MHz. calculate the upper cut off frequency in the following cases :-

i) INV amplifier with $A_{VC} = 100$ dB.

ii) Non-INV amplifier with $A_{VC} = 50$ dB

iii) Voltage follower :

show these on the frequency response plot if $A_V = 120$ dB.

Jan-09, 4M

Given : $f_u = 1$MHz

Sol :-

i) INV amplifier : $A_{VC} = 100$ dB

$$(A_{VC})_{dB} = 20 \log_{10} (A_{VC})$$

$$A_{VC} = \log^{-1}_{10} \left(\frac{100\,dB}{20} \right)$$

$$\boxed{A_{VC} = 100000.}$$

WKT $$f_2 = \frac{f_u}{A_{VC}} = \frac{1\,MHz}{100000.}$$

$$\boxed{f_2 = 10Hz} \leftarrow (1M)$$

ii) Non-INV amplifier : $A_{VC} = 50$ dB.

$$A_{VC} = \log^{-1}_{10} \left(\frac{50\,dB}{20} \right)$$

$$\boxed{A_{VC} = 316.227}$$

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WKT $f_2 = \frac{f_u}{A_V} = \frac{1MHz}{316.22}$

$\boxed{f_2 = 3.162\ KHz}$ ← (1M)

ii) Voltage follower :-

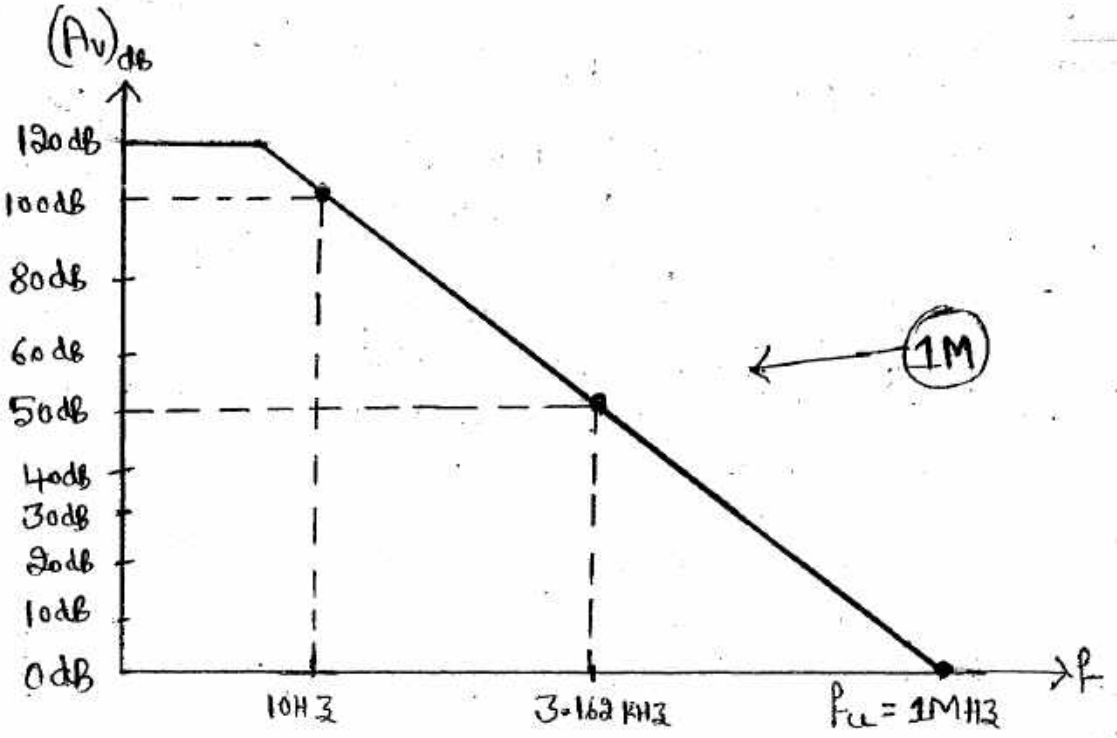
For voltage follower $A_V = 1$

$(A_V)_{dB} = 20 \log_{10}(1)$

$\boxed{(A_V)_{dB} = 0}$

WKT $f_2 = \frac{f_u}{A_V} = \frac{1MHz}{1}$

$\boxed{f_2 = 1MHz}$ ← (1M)



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* i) calculate the slew rate limited cut off frequency for a voltage follower circuit using a 741 op-amp if the peak of sinewave o/p is to be 5V.

← Model paper – 1, 4M

ii) Determine the maximum peak value of the sinusoidal o/p voltage that will allow the 741 voltage follower ckt to operate at 800 KHz. unity gain cutoff frequency.

Model-paper – II, 6M

Given :- $V_p = 5V$

i) For 741 op-amp : $S = 0.5\ V/\mu s$, $f_2 = 800\ KHz$

* WKT $t_r(f_2) = \frac{0.35}{f_2} = \frac{0.35}{800\ KHz}$

$$t_r(f_2) = 0.4375\ \mu sec$$

* $t_r(S) = \frac{V_p}{S} = \frac{5V}{0.5V/\mu s}$

$$t_r(S) = 10\ \mu s$$

ii) $f_2 = 800\ KHz$.

$$t_r(f_2) = \frac{0.35}{f_2} = \frac{0.35}{800\ KHz}$$

$$t_r(f_2) = 0.4375\ \mu sec$$

$$V_p = t_r(S) \times S = t_r(f_2) \times S = 0.4375\ \mu sec \times \frac{0.5V}{\mu sec}$$

$$V_p = 0.218V$$

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* Determine

i) the slew rate limited cutoff frequency for a voltage follower ckt using a LM353A op-amp if the peak of sine wave o/p is to be 6.5 volts.

ii) the maximum peak value of the sinusoidal o/p voltage that will allow the LM353-A voltage follower ckt to operate at the 4MHz Unity-gain cutoff freq.

iii) the maximum peak value of sine wave o/p voltage that can be produced by the amplifier having $f_2 = 250KHz$. Assume slew rate = 13V/μs.

Sol:-

i) Given: $S = 13V/\mu s$, $V_p = 6.5V$, $f_s = ?$

$$f_s = \frac{S}{2\pi V_p} = \frac{13V/\mu s}{2\pi \times 6.5V} = \frac{13V}{2\pi \times 6.5V \times 10^{-6}}$$

$$\boxed{f_s = 318.31KHz}$$

ii) Given: $S = 13V/\mu s$, unity gain frequency. $f_2 = 4MHz$

$$V_p = \frac{S}{2\pi f_2} = \frac{13V/\mu s}{2\pi \times 4 \times 10^6} = \frac{13V}{2\pi \times 4 \times 10^6 \times 10^{-6}}.$$

$$\boxed{V_p = 0.52V}$$

iii) Given: $f_2 = 250KHz$, $S = 13V/\mu s$.

$$V_p = \frac{S}{2\pi f_2} = \frac{13V/\mu s}{2\pi \times 250KHz} = \frac{13V}{2\pi \times 250KHz \times 10^{-6}}.$$

$$\boxed{V_p = 8.28 \text{ volts}}$$

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* calculate :

i) the cutoff frequency limited rise time for a voltage follower using LM 353A op-amp. Also find the slew rate - limited rise time if the o/p Amplitude. is to be 6.5 volts.

ii) the maximum undistorted pulse o/p amplitude for LM 353A voltage follower if the o/p rise time is not to exceed 0.8 μsec.

iii) the minimum o/p rise time & the maximum pulse amplitude at that rise time for a LM 353A amplifier with an upper cutoff frequency of 400 KHz.

[Assume $f_u = 4MHz$ and $S = 13V/\mu sec$ for LM 353A op-amp].

Given:

i) $V_p = 6.5V$, $f_u = 4MHz$, $S = 13V/\mu s$.

$$t_r(f_2) = \frac{0.35}{f_2} = \frac{0.35}{4\times10^6} = 87.5 nsec$$

$$\boxed{t_r(f_2) = 87.5 nsec}$$

$$t_r(S) = \frac{V_p}{S} = \frac{6.5V}{13V/\mu s}$$

$$\boxed{t_r(S) = 0.5 \mu s}$$

ii) $$V_p = t_{r(S)} \cdot S = (0.8\times10^{-6})(13V/\mu s) = \frac{0.8\times10^{-6}\times13V}{10^{-6}}$$

$$\boxed{V_p = 10.4V}$$

iii) Given :- $f_2 = 400 KHz$.

$$t_{r(f_2)} = \frac{0.35}{f_2} = \frac{0.35}{400\times10^3}$$

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$$t_{r(f_2)} = 0.875\,\mu s$$

$$V_p = t_{r(f_2)} \cdot S = 0.875\,\mu s \times 13V/\mu s$$

$$= 0.875\,\mu s \times \frac{13V}{10^{-6}}$$

$$V_p = 11.375 \text{ volts}$$

---

* calculate the minimum rise time and maximum undistorted o/p pulse amplitude at that rise time for an amplifier with closed loop gain 50, using a 741 op-amp. Jan-08, 4M(EE) Jan-05, 6M(EE)

Given: $A_V = 50$.

for 741 op-amp: $f_u = 800\,KHz$.

Sol: $f_2 = \frac{f_u}{A_V} = \frac{800KHz}{50}$

$$f_2 = 16\,KHz$$

* $t_{r(f_2)} = \frac{0.35}{f_2} = \frac{0.35}{16\,KHz}$.

$$t_{r(f_2)} = 21.875\,\mu sec$$

* $V_p = S \times t_{r(f_2)} = \frac{0.5V}{\mu s} \times 21.875\,\mu sec$

$$V_p = 10.9375\,V$$

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* calculate the slew rate limited cut off frequency for a voltage follower ckt using 741 op-amp. The peak value of the sinewave o/p is to be 5V. The slew rate of op-amp is 0.5V/μs. Determine the maximum peak value of the sinusoidal o/p voltage that will allow the voltage follower ckt to operate at 500kHz unity gain cutoff frequency.

June-07, 6M(EE)

Given :- $S = 0.5\,V/\mu s$, $V_p = 5V$.

i) $t_r(S) = \frac{V_p}{S} = \frac{5V}{0.5\,V/\mu s}$

$\boxed{t_r(S) = 10\,\mu s.}$

ii) $f_2 = 500\,kHz$.

$t_r(f_2) = \frac{0.35}{f_2} = \frac{0.35}{500\,kHz}$

$\boxed{t_r(f_2) = 0.7\,\mu sec}$

* $V_p = t_r(f_2)\, S = 0.7\,\mu sec \times 0.5V/\mu sec$.

$\boxed{V_p = 0.35V}$

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* A 741 with a slew rate of 0.5 V/μs is used as a voltage follower.

i) Calculate the slew rate limited cutoff frequency if the sine wave o/p is 5 volts.

ii). If this ckt is to operate with a unity gain cutoff frequency of 800 KHz, calculate the maximum peak value of the sinusoidal o/p voltage.

iii). If the upper cutoff frequency is 8 KHz, calculate the maximum value of the peak o/p voltage.

June-06, 6M (EE)

Sol:-

i) Given: $S = 0.5\,V/\mu s$, $V_p = 5\,V$

$$f_s = \frac{S}{2\pi V_p} = \frac{0.5\,V/\mu s}{2\pi \times 5\,V} = \frac{0.5\,V}{2\pi \times 5 \times 10^{-6}}$$

$$\boxed{f_s = 15.915\,KHz}$$

ii) $f_2 = f_s = 800\,KHz.$

$$V_p = \frac{S}{2\pi f_s} = \frac{0.5\,V/\mu s}{2\pi \times 800\,KHz} = \frac{0.5\,V}{2\pi \times 800KHz \times 10^{-6}}$$

$$\boxed{V_p = 99.47\,mV.}$$

iii) $f_2 = f_s = 8\,KHz.$

$$V_p = \frac{S}{2\pi f_s} = \frac{0.5\,V/\mu s}{2\pi \times 8\,KHz.} = \frac{0.5\,V}{2\pi \times 8\,KHz \times 10^{-6}}$$

$$\boxed{V_p = 9.947\,V}$$

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* Determine the upper cut-off frequency for
i) a voltage follower using a 741 op-amp and
ii) a unity gain inverting amplifier using a 741 op-amp unity gain frequency for 741 op-amp is 800 KHz.

Sol: Given: $f_u = 800\,KHz$

i) For voltage follower $\boxed{A_V = 1}$

$$f_2 = \frac{f_u}{A_V} = \frac{800\,KHz}{1}$$

$$\boxed{f_2 = 800\,KHz}$$

ii) For Non-INV amplifier gain $A_V = 1 + \frac{R_2}{R_1}$

For unity gain INV amplifier $R_1 = R_2$

$$A_V = 1 + \frac{R_1}{R_1}$$

$$\boxed{A_V = 2}$$

$$f_2 = \frac{f_u}{A_V} = \frac{800\,KHz}{2}$$

$$\boxed{f_2 = 400\,KHz}$$

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* A square wave of amplitude 500 mV is to be amplified to 3V amplitude (both peak to peak). The specified rise time should be 4 μsec or less. Can 741 be used?

[Given SR for 741 = 0.5 V / μsec]

Given:- $S = 0.5\ V/\mu sec$, $V_i = 500\ mV$, $V_{p(p-p)} = 3V$

$t_r = 4\ \mu sec.$

Sol: peak o/p $V_p = \frac{3V}{2}$

$$\boxed{V_p = 1.5V}$$

Slew rate: $S = \frac{\Delta V_o}{t} = \frac{1.5V - (-1.5V)}{4\ \mu sec}$

$$\boxed{S = 0.7\ V/\mu s}$$

The op-amp 741 has slew rate of 0.5 V / μs

* For the given parameter: $S = 0.75\ V/\mu sec.$

Hence 741 cannot be used.

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* Determine the upper cutoff frequency and maximum distortion free o/p amplitude for a voltage follower when a 741 op-amp is used. June-10, 4M

Given:

For 741 op-amp: $f_2 = 800\,kHz$ & $S = 0.5V/\mu s$.

for voltage follower: $A_V = 1$

Sol:-

* $t_r(f_2) = \frac{0.35}{f_2} = \frac{0.35}{800\,kHz}$

$t_r(f_2) = 0.44\,\mu sec$ ← (2M)

* $V_p = t_r(f_2) \times S = 0.44\,\mu s \times 0.5V/\mu s$

$V_p = 220\,mV$ ← (2M)

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Z_{in}. MOD compensation :-

* Sketch and explain a circuit to show the Z_{in} mod method of frequency compensation. state the application of the circuit. | Jan-10, 8M |

* With a neat circuit diagram, explain Z_{in} mod method of frequency compensation. Write the equation for the feedback factor | Jan-09, 6M(EE) | June-09, 8M |

* Explain how bandwidth increase by using Z_{in} mod compensation. | Jan-09, 8M |

In order to increase the bandwidth of an op-amp ckt, input impedance. modification 'Z_{in} MOD' technique of frequency compensation is used.

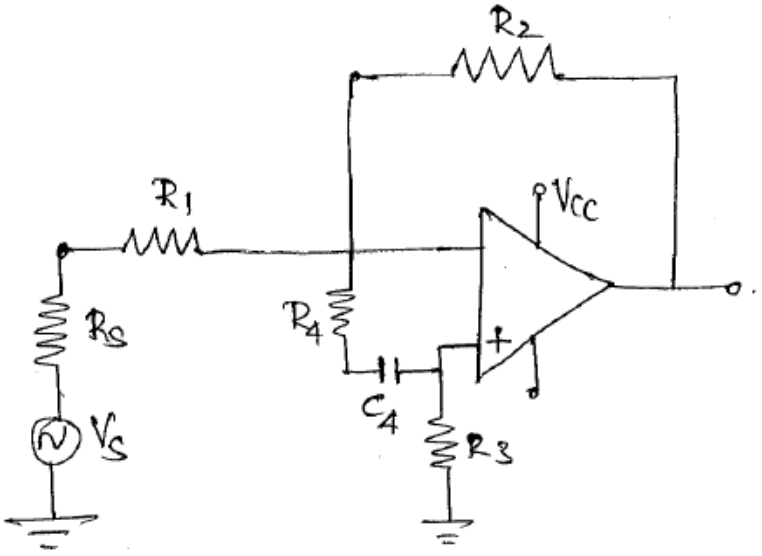

fig (a) : R_4 & C_4 are used at the op-amp I/p to alter the ckt loop gain.

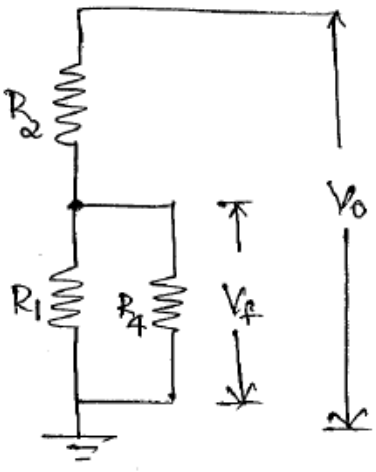

fig (b) Neglecting R_s & R_3, the feedback N/W is changed by Z_{in} MOD.

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* Fig @ shows INV amplifier ckt in which R_4 & C_4 are connected across the op-amp I/p terminals.

The capacitor C_4 acts as a open ckt to dc & passes (couples) ac signal.

Thus impedance of C_4 i.e X_{C4} is selected much smaller than the resistance of R_4 at the frequency at which $M\beta = 1$ ($X_{C4} \ll R_4$).

* At oscillation frequency of the ckt, R_4 appears in parallel ($C_4 \rightarrow$ acts as short ckt) with R_1 to give feedback N/W as shown in fig ⑥.

For simplicity, R_3 is assumed to be a short ckt and R_5 is taken to be much smaller than R_1 (i.e $R_5 \ll R_1$).

* Without R_4 & C_4 in the ckt, the feedback factor is $\boxed{\beta = \frac{R_1}{R_1 + R_2}}$.

* with R_4 in the ckt, the feedback factor becomes.

$$\boxed{\beta' = \frac{R_1 \,||\, R_4}{(R_1 \,||\, R_4) + R_2}} \qquad \because (R_1 \,||\, R_4)$$

Thus the voltage feedback from the o/p to the I/p is attenuated by the presence of R_4.

* for the ckt stability, the op-amp gain is now.

$$\frac{1}{\beta'} = \frac{(R_1 \,||\, R_4) + R_2}{R_1 \,||\, R_4}.$$

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* The voltage gain of INV amplifier remains

$$A_V = \frac{R_2}{R_1}$$

* Without the use of R_4 & C_4, the gain of the amplifier will be $A_V = \frac{1}{\beta}$. With the use of R_4 & C_2 $\beta' < \beta$. So that $\frac{1}{\beta'}$ is more.

The compensating components are actually selected according to higher gain. This increases the bandwidth.

* Due to presence of R_4 & C_4. Input impedance of op-amp is modified hence the method is called Z_{in} Mod compensation.

* The I/p Impedance is very high and is given by

$$Z_{in} = (1 + M\beta)(Z_{in} \parallel R_4)$$

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1) List the precautions that should be observed for op-amp circuit stability. Briefly explain each.

June-08, 8M | Jan-10, 4M | June-10, 8M

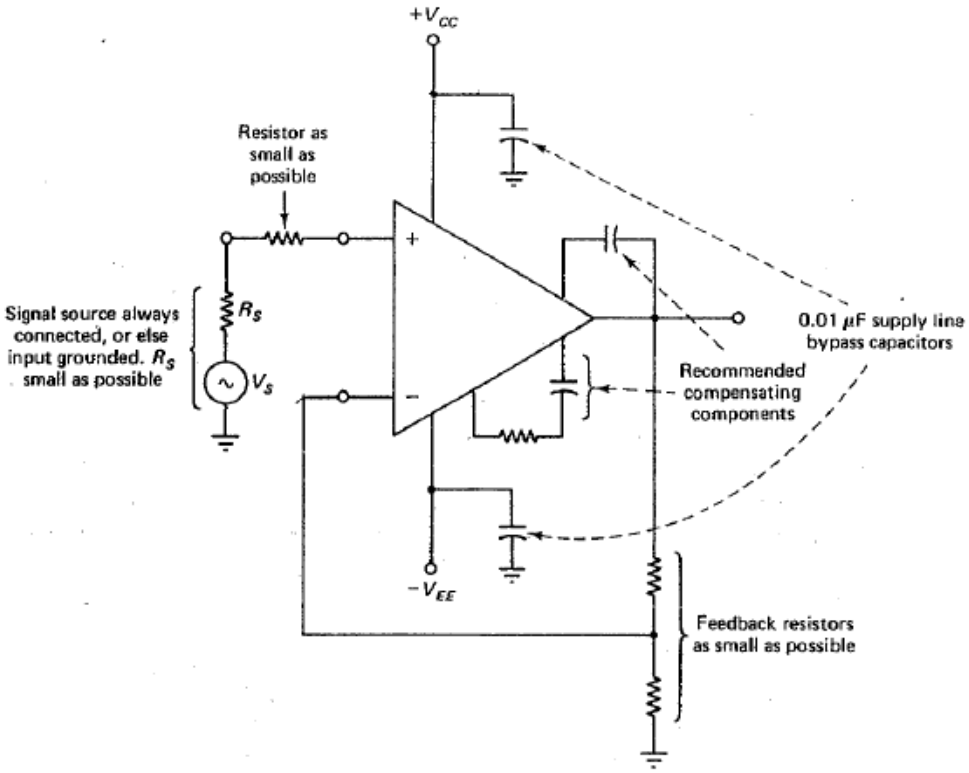

Figure For operational amplifier circuit stability, use the manufacturer's recommended compensating components, keep all resistor values to a minimum, connect 0.01 μF capacitors to bypass the supply lines to ground, and always have the signal source connected.

The following list of precautions should be observed for op-amp ckt stability:

1) For the low frequency applications, use an internally compensated op-amp like the 741.

2) When using an op-amp that must be compensated, use the manufacturer's recommended values & methods where possible use over-compensation.

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3) Keep all component leads as short as possible and take care with component placement.

Resistors connected to the op-amp I/p terminals should have the body of the resistor placed close to the I/p terminals.

4) Use 0.01 μF high frequency capacitors to bypass the supply terminals (V_{CC} & $-V_{EE}$) to ground. connect these capacitors close to the IC terminals.

5) Always connect signal source to the ckt or ground the ckt I/p (i.e Do not keep source open ckted).

6) Do not connect oscilloscopes or other instruments at the op-amp input terminals (INV & NON-INV I/p).

7) If a circuit is unstable after all of the above precautions have been observed, reduce the value of all circuit resistors. Also reduce the signal source resistance if possible.

If necessary, try compensating for stray capacitance or load capacitance.

8) For increasing circuit bandwidth, use Zin Mod compensation.

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Non-Linear circuit Applications

Crossing detectors :-

* What is zero crossing detector.

Whenever op-amp is operated in the open-loop mode & everytime an I/p signal crosses zero, the op-amp o/p will change its states either from +Vsat to -Vsat or vice-versa.

Zero-crossing detectors are of two types:

1) Non-INV Zero-crossing detector.
2) INV-Zero-crossing detector.

Non-INV Zero-crossing detector :-

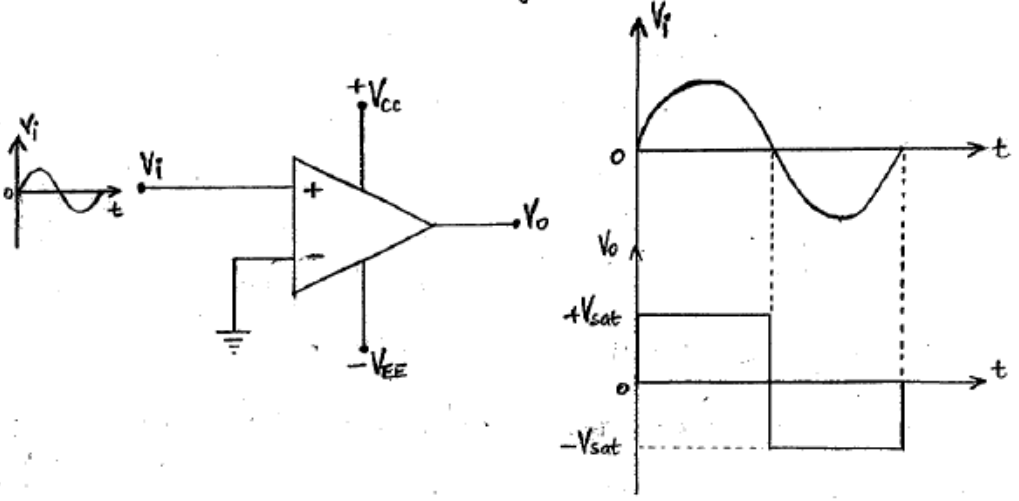

fig @ : Non-INV zero-crossing detector ckt.

* The input voltage is applied to the NON-INV terminal & INV terminal is grounded.

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When the input signal is positive, the o/p of the op-amp will be at $+V_{sat}$. When the input signal is negative, the o/p of the op-amp immediately switches to $-V_{sat}$.

Thus when the input signal crosses the zero level, the o/p voltage switches from one saturation level to another i.e $+V_{sat}$ to $-V_{sat}$. So this ckt is called NON-INV zero crossing detector.

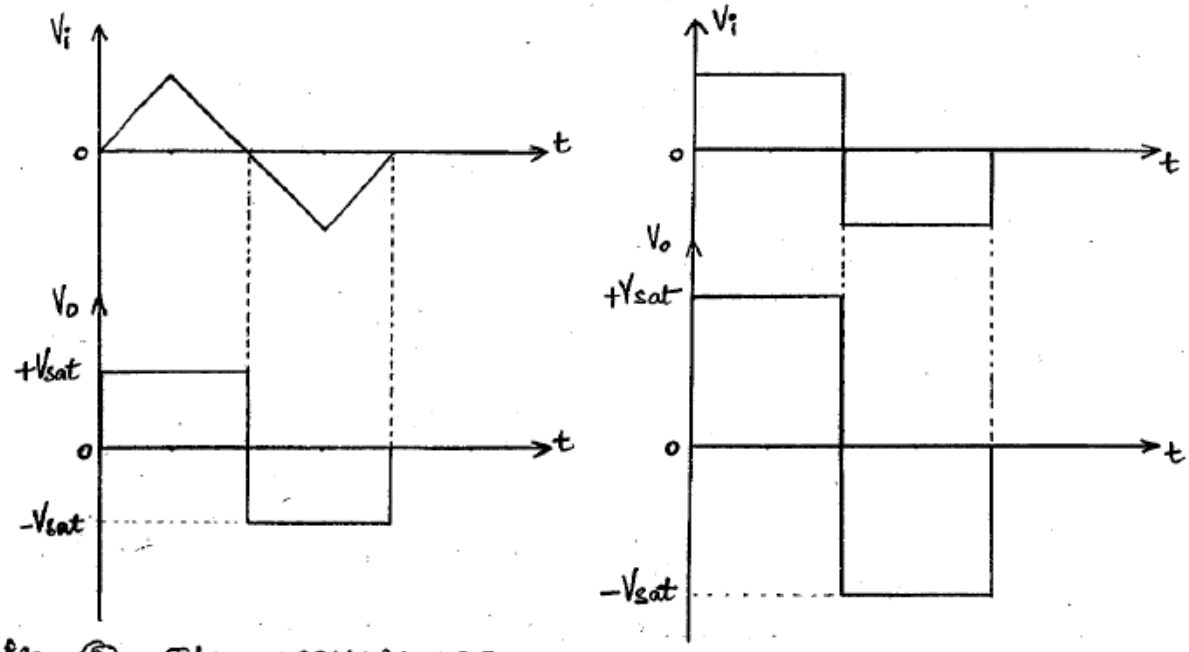
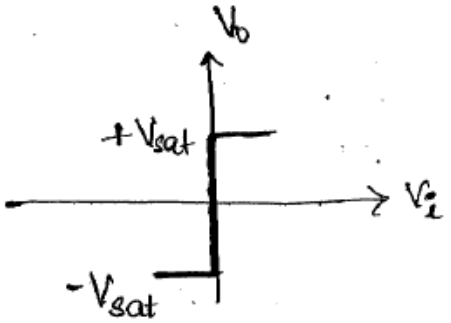


fig ⑤ I/o waveforms.

fig ② shows the o/p waveforms that result for various I/p to a zero-crossing detector.

Regardless of the I/p waveshape, the o/p is always a rectangular waveform.

Transfer characteristics :-



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INV Zero crossing detector :-

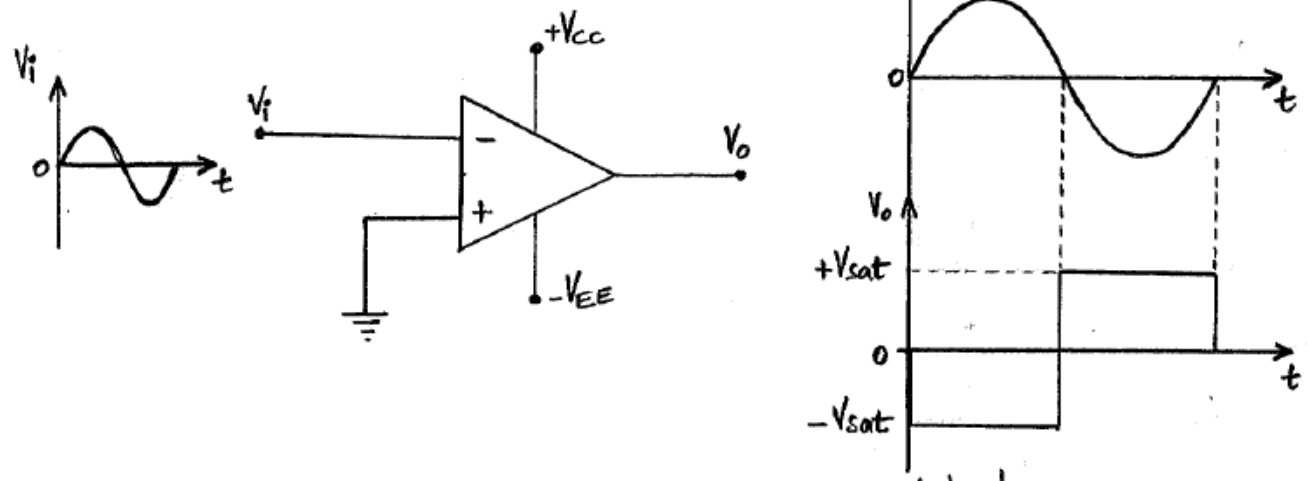
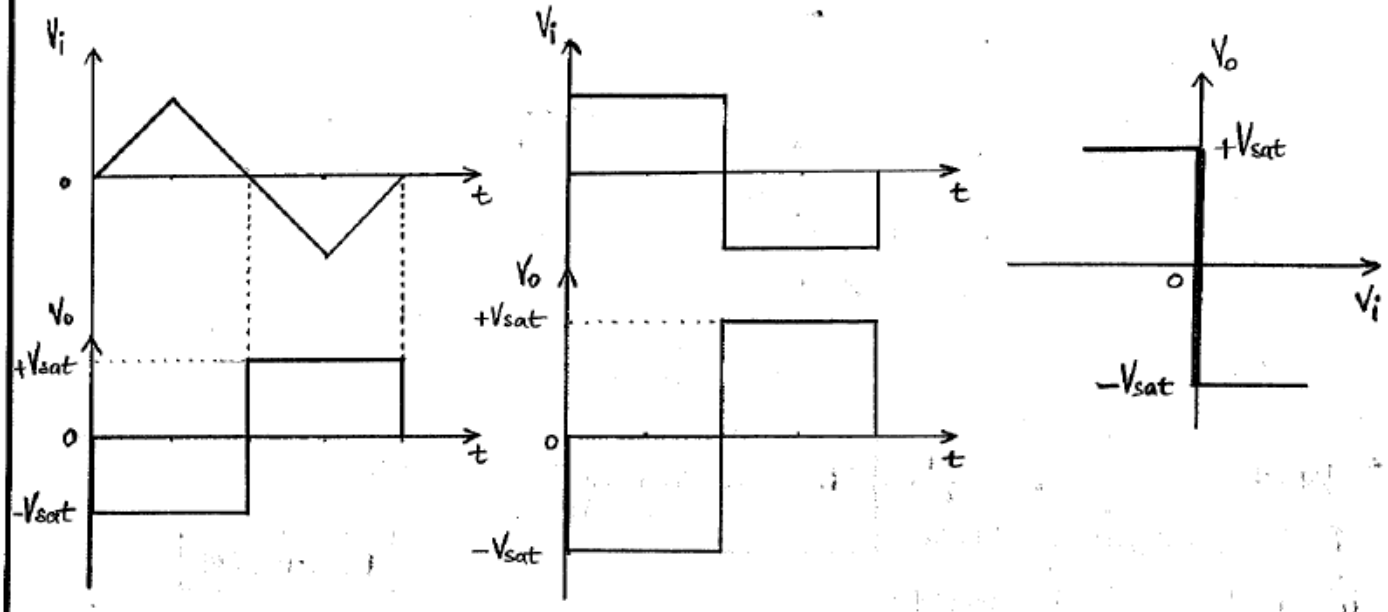


fig ① : INV zero-crossing detector

When the input signal is positive, the o/p of the op-amp will be at $-V_{sat}$. When the I/p signal is negative, the o/p of the op-amp immediately switches to $+V_{sat}$.

Thus when the input signal crosses the zero level, the o/p voltage switches from one saturation level to another i.e $+V_{sat}$ to $-V_{sat}$. So this ckt is called INV - zero crossing detector. Sometimes termed as inverter.



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Voltage - level detector : (NON-INV)

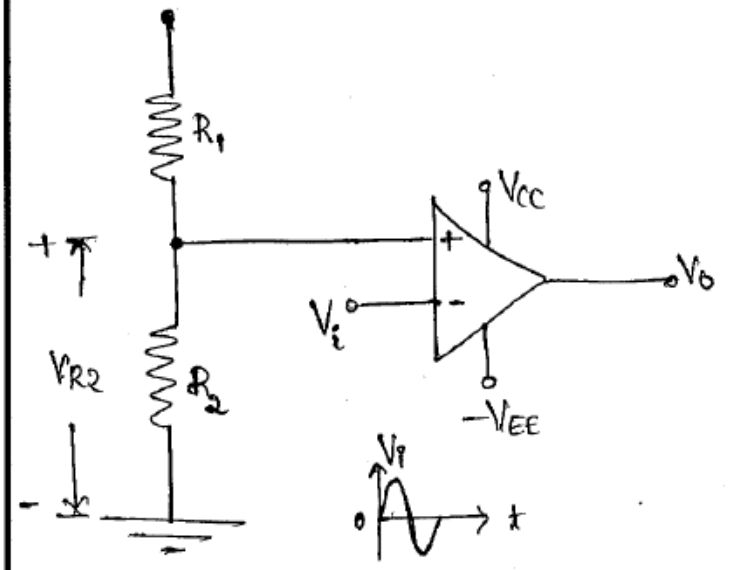

fig ① : Voltage level detector.

* Instead of biasing the NON-INV terminal to ground level it can be connected to a positive or negative dc voltage level as shown in fig ①. Here the o/p changes each time input crosses the reference voltage. Thus this ckt is called a voltage level detector.

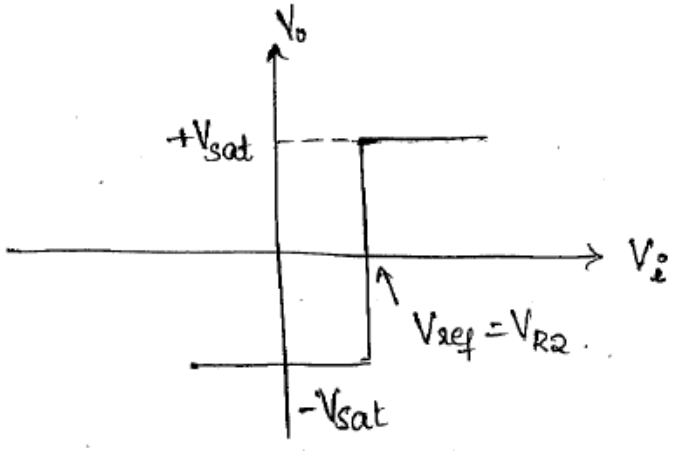

fig ② : Transfer characteristics.

* With waveforms, explain the working of :
  i) Zero-Crossing detector
  ii) voltage - level detector

Dec-10, 6M

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Capacitor · Coupled crossing detector :-

* Explain working of capacitor coupled zero crossing detector, show waveforms at various points.

Jan-06, 6M(EE)	June-06, 6M(EE)	Jan-08, 08 M(EE)	June-09, 7M(EE)

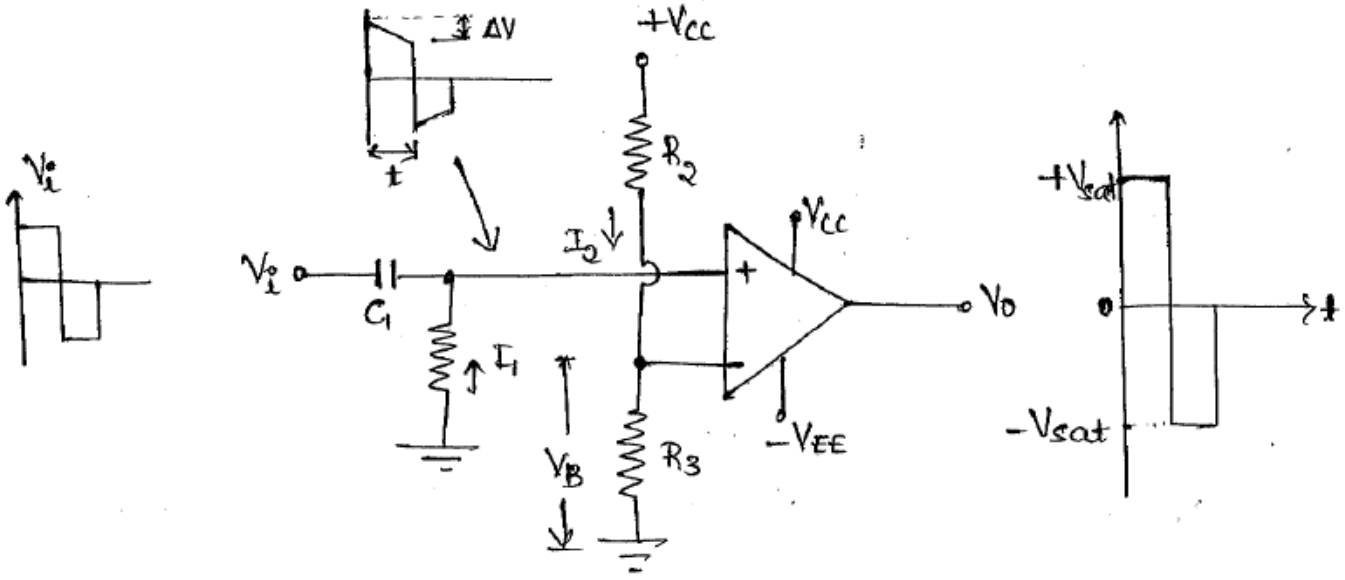

fig @ Capacitor coupled crossing detector.

fig @ shows capacitor coupled crossing detector with Non-INV terminal connected to ground via resistor R_1 to provide a dc bias current path to the op-amp.

The INV terminal connected to a potential divider ckt. Due to this INV terminal is held at a small +ve voltage (V_B). This ensures that the o/p is held at $-V_{sat}$, when no input signal is present.

* When capacitor-coupled signal (V_i) drives the Non-INV I/p terminal above V_B, the o/p switches to $+V_{sat}$ and when input is less than V_B (i.e. $V_i < V_B$) the o/p falls back to $-V_{sat}$.

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* The resistance R_1 is designed as

$$R_{1(max)} = R_1 = \frac{0.1 V_{BE}}{I_{B(max)}}$$

* The current I_2 is chosen to be about 100 times $I_{B(max)}$

$$\therefore I_2 = 100 \times I_{B(max)}$$

* The voltage V_B across R_3 is given by:

$$V_B = I_2 R_3$$

$$R_3 = \frac{V_B}{I_2}$$

$$V_B = V_{R3} = 0.1V$$

V_B is usually chosen to be about 0.1V.

* Applying KVL from V_{CC}, R_2 & R_3, we get

$$V_{CC} - I_2 R_2 - I_2 R_3 = 0.$$

$$V_{CC} = I_2 [R_2 + R_3]$$

$$R_2 + R_3 = \frac{V_{CC}}{I_2}$$

$$R_2 = \frac{V_{CC}}{I_2} - R_3$$

$$V_{CC} - V_{R2} - V_B = 0.$$

$$V_{R2} = V_{CC} - V_B$$

NOTE $V_B = V_{R3}$

$$V_{R2} = V_{CC} - V_{R3}$$

$$\therefore R_2 = \frac{V_{R2}}{I_2}$$

* At lower frequency, X_{C1} should be much smaller than R_1 i.e $X_{C1} = \frac{R_1}{20}$ $\therefore C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{20}\right)}$

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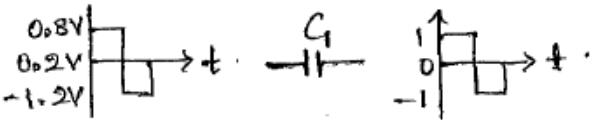
* The input voltage to capacitor 'C_1' may not be symmetrical above or below ground level, but it is always symmetrical on the op-amp side of C_1.

(eg :



* When square wave is applied as an input to a capacitor – coupled detector, the waveform at the op-amp input terminal can develop considerable tilt as shown in fig ①.

* The I/p current is calculated as :

$$I_1 = \frac{V_i}{R_1}$$

(Note.
$I_1 = \frac{V_{i(peak)}}{R_1}$)

Assuming I_1 constant,

$$C_1 = \frac{I_1 t}{\Delta V}$$

Where,

$t = \frac{1}{2f}$

$\because$ $T = t + t$

$T = 2t$

$t = \frac{T}{2}$.

$t = \frac{1}{2f}$.

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FORMULAE

Design steps:-

1) $R_1 = \dfrac{0.1\,V_{BE}}{I_{B(max)}}$

2) Let $I_2 = 100 \times I_{B(max)}$

3) Assume $V_B = V_{R3} = 0.1V$

4) $V_{R2} = V_{CC} - V_B$

5) $R_2 = \dfrac{V_{R2}}{I_2}$

6) $R_3 = \dfrac{V_{R3}}{I_2}$

7) $V_{i(peak)} = \dfrac{V_{i(p-p)}}{2}$

8) $I_1 = \dfrac{V_i}{R_1}$

9) Assume $\Delta V = 1V$

10) $t = \dfrac{T}{2} = \dfrac{1}{2f}$

11) $C_1 = \dfrac{I_1 t}{\Delta V}$

Formulae to find the Slew rate.

1) $\Delta V_0 = +V_{sat} - (-V_{sat})$

WKT $+V_{sat} = (V_{CC} - 1)$

$-V_{sat} = (-V_{EE} + 1)$

2) $\Delta t = 0.1 \times t$

3) $X_{C1} = \dfrac{R_1}{20}$

4) $f_{(min)} = \dfrac{1}{2\pi X_{C1} C_1}$

5) $S_{min} = \dfrac{\Delta V_0}{\Delta t}$

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Problems

1) A capacitor-coupled zero-crossing detector is to handle a 1KHz square wave input with a peak-to-peak amplitude of 6V. Design a suitable circuit, using a 741 op-amp with a ±12V supply.

Given :- $f = 1\,KHz$, $V_{(p-p)} = 6V$, $V_{CC} = 12V$.

Sol :- For op-amp 741 : $I_{B(max)} = 500\,nA$

Assuming i) $\Delta V = 1V$,

ii) $V_B = V_{R3} = 0.1V$

iii) $V_{BE} = 0.7V$

* $R_1 = \dfrac{0.1 V_{BE}}{I_{B(max)}} = \dfrac{0.1 \times 0.7V}{500\,nA} = 140\,K\Omega$

use $\boxed{R_1 = 120\,K\Omega}$

* Let $I_2 = 100 \times I_{B(max)} = 100 \times 500\,nA$

$\boxed{I_2 = 50\,\mu A}$

* $V_{R2} = V_{CC} - V_B = 12V - 0.1V$

$\boxed{V_{R2} = 11.9V}$

* $R_2 = \dfrac{V_{R2}}{I_2} = \dfrac{11.9V}{50\,\mu A} = \underline{238\,K\Omega}$

Use standard value : $\boxed{R_2 = 220\,K\Omega}$

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Now $I_2 = \frac{V_{R2}}{R_2} = \frac{11.9\ V}{220\ K\Omega}$

$$\boxed{I_2 = 54.1\ \mu A}$$

* $R_3 = \frac{V_{R3}}{I_2} = \frac{0.1\ V}{54.1\ \mu A} = 1.85\ K\Omega$

Use $\boxed{R_3 = 1.8\ K\Omega}$

* $V_{i(peak)} = \frac{V_{i(p-p)}}{2} = \frac{6V}{2}$

$$\boxed{V_{i(peak)} = 3V}$$

* $I_1 = \frac{V_i}{R_1} = \frac{3V}{120\ K\Omega}$

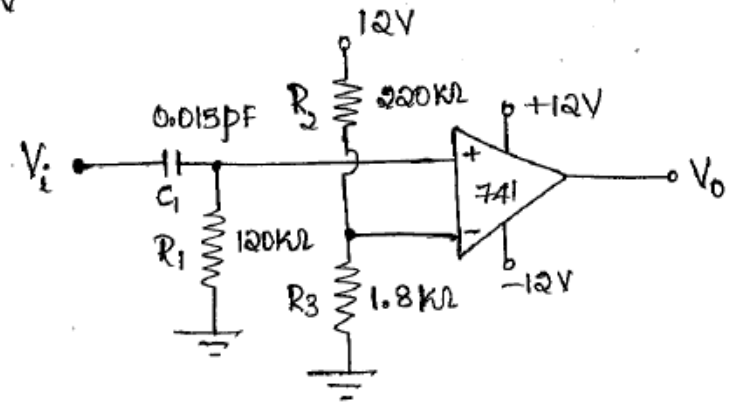
$$\boxed{I_1 = 25\ \mu A}$$

* $t = \frac{1}{2f} = \frac{1}{2 \times 1KHz}$

$$\boxed{t = 500\ \mu s}$$

* $C_1 = \frac{I_1 t}{\Delta V} = \frac{25\ \mu A \times 500\ \mu S}{1V} = 0.0125\ \mu F$

Use $\boxed{C_1 = 0.015\ \mu F}$



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2) For the circuit designed in problem 1, estimate the minimum op-amp slew rate to give a reasonably undistorted o/p. Also, calculate the lowest sine wave input frequency that can be applied without the phase shift error exceeding 3°.

Given: from problem 1

$V_{CC} = 12V$, $-V_{EE} = -12V$, $t = 500\,\mu sec$, $R_1 = 120\,K\Omega$

Sol:- $\Delta V_0 = +V_{sat} - (-V_{sat})$

$+V_{sat} = V_{CC} - 1V = 12V - 1V$

$\boxed{+V_{sat} = 11V}$

$-V_{sat} = (-V_{EE} + 1V) = -12V + 1V$

$\boxed{-V_{sat} = -11V}$

$\Delta V_0 = 11V - (-11V)$

$\therefore \boxed{\Delta V_0 = 22V}$

* $\Delta t = 0.1 \times t = 0.1 \times 500\,\mu sec$

$\boxed{\Delta t = 50\,\mu sec}$

* $S_{min} = \frac{\Delta V_0}{\Delta t} = \frac{22V}{50\,\mu s} = 0.44\,V/\mu s.$

* $X_{C1} = \frac{R_1}{20} = \frac{120K\Omega}{20}$

$\boxed{X_{C1} = 6K\Omega}$

* $f_{(min)} = \frac{1}{2\pi X_{C1} C_1} = \frac{1}{2\pi \times 6K\Omega \times 0.015\,\mu F} = 1.8\,KHz.$

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3) A capacitor-coupled zero crossing detector is to handle a 2KHz square wave with a peak-to-peak amplitude of 10V. Design a ckt using a 741 op-amp with a ±15V supply. Estimate the minimum op-amp slew rate to give a reasonably undistorted o/p. Also, calculate the lowest sine wave input frequency that can be applied without the phase shift error exceeding 5°.

June-09, 8m

Given: $V_B = 0.1V$, $I_{B(max)} = 500nA$

$f = 2KHz$, $V_{(p-p)} = 10V$, $V_{CC} = 15V$, $-V_{EE} = -15V$

Sol: Assuming

$\Delta V = 1V$

$V_B = V_{R3} = 0.1V$

$V_{BE} = 0.7V$

* $R_1 = \frac{0.1 V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7V}{500nA} = 140K\Omega$

Use $R_1 = 120K\Omega$ ← (1m).

* Let $I_2 = 100 \times I_{B(max)} = 100 \times 500nA$

$I_2 = 50\mu A$

* $V_{R2} = V_{CC} - V_B = 15 - 0.1V$

$V_{R2} = 14.9V$

* $R_2 = \frac{V_{R2}}{I_2} = \frac{14.9V}{50\mu A} = 298K\Omega$

Use $R_2 = 270K\Omega$

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* Now $I_2 = \frac{V_{R2}}{R_2} = \frac{14.9V}{270K\Omega}$

$$\boxed{I_2 = 65.18\,\mu A}$$

* $R_3 = \frac{V_{R3}}{I_2} = \frac{0.1V}{50\,\mu A} = 2K\Omega$

use $\boxed{R_3 = 1.8K\Omega}$ ← (1M)

* $V_{i(peak)} = \frac{V_{i(p-p)}}{2} = \frac{10\,V}{2}$

$$\boxed{V_{i(peak)} = 5V}$$

* $I_1 = \frac{V_i}{R_1} = \frac{5V}{1.8K\Omega}$

$$\boxed{I_1 = 41.6\,\mu A}$$

* $t = \frac{1}{2f} = \frac{1}{2 \times 2KHz}$

$$\boxed{t = 250\,\mu sec}$$

* $C_1 = \frac{I_1 t}{\Delta V} = \frac{41.6\,\mu A \times 250\mu}{1V} = 0.0104\,\mu sec$

use $\boxed{C = 0.01\,\mu F}$ ← (1M)

* $\Delta V_0 = +V_{sat} - (-V_{sat})$

$+V_{sat} = (V_{CC} - 1) = (15V - 1V) = 14V$

$-V_{sat} = (-V_{EE} + 1) = (-15V + 1V) = -14V$

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$\therefore \quad \Delta V_0 = 14 - (-14\,V)$

$$\boxed{\Delta V_0 = 28\,V} \leftarrow (1M)$$

* $t = \frac{1}{2f} = \frac{1}{2 \times 2 \times 10^3}$

$$\boxed{t = 250\,\mu sec}$$

* $\Delta t = 0.1 \times t = 0.1 \times 250\,\mu sec$

$$\boxed{\Delta t = 25\,\mu sec}$$

* $X_{C1} = \frac{R_1}{20} = \frac{120\,K\Omega}{20}$

$$\boxed{X_{C1} = 6\,K\Omega}$$

* $S(min) = \frac{\Delta V_0}{\Delta t} = \frac{28\,V}{25\,\mu sec.}$

$$\boxed{S(min) = 1.12\,V/\mu sec} \leftarrow (1M)$$

* $f(min) = \frac{1}{2\pi X_{C1} C_1} = \frac{1}{2\pi \times 6\,K\Omega \times 0.01\,\mu F}$

$$\boxed{f(min) = 2.65\,kHz} \leftarrow (1M)$$

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4) A capacitor coupled zero detector is to handle a 1KHz square wave with a peak to peak amplitude of 6V. Design a suitable circuit using a 741 op-amp with a ±12V supply. Estimate the minimum op-amp slew rate to give a reasonably undistorted output. Also calculate the lowest sine wave input frequency that can be applied without the phase shift error exceeding 3°.

Jan-09, 8M(EE)

Given :-

$f = 1KHz$, $V_{(p-p)} = 6V$, $+V_{CC} = 12V$, $-V_{EE} = -12V$

Sol :- Assuming :

$V_{BE} = 0.7V$

$V_B = V_{R3} = 0.1V$

$\Delta V = 1V$

for 741 op-amp : $I_{B(max)} = 500nA$

* $R_1 = \frac{0.1\ V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7V}{500nA} = 140K\Omega$

choose. $R_1 = 120K\Omega$

* Let $I_2 = 100 \times I_{B(max)} = 100 \times 500nA$

$I_2 = 50\mu A$

* $V_{R2} = V_{CC} - V_B = 12V - 0.1V$

$V_{R2} = 11.9V$

* $R_2 = \frac{V_{R2}}{I_2} = \frac{11.9V}{50\mu A} = 238K\Omega$

choose, $R_2 = 270K\Omega$

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* Now $I_2 = \frac{V_{R2}}{I_2} = \frac{11.9V}{270K\Omega}$.

$$\boxed{I_2 = 54.1\mu A}$$

* $R_3 = \frac{V_{R3}}{I_2} = \frac{0.1V}{54.1\mu A} = 1.85K\Omega$

Choose $\boxed{R_3 = 1.8K\Omega}$

* $V_{i(peak)} = \frac{V_{i(p-p)}}{2} = \frac{6V}{2}$

$$\boxed{V_{i(peak)} = 3V}$$

* $I_1 = \frac{V_{i(p)}}{R_1} = \frac{3V}{120K\Omega}$

$$\boxed{I_1 = 25\mu A}$$

* $t = \frac{1}{2f} = \frac{1}{2 \times 1KHz}$

$$\boxed{t = 50.0\,msec}$$

* $C_1 = \frac{I_1 t}{\Delta V} = \frac{25\mu A \times 500\mu sec}{1V} = 0.0125\mu F.$

Choose $\boxed{C_1 = 0.015\mu F}$

* $\Delta V_0 = +V_{sat} - (-V_{sat}) = [V_{cc} - 1] - [-V_{EE} + 1]$

$\Delta V_0 = (12-1) - (-12+1)$

$$\boxed{\Delta V_0 = 22V}$$

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* $\Delta t = 0.1 \times t = 0.1 \times 500\,\mu sec$

$$\boxed{\Delta t = 50\,\mu sec}$$

* $S_{min} = \frac{\Delta V_o}{\Delta t} = \frac{22V}{50\,\mu sec}$

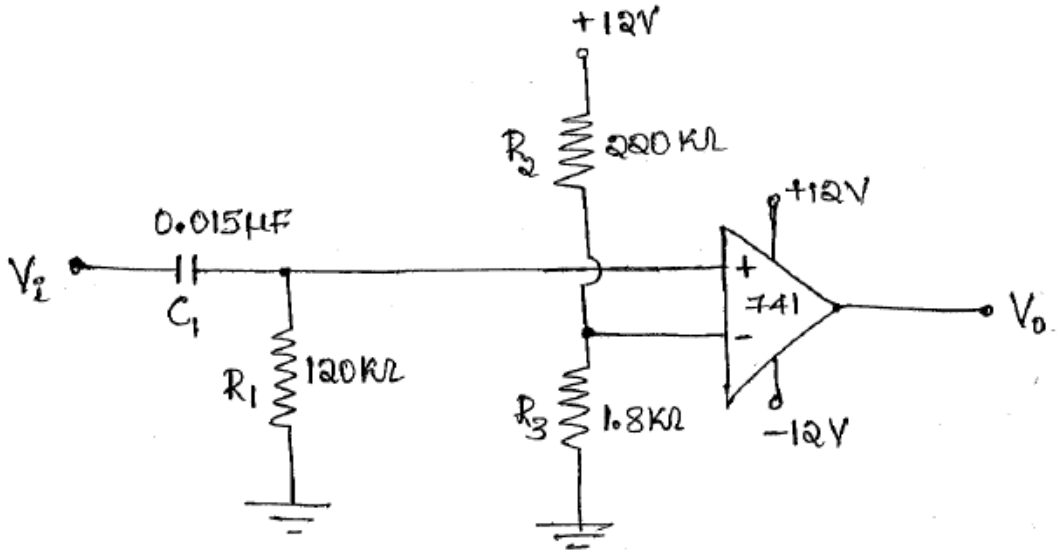
$$\boxed{S_{min} = 0.44\,V/\mu sec}$$

* $X_{C1} = \frac{R_1}{20} = \frac{120\,K\Omega}{20}$

$$\boxed{X_{C1} = 6K\Omega}$$

* $f_{(min)} = \frac{1}{2\pi X_{C1} C_1} = \frac{1}{2\pi \times 6K\Omega \times 0.015\mu F}$

$$\boxed{f_{(min)} = 1.8\,KHz}$$



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5) A capacitor coupled zero crossing detector is to provide an o/p voltage of approximately ±15V, when a 5KHz, ±3V square wave input is applied. Design a suitable ckt to use a bipolar op-amp. Tilt at the Non-INV terminal ΔV is to be 0.75V.

June-07, 6M(EE)

Given :- $V_{CC} = +15V$, $-V_{EE} = -15V$, $f = 5KHz$,

$V_i = 3V$, $\Delta V = 0.75V$.

Sol :- Assuming : $V_{BE} = 0.7V$, $V_B = V_{R3} = 0.1V$

For 741 op-amp : $I_{B(max)} = 500nA$

* $R_1 = \frac{0.1 V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7V}{500nA} = 140K\Omega$

Choose, $R_1 = 120K\Omega$

* Let $I_2 = 100 \times I_{B(max)} = 100 \times 500nA$

$I_2 = 50\mu A$

* $V_{R2} = V_{CC} - V_B = 15V - 0.1V$

$V_{R2} = 14.9V$

* $R_2 = \frac{V_{R2}}{I_2} = \frac{14.9V}{50\mu A} = 298K\Omega$

Choose $R_2 = 270K\Omega$

Now. $I_2 = \frac{V_{R2}}{R_2} = \frac{14.9V}{270K\Omega}$ $\therefore I_2 = 55.18\mu A$

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* $R_3 = \frac{V_{R3}}{I_2} = \frac{0.1\,V}{55.18\,\mu A} = 1.812\,K\Omega$

choose $\boxed{R_3 = 1.8\,K\Omega}$

* $I_1 = \frac{V_{i(p)}}{R_1} = \frac{3\,V}{120\,K\Omega}$

$\boxed{I_1 = 25\,\mu sec}$

* $t = \frac{1}{2f} = \frac{1}{2 \times 5\,KHz}$

$\boxed{t = 100\,\mu sec}$

* $C_1 = \frac{I_1 t}{\Delta V} = \frac{25\,\mu sec \times 100\,\mu sec}{0.75\,V.}$

$\boxed{C_1 = 3333.33\,pF}$ choose $\boxed{C_1 = 3300\,pF}$

* $\Delta V_0 = +V_{sat} - (-V_{sat})$

$+V_{sat} = (V_{cc} - 1V) = (15V - 1V) = 14\,V$

$-V_{sat} = (-V_{EE} + 1V) = (-15 + 1V) = -14\,V$

$\Delta V_0 = 14\,V - (-14\,V)$

$\boxed{\Delta V_0 = 28\,V}$

* $\Delta t = 0.1 \times t = 0.1 \times 100\,\mu sec$

$\boxed{\Delta t = 10\,\mu sec}$

* $S_{min} = \frac{\Delta V_0}{\Delta t} = \frac{28\,V}{10\,\mu sec}$

$\boxed{S_{min} = 2.8\,V/\mu sec}$

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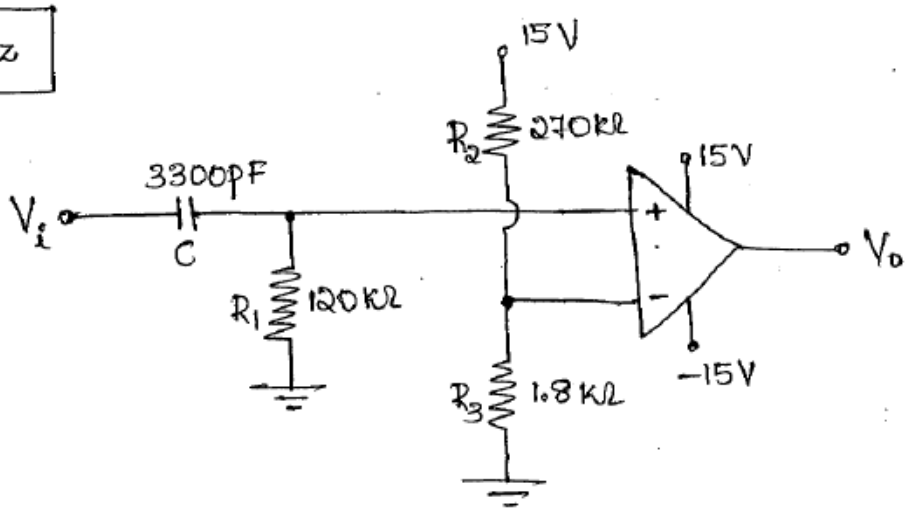
* $X_{C1} = \frac{R_1}{20} = \frac{120\,K\Omega}{20}$

$\boxed{X_{C1} = 6\,K\Omega}$

$f_{min} = \frac{1}{2\pi X_{C1} C_1} = \frac{1}{2\pi \times 6K\Omega \times 3300pF}$

$\boxed{f_{min} = 8.038\,KHz}$



6) A capacitor coupled zero crossing detector is to provide an o/p voltage of approximately ±17V, when a 3KHz, ±2V square wave I/p is applied. Design a suitable ckt to use a bipolar op-amp. Jan-06, 6M (EE)

Given: $+V_{CC} = 17V$, $-V_{EE} = -17V$, $f = 3KHz$, $V_{i(p)} = 2V$.

Sol: Assuming

i) $A_V = 1$
ii) $V_B = V_{R3} = 0.1V$
iii) $V_{BE} = 0.7V$

For 741 op-amp: $I_{B(max)} = 500nA$

* $R_1 = \frac{0.1\,V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7V}{500nA} = 140\,K\Omega$ choose $\boxed{R_1 = 120K\Omega}$

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* Let $I_2 = 100 \times I_{B(max)} = 100 \times 500\,nA$

$$\boxed{I_2 = 50\,\mu A}$$

* $V_{R2} = V_{CC} - V_B = 17V - 0.1V$

$$\boxed{V_{R2} = 16.9\,V}$$

* $R_2 = \frac{V_{R2}}{I_2} = \frac{16.9\,V}{50\,\mu A} = 338\,K\Omega$, choose $\boxed{R_2 = 330\,K\Omega}$

* Now $I_2 = \frac{V_{R2}}{R_2} = \frac{16.9\,V}{330\,K\Omega}$. $\boxed{I_2 = 51.212\,\mu A}$

* $R_3 = \frac{V_{R3}}{I_2} = \frac{0.1\,V}{51.212\,\mu A} = 1.952\,K\Omega$

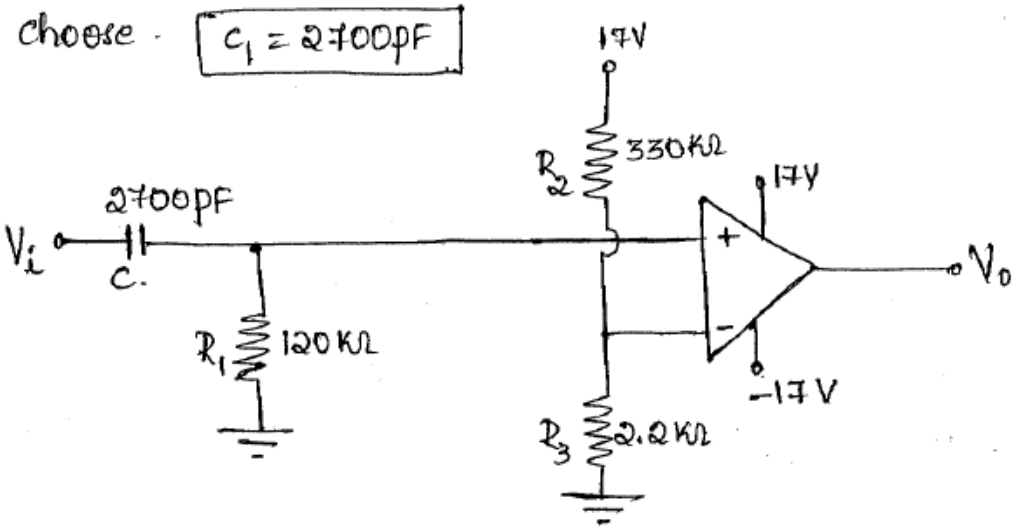
choose $\boxed{R_3 = 2.2\,K\Omega}$

* $I_1 = \frac{V_{i(p)}}{R_1} = \frac{2V}{120\,K\Omega}$, $\boxed{I_1 = 16.66\,\mu A}$

* $t = \frac{1}{2f} = \frac{1}{2 \times 3\,KHz}$, $\boxed{t = 166.66\,\mu sec}$

* $C_1 = \frac{I_1 t}{\Delta V} = \frac{16.66\,\mu A \times 166.66\,\mu sec}{1V} = 2776.55\,pF$.

choose $\boxed{C_1 = 2700pF}$



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INVERTING SCHMITT TRIGGER CIRCUIT :-

1) With a neat circuit diagram and waveforms, explain the operation of INV schmitt trigger.

June -09, 6 M | June-10, 6M(EE) | Jan-09, 6M(EE) | June-06, 6 M(EE) | Jan-05, 6 M(EE)

2) Explain the operation of an INV schmitt trigger circuit with different UTP & LTP voltages, with the help of a suitable ckt. Discuss the design procedure for components used. Also indicate the input/output characteristics for the INV schmitt trigger circuit.

Jan -10, 10M

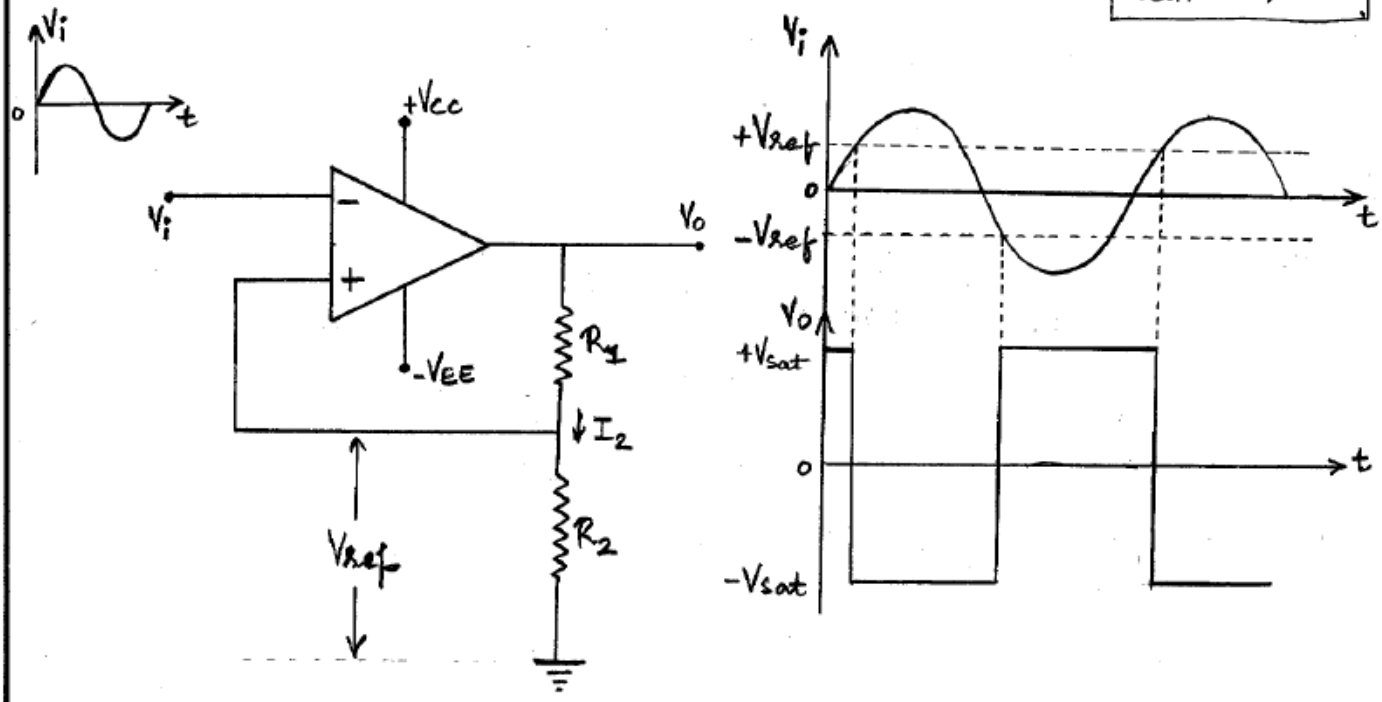

fig 1 @ shows an INV schmitt trigger circuit.

* The input is applied to the inverting terminal of the schmitt trigger circuit. The feedback signal is given to the NON-INV terminal. This ensures +ve feedback.

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* The voltage at the Non-INV input is

$$V_{ref} = I_2 R_2$$

Where $$I_2 = \frac{V_0}{R_1 + R_2}$$

$$\therefore \boxed{V_{ref} = \frac{V_0 R_2}{R_1 + R_2}}$$

* When the o/p voltage V_0 is at $+V_{sat}$, then V_{ref} will be a positive voltage & voltage at Non-INV terminal will also be positive ($+V_{ref}$).

i.e $$V_{ref} = \frac{V_0 R_2}{R_1 + R_2}$$ ($\because$ Now $V_0 = +V_{sat}$)

$$\boxed{+V_{ref} = \frac{+V_{sat} R_2}{R_1 + R_2}}$$ (+Ve saturation)

* When $V_i > +V_{ref}$, then the voltage at INV terminal becomes greater than ($+V_{ref}$) Non INV terminal & the o/p will switch from $+V_{sat}$ to $-V_{sat}$.

i.e. $$V_{ref} = \frac{V_0 R_2}{R_1 + R_2}$$ ($\because$ Now $V_0 = -V_{sat}$)

$$\therefore \boxed{-V_{ref} = \frac{-V_{sat} R_2}{R_1 + R_2}}$$ (-ve saturation)

* In fig 1 (b), the voltage at point $+V_{ref}$ on the waveform at which o/p shifts from $+V_{sat}$ to $-V_{sat}$ is called "upper Triggering point" (UTP).

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Similarly, the voltage at point $-V_{ref}$ on the waveform at which o/p shifts from $-V_{sat}$ to $-V_{sat}$ is called "Lower Triggering point" (LTP).

Thus the o/p of a schmitt trigger is always a square wave or rectangular wave.

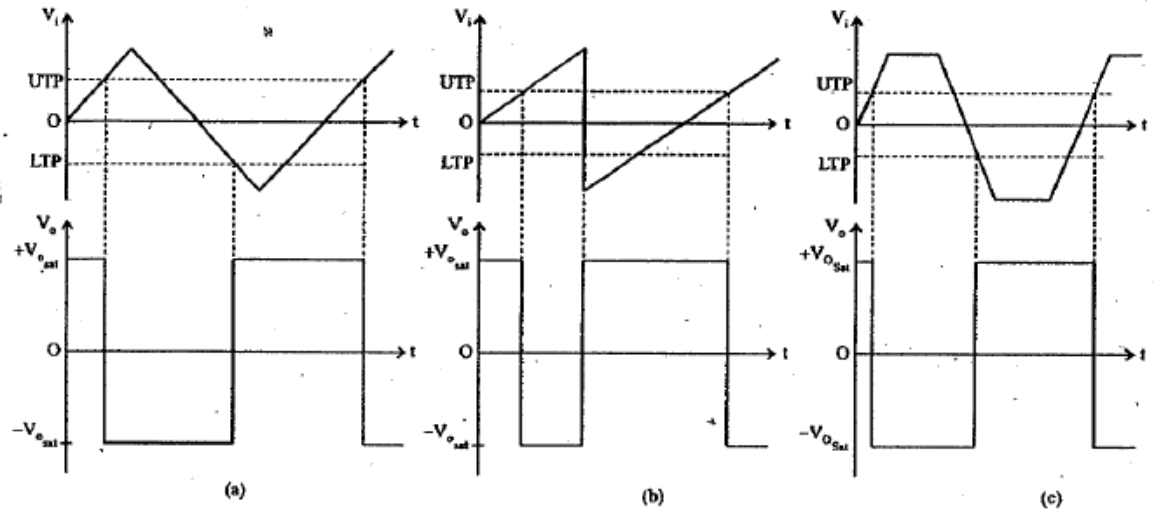

Fig. : (a) Triangular input waveform producing square wave
(b) Saw tooth input waveform producing square wave
(c) Trapezoidal input waveform producing square wave

Input / output characteristics or Transfer characteristics :-

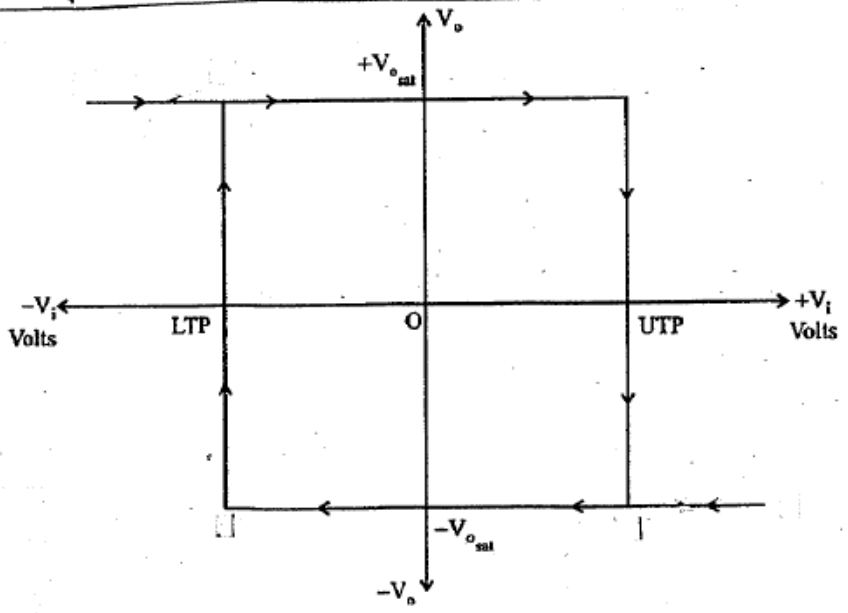

Fig. : Input/output characteristics (transfer characteristics) of Schmitt trigger

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* When $V_i = 0V$, the o/p will be at $+V_{sat}$. When $V_i = UTP$ the o/p switches from $+V_{sat}$ to $-V_{sat}$.

When $V_i < LTP$, the o/p will be at $-V_{sat}$. When $V_i = LTP$, the o/p switches from $-V_{sat}$ to $+V_{sat}$.

* The voltage difference between the upper and lower triggering points is referred to as hysteresis.

$$\therefore \boxed{V_H = UTP - LTP}$$

Schmitt trigger circuit design :-

* The current I_2 flowing through the resistors R_1 & R_2 is chosen to be 100 times $I_{B(max)}$.

i.e. $\boxed{I_2 = 100\, I_{B(max)}}$

* $R_2 = \dfrac{\text{triggering voltage}}{I_2}$

* $R_1 = \dfrac{V_0 - \text{triggering voltage}}{I_2}$

NOTE : WKT $V_{ref} = I_2 R_2$

* $R_2 = \dfrac{V_{ref}}{I_2}$

* Applying KVL from o/p V_0, R_1 & R_2, we get

$V_0 - I_2 R_1 - V_{ref} = 0.$

$V_0 - V_{ref} = I_2 R_1.$ $\therefore \boxed{R_1 = \dfrac{V_0 - V_{ref}}{I_2}}$

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FORMULAE :-

For equal UTP & LTP i.e, UTP = LTP

1) Let $I_2 = 100 \times I_{B(max)}$

2) UTP $= V_{R2}$

3) $R_2 = \frac{V_{R2}}{I_2}$

4) Applying KVL from V_0, R_1 & R_2

$$V_0 - I_2R_1 - I_2R_2 = 0$$

$$V_0 - I_2R_1 - V_{R2} = 0.$$

$$I_2R_1 = V_0 - V_{R2}$$

$$R_1 = \frac{V_0 - V_{R2}}{I_2}.$$

$$V_0 = +V_{sat}$$

$$\boxed{R_1 = \frac{V_{sat} - V_{R2}}{I_2}}$$

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1) Using a 741 op-amp with a supply of ±12V, design an INV-schmitt triggering circuit to have trigger points of ±2V.

Given :- $V_{cc} = +12V$, $V_{sat} = 12V$, $UTP = LTP = 2V$.

Sol :- for 741 op-amp : $I_{B(max)} = 500nA$

* let $I_2 = 100 \times I_{B(max)} = 100 \times 500nA$

$$\boxed{I_2 = 50\mu A}$$

* $$\boxed{V_{R2} = UTP = 2V}$$

* $$R_2 = \frac{V_{R2}}{I_2} = \frac{2V}{50\mu A} = 40K\Omega$$

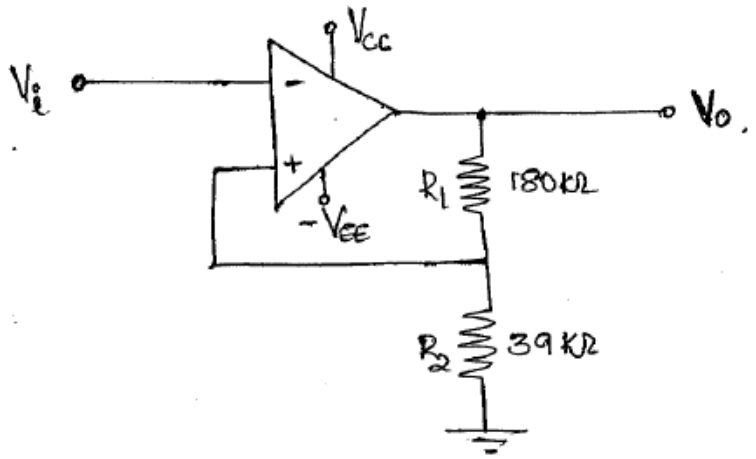
choose $\boxed{R_2 = 39K\Omega}$

Now, $$I_2 = \frac{V_{R2}}{I_2} = \frac{2V}{39K\Omega}$$

$$\boxed{I_2 = 51.3\mu A}$$

* $$R_1 = \frac{V_{sat} - V_{R2}}{I_2} = \frac{12-2}{51.3\mu A} = 175\Omega$$

choose $\boxed{R_1 = 180\Omega}$



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2) Using a bipolar op-amp, design an INV schmitt trigger ckt to trigger at ± 0.8 volts and to produce an o/p of approximately ± 11 V.

Given :- $\pm V_{sat} = \pm 11V$, $UTP = LTP = \pm 0.8V$

For 741 op-amp · $I_{B(max)} = 500nA$

Sol :-

* Let $I_2 = 100 \times I_{B(max)} = 100 \times 500nA$

$$\boxed{I_2 = 50\,\mu A}$$

* $V_{R2} = UTP = 0.8V$

* $R_2 = \frac{V_{R2}}{I_2} = \frac{0.8V}{50\,\mu A} = 16\,K\Omega$

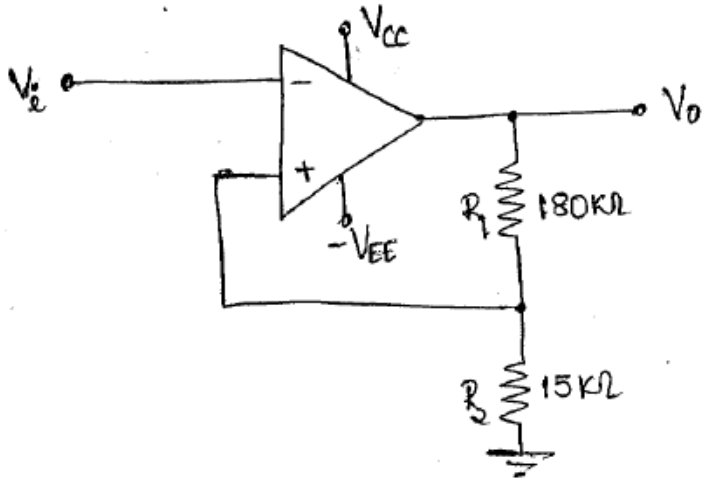
Choose $\boxed{R_2 = 15\,K\Omega}$

* Now $I_2 = \frac{V_{R2}}{15K\Omega}$.

$$\boxed{I_2 = 53.33\,\mu A}$$

* $R_1 = \frac{V_{sat} - V_{R2}}{I_2} = \frac{11 - 0.8V}{53.33\,\mu A} = 191.25\,K\Omega$

Choose $\boxed{R_1 = 180K\Omega}$



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Adjusting the Trigger points (UTP & LTP) :-

i) Schmitt Trigger with LTP = 0 :-

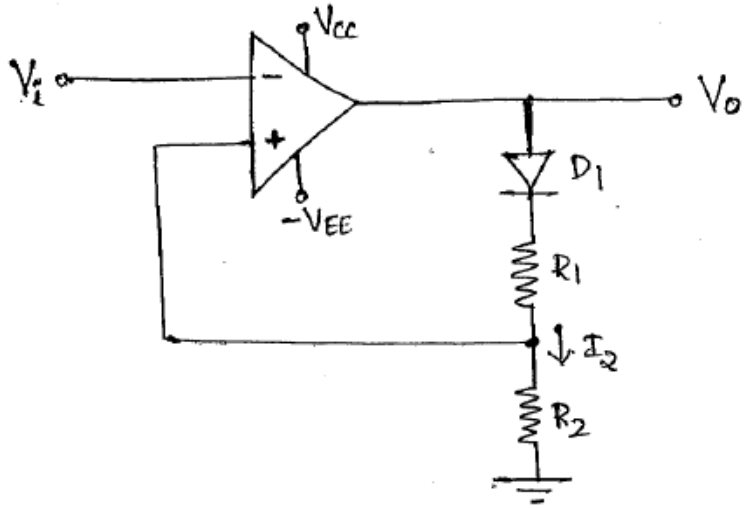

fig ① : Schmitt trigger ckt with LTP = 0

* fig ① shows the ckt with +ve UTP & zero LTP. This can be achieved by using a diode in series with R_1.

When the o/p is at $+V_{sat}$, the diode D_1 is forward biased and UTP will be equal to the voltage drop across the resistor R_2 (i.e. V_{ref} = UTP).

$$UTP = IR_2$$

$$\boxed{UTP = \frac{V_{sat} \cdot R_2}{R_1 + R_2}} \qquad \left(\text{where } \beta = \frac{R_2}{R_1 + R_2} \right)$$

* When the o/p is at $-V_{sat}$, the diode D_1 is reverse biased and only a very input bias current (I_B) flows through R_2 & the Non-INV terminal is held at ≈0V. thus LTP = 0.

* When the input voltage is reduced below ground level, the o/p will go to $+V_{sat}$.

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* The diode D_1 must be selected to have a maximum reverse voltage (PIV) greater than the circuit supply voltage.

* The maximum reverse recovery time 't_{rr}' should be much smaller than the minimum pulse width of the input signal i.e.

$$t_{rr} \leq \frac{\text{minimum pulse width}}{10}$$

ii) INV - SCHMITT trigger having different LTP & UTP :-

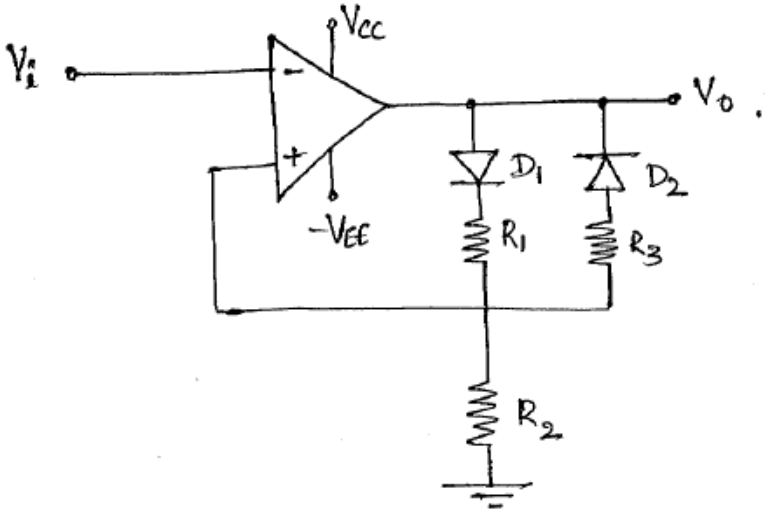

fig ①: schmitt trigger circuit with different LTP & UTP.

* The schmitt trigger ckt shown in fig ① uses two diodes D_1 & D_2 and three resistors R_1, R_2 & R_3 to get different LTP & UTP voltages.

Case 1: When $V_o = +V_{sat}$, the diode D_1 is forward biased and D_2 is reverse biased. The UTP is given by.

$$UTP = V_{R2} = \frac{R_2}{R_1 + R_2}\left[|V_o| - V_F\right]$$

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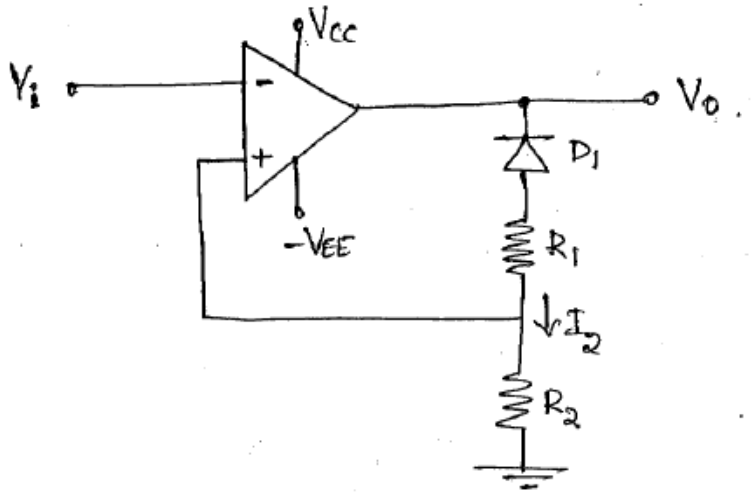
Case ii : When $V_o = -V_{sat}$, the diode D_1 is reverse biased and D_2 is forward biased. The LTP is given by.

$$LTP = V_{R2} = \frac{R_2}{R_3 + R_2} \left[|V_o| - V_F \right]$$

Where V_F is the voltage drop across D_1 & D_2.

* Different values of R_1 & R_2 gives different UTP & LTP voltages.

NOTE :- Schmitt trigger with UTP = 0 :-.



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UNEQUAL 'UTP' & LTP :-

FORMULAE

Let $I_2 = 500\mu A$

1) $R_2 = \dfrac{V_{R2}}{I_2}$

$V_{R2} = UTP$

$$R_2 = \frac{UTP}{I_2}$$

2) $V_{sat} = (V_{cc} - 1V)$

3) $-V_{sat} = (-V_{EE} + 1V)$

4) Assume $V_F = 0.7V$

5) $UTP = \dfrac{R_2}{R_1 + R_2} \left(|+V_{sat}| - V_F \right)$

Determine R_1.

6) $LTP = \dfrac{R_2}{R_3 + R_2} \left(|-V_{sat}| - V_F \right)$

Determine R_3.

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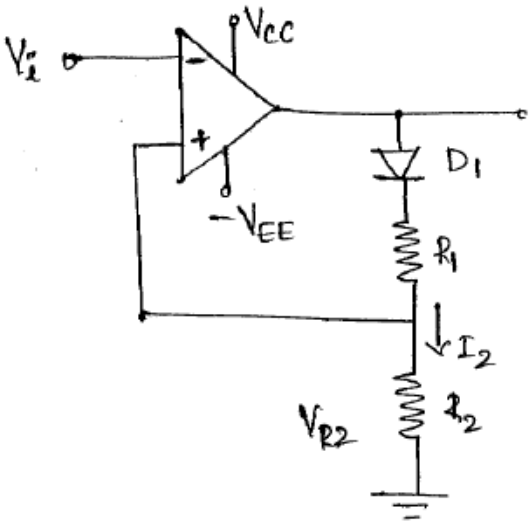
FORMULAE for LTP = 0 & UTP = +Ve Schmitt trigger.

1) Let $I_2 = 500\ \mu A$

2) $R_2 = \dfrac{V_{R2}}{I_2}$

Here $V_{R2} = UTP.$

$\therefore R_2 = \dfrac{UTP}{I_2}$



3) $R_1 = \dfrac{V_{R1}}{I_2}$

Applying KVL to o/p ckt

$$V_{sat} - V_F - I_2 R_1 - V_{R2} = 0$$

$$I_2 R_1 = V_{sat} - V_F - V_{R2}$$

$$R_1 = \frac{V_{sat} - V_F - V_{R2}}{I_2}$$

where

$+V_{sat} = (V_{CC} - 1V)$ &

$V_{R2} = UTP$

$$R_1 = \frac{[V_{CC} - 1] - V_F - UTP}{I_2}$$

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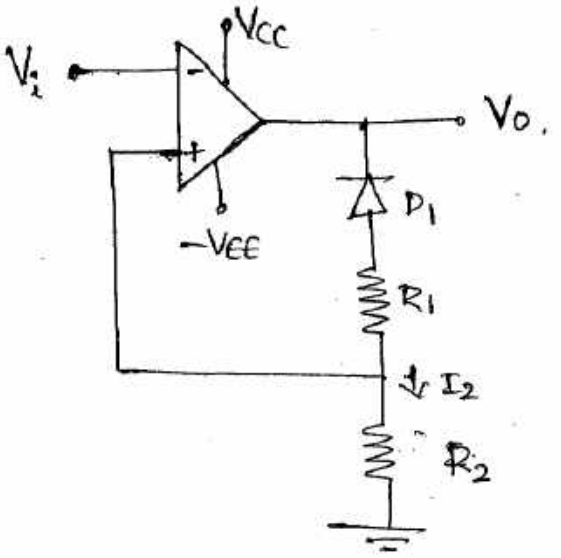
Formula for UTP = 0 & LTP = +Ve Schmitt trigger.



1) Let $I_2 = 500\ \mu A$

2) $R_2 = \frac{V_{R2}}{I_2}$

Here $V_{R2} = LTP$

$$R_2 = \frac{LTP}{I_2}$$

3) $R_1 = \frac{V_{R1}}{I_2}$

Applying KVL to o/p ckt

$$V_{sat} - V_F - I_2R_1 - V_{R2} = 0$$

$$V_{sat} - V_F - V_{R2} = I_2R_1$$

$$R_1 = \frac{V_{sat} - V_F - V_{R2}}{I_2}$$

$$V_{sat} = V_{cc} - 1V$$

$$V_{R2} = LTP$$

$$\therefore \quad R_1 = \frac{[V_{cc} - 1V] - V_F - LTP}{I_2}$$

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1) An INV schmitt trigger ckt is to have UTP = 0V & LTP = -1V. Design a suitable ckt using a bipolar op-amp and ±15V supply. June -08, 7M

Given: UTP = 0V, |LTP| = 1V, V_{CC} = 15V, $-V_{EE}$ = -15V.

Sol:

Assume $V_F = 0.7V$

* Let $I_2 = 500\,\mu A$ ← (1M)

* $R_2 = \frac{V_{R2}}{I_2}$.

$V_{R2} = LTP$

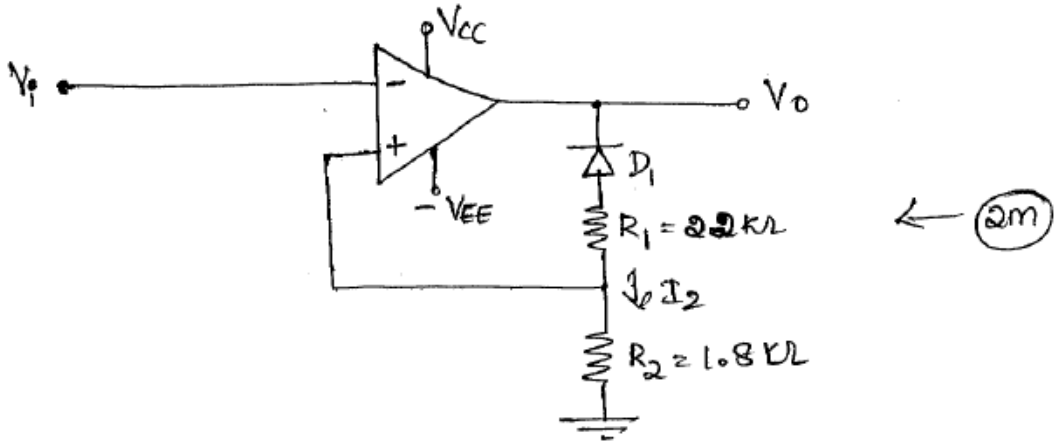
$R_2 = \frac{|LTP|}{I_2} = \frac{1V}{500\,\mu A} = 2K\Omega$, choose $R_2 = 1.8K\Omega$ ← (1m)

* Now I_2 becomes $I_2 = \frac{V_{R2}}{R_2} = \frac{1V}{1.8K\Omega}$

$I_2 = 555.5\,\mu A$ ← (1m)

* $R_1 = \frac{|-V_{EE}+1| - V_F - LTP}{I_2} = \frac{|-15+1| - 0.7V - 1V}{555.5\,\mu A}$

$R_1 = 22.14K\Omega$ ← (2m) Choose $R_1 = 22K\Omega$



← (2m)

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2) An INV schmitt trigger ckt is to have UTP = 0 & LTP = 2.5V. Design a suitable ckt using a bipolar op-amp & a ±18V supply. June -10, 8M

Given :- UTP = 0V, |LTP| = 2.5V, V_{CC} = 18V

$-V_{EE} = -18V$. Assume $V_F = 0.7V$

Sol :-

* Let $I_2 = 500\mu A$

* $R_2 = \frac{V_{R2}}{I_2} = \frac{|LTP|}{2} = \frac{2.5V}{500\mu A} = 5K\Omega$

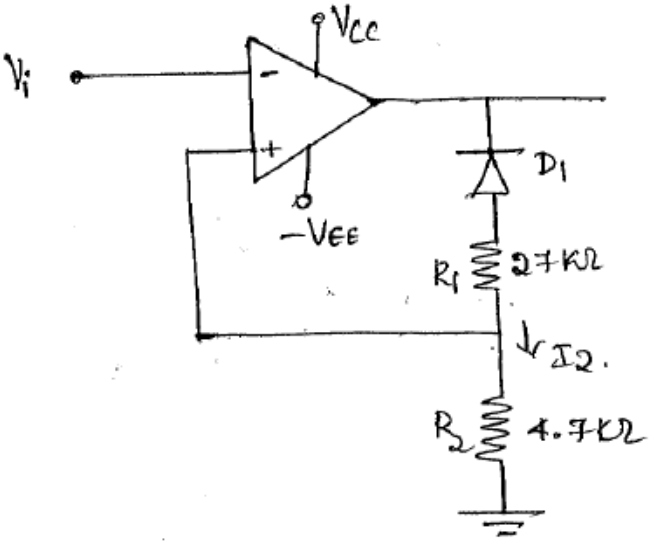
choose $R_2 = 4.7K\Omega$ ← (3m)

* Now I_2 becomes $I_2 = \frac{V_{R2}}{R_2} = \frac{2.5V}{4.7K\Omega}$

$I_2 = 532\mu A$

* $R_1 = \frac{|-V_{EE}+1| - V_F - |LTP|}{I_2} = \frac{17 - 0.7 - 2.5V}{532\mu A} = 25.9K\Omega$

choose $R_1 = 27K\Omega$ ← (3m)



← (2m)

ARUNKUMAR G M.Tech, Lecturer in E&CE Dept. S.T.J.I.T., Ranebennur.

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3) An INV schmitt trigger ckt is to have UTP = 2.5 V & LTP = 0. Design a suitable ckt using a bipolar and a ± 18V supply.

Given: UTP = 2.5V , LTP = 0V , V_{cc} = 18 V .

Assume V_F = 0.7 V.

Sol :-

* let $I_2 = 500\mu A$ $\quad$ $V_{R2} = UTP = 2.5V$

* $R_2 = \frac{V_{R2}}{I_2} = \frac{UTP}{I_2} = \frac{2.5V}{500\mu A} = 5K\Omega$

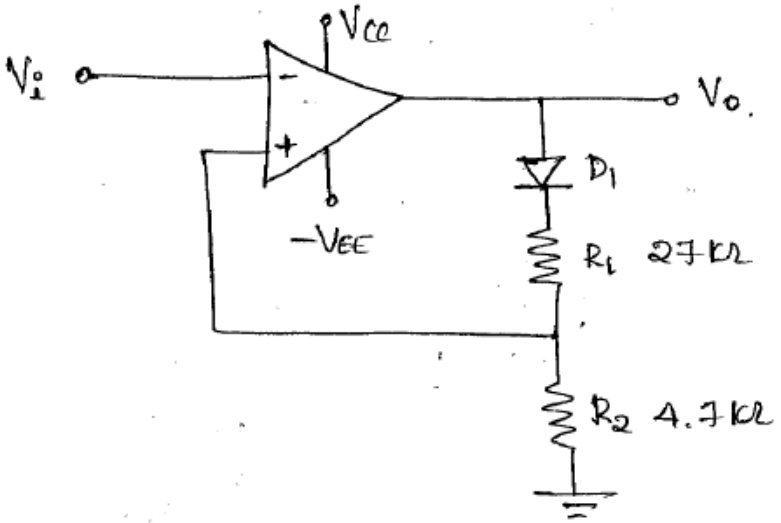
choose $R_2 = 4.7K\Omega$, Now $I_2 = \frac{V_{R2}}{R_2} = \frac{2.5V}{4.7K\Omega}$

$I_2 = 532\mu A$

* $R_1 = \frac{(V_{cc}-1) - V_F - V_{R2}}{I_2}$

$= \frac{17 - 0.7V - 2.5V}{532\mu A} = 25.9K\Omega$

choose $R_1 = 27K\Omega$



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4) An INV schmitt trigger ckt is to have UTP = 1V & LTP = 0V. Design a suitable ckt using a bipolar op-amp & ±15V supply.

Given:- UTP = 1V, LTP = 0V, V_{CC} = 15V

Sol:- Assume $V_F = 0.7V$

* Let $\boxed{I_2 = 500\,\mu A}$

* $\boxed{V_{R2} = UTP = 1V}$

* $R_2 = \frac{V_{R2}}{I_2} = \frac{1V}{500\,\mu A} = 2K\Omega$

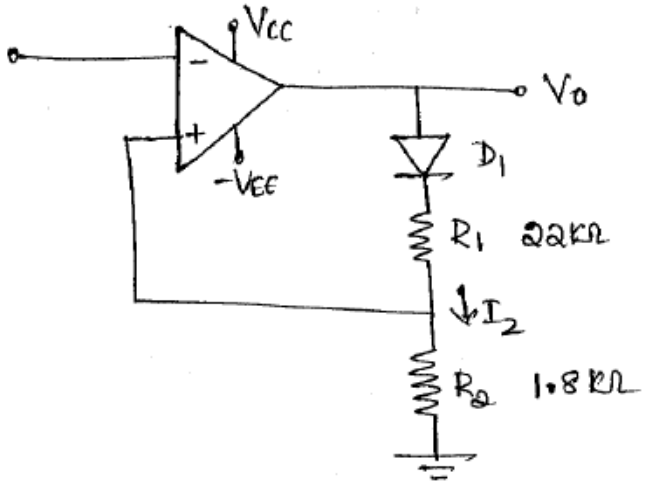
choose $\boxed{R_2 = 1.8\,K\Omega}$

* Now I_2 becomes $I_2 = \frac{V_{R2}}{R_2} = \frac{1V}{1.8V}$

$\boxed{I_2 = 555.5\,\mu A}$

* $R_1 = \frac{(V_{CC}-1) - V_F - V_{R2}}{I_2} = \frac{14 - 0.7V - 1V}{555.5\,\mu A}$

$\boxed{R_1 = 22.14\,K\Omega}$ choose $\boxed{R_1 = 22K\Omega}$



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1) Using a bipolar op-amp with ±18 volts supply, design an inverting schmitt trigger circuit to have UTP = 1.5V & LTP = −3V.

Given :- $V_{CC} = 18V$, $-V_{EE} = -18V$, $UTP = 1.5V$, $|LTP| = 3V$.

Assume $V_F = 0.7V$.

Sol :

$V_{R2} = UTP = 1.5V$.

$+V_{sat} = (V_{CC} - 1) = 17V$

$-V_{sat} = -V_{EE} + 1 = -18 + 1$.

$-V_{sat} = -17V$

* Let $\boxed{I_2 = 500\mu A}$

* $R_2 = \frac{V_{R2}}{I_2} = \frac{1.5V}{500\mu A} = 3K\Omega$

choose. $\boxed{R_2 = 2.7K\Omega}$

$$UTP = \frac{R_2 (+V_{sat} - V_F)}{R_1 + R_2}$$

$$1.5V = \frac{2.7K\Omega (17V - 0.7V)}{R_1 + 2.1K\Omega}$$

$$1.5R_1 + 4.05 \times 10^3 = 2.7K\Omega (16.3V)$$

$$1.5R_1 = 44.01 \times 10^3 - 4.05 \times 10^3$$

$$R_1 = \frac{39.96 \times 10^3}{1.5} = 26.64K\Omega$$

Choose $\boxed{R_1 = 27K\Omega}$

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* $|LTP| = \dfrac{R_2\ (|-V_{sat}| - V_\gamma)}{R_2 + R_3}$.

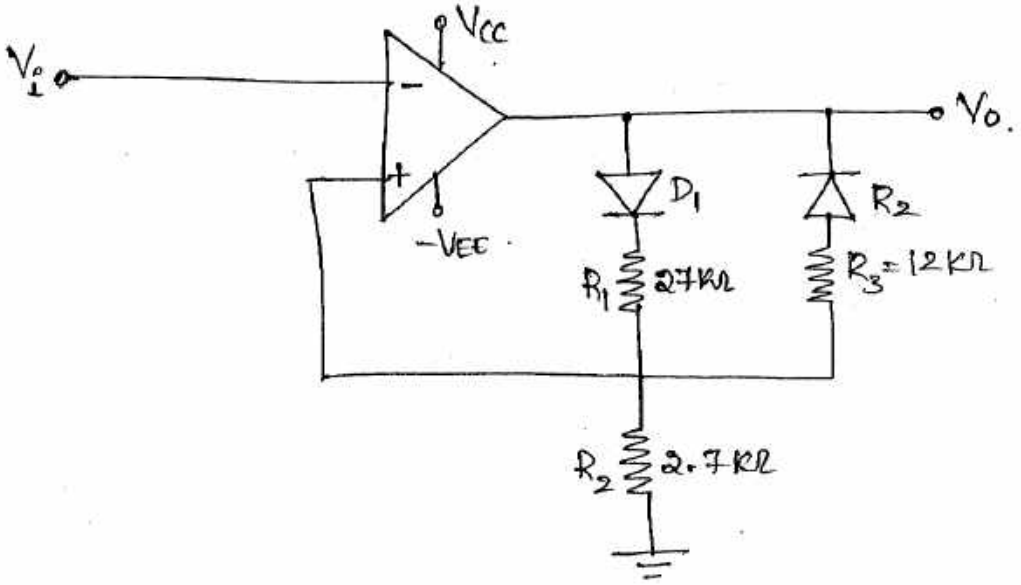
$3 = \dfrac{2.7K\Omega}{2.7K + R_3}\ (17 - 0.7V)$

$3R_3 + 8.1 \times 10^3 = 2.7K\Omega\ (16.3V)$

$3R_3 = 44.01 \times 10^3 - 8.1 \times 10^3$.

$R_3 = \dfrac{35.91 \times 10^3}{3.} = 11.97K\Omega$

choose. $\boxed{R_3 = 12K\Omega}$



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Astable Multivibrator :- (Free running Multivibrator)

1) Sketch the ckt of an op-amp astable multivibrator, show the voltage waveforms at various points in the ckt and explain its operation. **Dec-10, 6M**

Jan-09, 6M (EE)	Jan-10, 6M (EE)	June-08, 5m (EE)	Jan-06, 8M (EE)

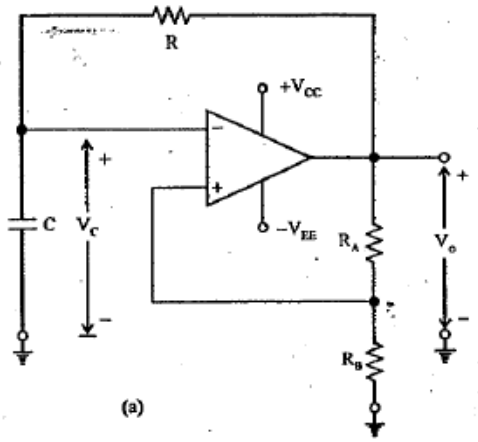
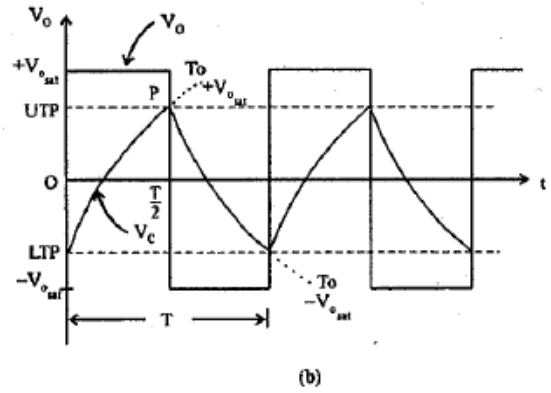


Fig. 6.31 : (a) Astable multivibrator circuit,



(b) Output voltage and capacitor voltage waveforms

* Astable multivibrator is also called as free-running multivibrator (∵ it has no I/p). The o/p voltage continuously switches between high & low levels without any I/p. It has no stable state.

* The op-amp resistors R_1 and R_2 constitutes an INV schmitt trigger circuit. The I/p voltage to the schmitt trigger circuit is the voltage across the capacitor C.

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Operation :

Let the capacitor voltage be initially zero i.e. $V_c = 0$ and let $V_0 = +V_{sat}$. Due to positive feedback, the potential at point B in fig ① is given by

$$V_B = \frac{R_2}{R_1 + R_2} V_{sat} = UTP$$

* The capacitor 'C' charges exponentially with a time constant equal to RC with a polarity '+' on top. When the capacitor voltage V_c just crosses the UTP voltage, the o/p V_0 rapidly changes from $+V_{sat}$ to $-V_{sat}$. Now o/p voltage $V_0 = -V_{sat}$. The voltage at point B is given by :

$$V_B = \frac{R_2}{R_1 + R_2} - V_{sat} = LTP$$

$V_c = -V_{sat}$ ↓

* Now the capacitor discharges to zero & starts charging in the reverse direction due to o/p V_0 being at $-V_{sat}$. The capacitor voltage increases negatively towards $-V_{sat}$. When V_c just crosses LTP voltage, the o/p V_0 rapidly changes from $-V_{sat}$ to $-V_{sat}$.

Thus producing a symmetrical square wave o/p V_0 as shown in fig ②.

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Design :-

* The minimum current flowing through R is chosen to be 100 times the op-amp input bias current $I_{B(max)}$.

$$I_1 = 100 \times I_{B(max)}$$

* The resistor R is then calculated as :

$$R = \frac{|V_o| - UTP}{I_1}$$

* The capacitance C_1 is

$$C = \frac{I_1 \times t}{\Delta V}$$

Where $t = T/2$ &

$\Delta V = UTP - LTP$

$$C = \frac{I_1 \times T/2}{(UTP - LTP)}$$

* For BIFET op-amp, the capacitor C_1 is first chosen to be much greater than stray capacitance.

---

* Explain the operation of an op-amp based astable multivibrator. Use relevant waveform.

Dec-10, 6M

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* Explain working of an op-amp based Astable multivibrator. Show that $T = 2RC \ln \frac{(1+\beta)}{(1-\beta)}$ where β is feedback ratio.

June-05, 8M(EE)

1st Explain Astable multivibrator

* The charging of capacitor is exponential & the capacitor voltage at any instant is given by:

$$V_{C1} = V_f + (V_i - V_f)\, e^{-t/\tau} \longrightarrow (1)$$

Where $\tau = RC$ time constant of charging.

V_f = final value of capacitor voltage.

$\therefore$ $V_f = +V_{sat}$ in the interval $0 < t < T/2$

V_i = Initial value of the capacitor voltage

$\therefore$ $V_i = -\frac{R_2}{R_1 + R_2} V_{sat}$

(where $\beta = \frac{R_2}{R_1 + R_2}$)

$$V_i = -\beta V_{sat}$$

Now eq (1) becomes.

$$V_{C1} = +V_{sat} + \left[-\beta V_{sat} - V_{sat}\right] e^{-\frac{t}{R_1 C_1}}$$

$$= +V_{sat} + \left[-V_{sat}(1+\beta)\right] e^{-\frac{t}{R_1 C_1}}$$

$$V_{C1} = +V_{sat}\left[1 - (1+\beta)\, e^{-t/R_1 C_1}\right] \longrightarrow (2)$$

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At $t = T/2$, $V_c = +\beta V_{sat}$

Now eq ② becomes

$$\beta V_{sat} = V_{sat}\left[1-(1+\beta)\,e^{-\frac{T}{2RC}}\right]$$

$$\beta = 1-(1+\beta)\,e^{-\frac{T}{2RC}}$$

$$(1+\beta)\,e^{-\frac{T}{2RC}} = 1-\beta.$$

$$\boxed{e^{-\frac{T}{2RC}} = \frac{(1-\beta)}{(1+\beta)}} \rightarrow ③$$

Taking natural log on bothsides of eq ③, we get,

$$-\frac{T}{2RC} = \ln.\frac{(1-\beta)}{(1+\beta)}$$

$$T = -2RC\,\ln\left(\frac{1-\beta}{1+\beta}\right)$$

$$\boxed{T = +2RC\,\ln\left(\frac{1+\beta}{1-\beta}\right)} \rightarrow ④$$

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* For a astable multivibrator, show that frequency of o/p waveform is $f = \frac{1}{2RC}$ for a symmetric o/p square wave. Show the ckt.

June - 09, 7M(EE)

Sol:-

* The charging of capacitor is exponential & the capacitor voltage at any instant is given by:

$$V_{C1} = V_f + (V_i - V_f)\, e^{-t/\tau} \longrightarrow (1)$$

Where $\boxed{\tau = RC}$ time constant of charging.

V_f = final value of capacitor voltage.

$\therefore \boxed{V_f = +V_{sat}}$ in the interval $0 < t < T/2$

V_i = Initial value of the capacitor voltage

$$\therefore V_i = -\frac{R_2}{R_1 + R_2} V_{sat}$$

$$\left(\text{where } \beta = \frac{R_2}{R_1 + R_2}\right)$$

$$\boxed{V_i = -\beta V_{sat}}$$

Now eq (1) becomes.

$$V_{C1} = +V_{sat} + \left[-\beta V_{sat} - V_{sat}\right] e^{-\frac{t}{R_1 C_1}}$$

$$= +V_{sat} + \left[-V_{sat}(1+\beta)\right] e^{-\frac{t}{R_1 C_1}}$$

$$V_{C1} = +V_{sat}\left[1 - (1+\beta)\, e^{-t/R_1 C_1}\right] \longrightarrow (2)$$

At $t = T/2$, $V_c = +\beta V_{sat}$

Now eq (2) becomes

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$$\beta V_{sat} = V_{sat}\left[1-(1+\beta)\,e^{-\frac{T}{2RC}}\right]$$

$$\beta = 1-(1+\beta)\,e^{-\frac{T}{2RC}}$$

$$(1+\beta)\,e^{-\frac{T}{2RC}} = 1-\beta.$$

$$\boxed{e^{-\frac{T}{2RC}} = \frac{(1-\beta)}{(1+\beta)}} \rightarrow (3)$$

Taking natural log on bothsides of eq (3), we get,

$$-\frac{T}{2RC} = \ln.\frac{(1-\beta)}{(1+\beta)}$$

$$T = -2RC\,\ln\left(\frac{1-\beta}{1+\beta}\right)$$

$$\boxed{T = +2RC\,\ln\left(\frac{1+\beta}{1-\beta}\right)} \rightarrow (4)$$

Now if $\beta = 0.47$ in eq (4), then

$$T = 2RC\,\ln\left(\frac{1+0.47}{1-0.47}\right)$$

$$T = 2RC\,\ln(2.77)$$

$$T = 2RC(1)$$

$$T = 2RC$$

$$\boxed{f = \frac{1}{2RC}}$$

WKT $\boxed{f = \frac{1}{T}}$

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FORMULAE :-

Astable Multivibrator

1) Let $I_1 = 100 \times I_{B(max)}$.

2) $R_2 = \frac{V_{R2}}{I_1}$.

3) $R_1 = \frac{V_{sat} - V_{R2}}{I_1}$

4) $R = \frac{V_{sat} - UTP}{I_1}$.

5) $C = \frac{I_1 \times t}{\Delta V}$

Where $t = T/2$

$\Delta V = UTP - LTP$

6) $f = \frac{1}{2RC}$

7) $T = 2RC \ln\left(\frac{1+\beta}{1-\beta}\right)$

Where $\beta = \frac{R_2}{R_1 + R_2}$

8) $T = T_{ON} + T_{OFF}$

$$\boxed{f = \frac{1}{T}}$$

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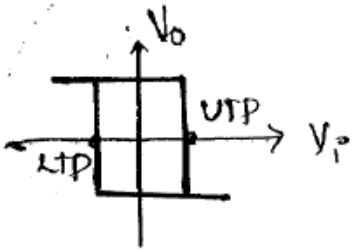
1) Design an Astable multivibrator that can produce an op with $t_{ON} = t_{OFF} = 1$ msec. The op-amp is driven with a ±15V supply. Draw waveforms across capacitor, feedback and output. The hysteresis should not exceed 0.1 V.

Jan-09, 6M

Given:-

$V_H = 0.1$ V

UTP − LTP = 0.1V



If UTP = LTP = $\frac{0.1V}{2} = 0.05V$.

$t_{ON} = t_{OFF} = 1$msec

$V_{CC} = 15V$, $-V_{EE} = -15V$

$V_{sat} = (V_{CC} - 1) = 15V - 1V = 14V$

Sol:- for 741 op-amp: $I_{B(max)} = 500nA$

$V_{R2} = UTP = 0.05V$.

* Let $I_1 = 100 \times I_{B(max)} = 100 \times 500nA$

$I_1 = 50\mu A$

* $R_2 = \frac{V_{R2}}{I_1} = \frac{UTP}{50\mu A} = \frac{0.05V}{50\mu A}$

$R_2 = 1K\Omega$.

* $R_1 = \frac{V_{sat} - V_{R2}}{I_1} = \frac{14V - 0.05V}{50\mu A} = 279K\Omega$

Choose $R_1 = 270K\Omega$

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* $R = \frac{V_{sat} - UTP}{I_1} = \frac{14V - 0.05V}{50\,\mu A} = 279K\Omega$

choose $\boxed{R = 270K\Omega}$

* $C = \frac{I_1 \times t}{\Delta V}$

$t = T/2$

$T = t_{ON} + t_{OFF} = 1msec + 1msec = 2msec$

$t = \frac{T}{2} = \frac{2msec}{2}$

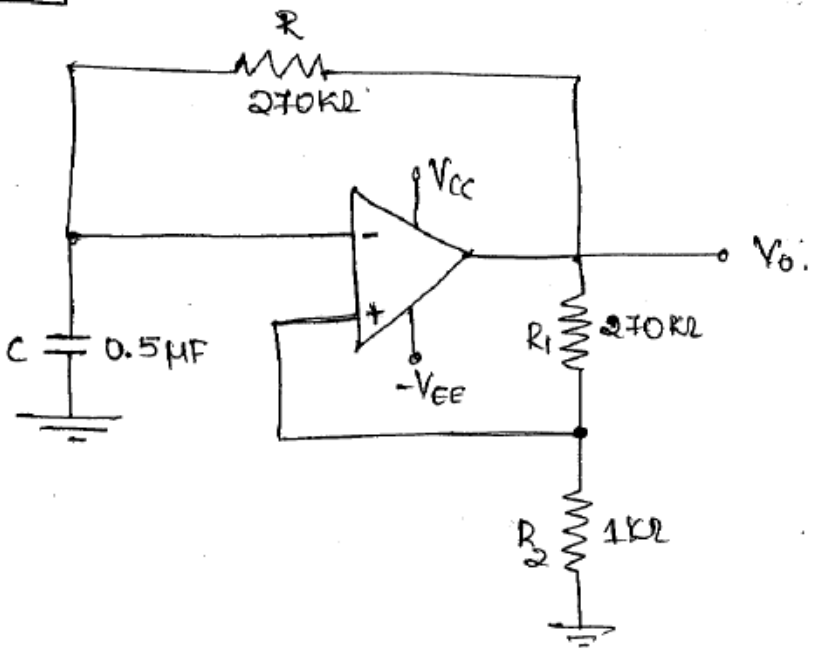
* $\boxed{t = 1msec}$

* $\Delta V = UTP - LTP = 0.05V - (-0.05V)$

$\boxed{\Delta V = 0.1V}$

$C = \frac{50\,\mu A \times 1msec}{0.1V}$

$\boxed{C = 0.5\,\mu F}$



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2) An op-amp astable multivibrator circuit is to have a 4 KHz. output with an amplitude of ±14 volts using a ±15 V supply. Using a bipolar op-amp, design a suitable ckt.

Given :- $f = 4\,KHz$, $\pm V_{sat} = \pm 14\,V$

Sol :- Assuming $UTP = |LTP| = 0.5\,V$

for 741 op-amp $\boxed{I_{B(max)} = 500\,nA}$

* $V_{R2} = UTP = 0.5\,V$

$\Delta V = UTP - LTP = 0.5\,V - (-0.5\,V)$

$\boxed{\Delta V = 1\,V}$

* $T = \frac{1}{f} = \frac{1}{4\,KHz} = \underline{250\,\mu sec}$

$t = \frac{T}{2} = \frac{250\,\mu sec}{2}$

$\boxed{t = 125\,\mu sec}$

* Let $I_1 = 100 \times 500\,nA$

$\boxed{I_1 = 50\,\mu A}$

* $R_2 = \frac{V_{R2}}{I_1} = \frac{UTP}{50\,\mu A} = \frac{0.5\,V}{50\,\mu A} = 10\,K\Omega$

$\boxed{R_2 = 10\,K\Omega}$

* $R = R_1 = \frac{V_{sat} - V_{R2}}{I_1} = \frac{14\,V - 0.5\,V}{50\,\mu A} = \underline{270\,K\Omega}$

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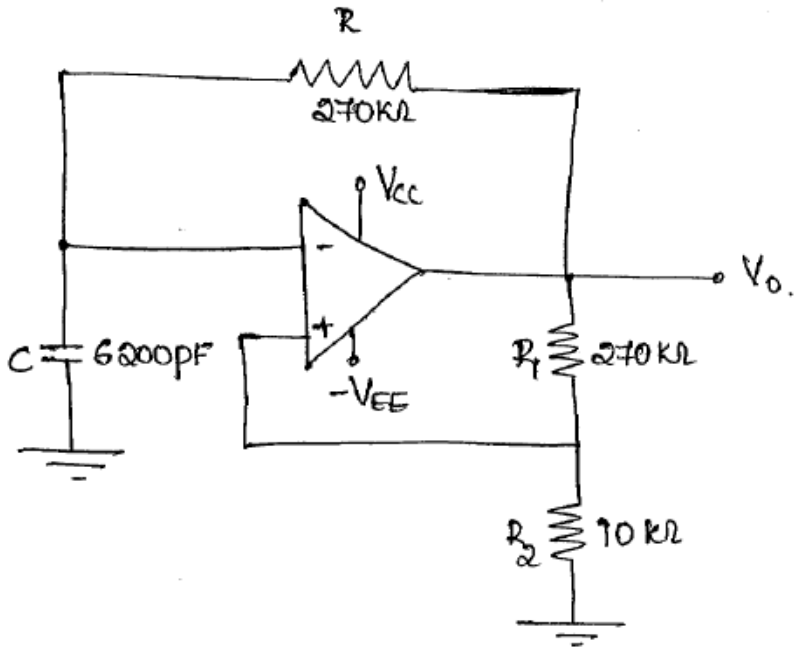
* $C = \frac{I_1 \times t}{\Delta V} = \frac{50\mu A \times 125\ \mu sec}{1V} = 6250\ pF.$

choose. **C = 6200pF**



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Design of Astable multivibrator using BIFET op-amp:

1) Select UTP & LTP $\ll V_0$.

Let $|UTP| = |LTP| = 0.5\,V$

2) $V_{CC} = (V_0 + 1V)$

3). For BIFET select $\boxed{R_1 = 1M\Omega}$

4). $I_2 = \dfrac{|V_0| - UTP}{R_1}$.

5) $R_2 = \dfrac{V_{R2}}{I_2}$.

6) Let $\boxed{C = 0.1\mu F}$

7) $t = \dfrac{1}{2f}$

8) $C = \dfrac{I_1 t}{\Delta V}$

$I_1 = \dfrac{C \cdot \Delta V}{t}$

Where $\Delta V = (UTP - LTP)$

9) $R = \dfrac{V_0 - UTP}{I_1}$

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1) Using a BIFET op-amp, design an astable multivibrator to have a $\pm 9V$ output with a frequency of 1KHz.

Given : $V_0 = \pm 9V$, $f = 1KHz$

Sol :

* select UTP & LTP $<< V_0$.

  Let $|UTP| = |LTP| = 0.5\,V$.

  Let $\boxed{R_1 = 1M\Omega}$

* $I_2 = \dfrac{|V_0| - UTP}{R_1} = \dfrac{9V - 0.5V}{1M\Omega}$

  $\boxed{I_2 = 8.5\,\mu A}$

* $R_2 = \dfrac{V_{R2}}{I_2} = \dfrac{UTP}{I_2} = \dfrac{0.5V}{8.5\,\mu A} = 59K\Omega$

  choose $\boxed{R_2 = 56K\Omega}$

* Let $\boxed{C = 0.1\,\mu F}$

* $t = \dfrac{1}{2f} = \dfrac{1}{2 \times 1KHz}$.

  $\boxed{t = 500\,\mu sec}$

  $\Delta V = UTP - (-LTP) = 0.5V - (-0.5V)$

  $\boxed{\Delta V = 1V}$

* $I_1 = \dfrac{C\Delta V}{t} = \dfrac{0.1\,\mu F \times 1V}{500\,\mu sec} = \underline{200\,\mu A}$.

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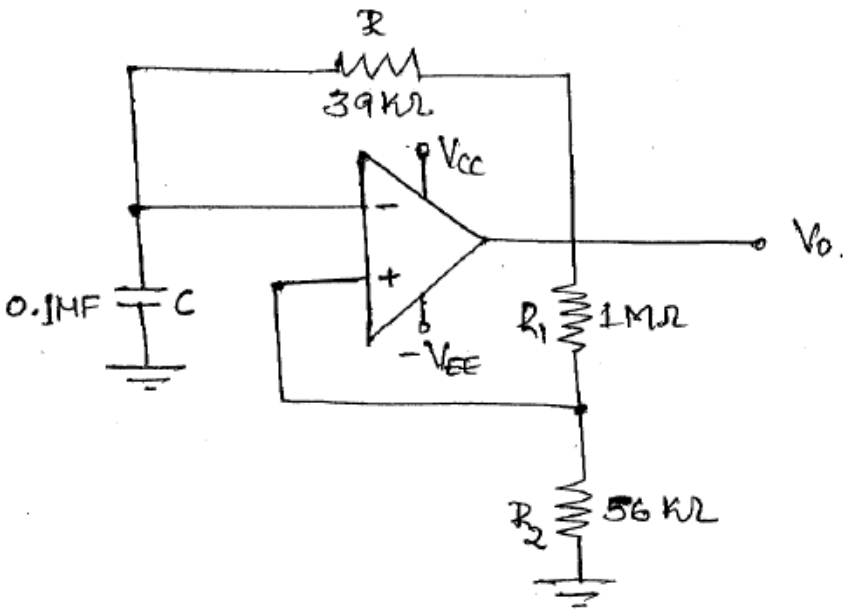
* $R = \frac{V_o - UTP}{I_1}$

$= \frac{9V - 0.5V}{200\mu A}$

$R = 42.5K\Omega$

choose. $R = 39K\Omega$



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Monostable Multivibrator :-

1) Draw the ckt of an op-amp monostable multivibrator & explain its operation — June-08, 7M

2) With a neat ckt diagrams & waveforms derive an expression for pulse width of monostable multivibrator using op-amp. — Model-1, 8M

June-10, 10M(EE) | June-09, 7M(EE) | June-07, 8M(EE) | Jan-05, 8M(EE)

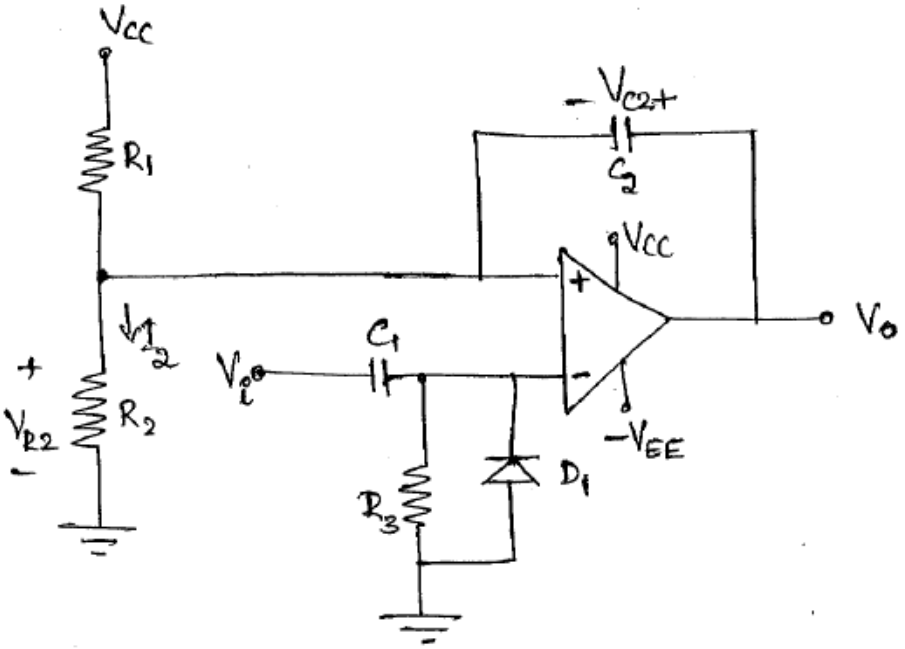

Fig
Bell → 230

fig ①: Monostable multivibrator and ckt waveforms.

* A monostable multivibrator has only one stable o/p state. In this stable state, the o/p voltage may be high or low, and it remains in this state until the multivibrator is triggered.

Operation :-

Before the application of trigger pulse, the INV input terminal of op-amp is grounded through resistor R_3. The Non-INV terminal is connected to voltage divider ckt of R_1 & R_2 connected to $+V_{CC}$.

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* The voltage V_{R2} across R_2 at Non-INV terminal is higher than INV terminal voltage & the o/p voltage is held at $+V_{sat}$ and capacitor C_2 is charged with the polarity shown in fig ①.

* The I/p positive trigger pulse is now applied to the differentiating circuit of R_3 & C_1 to produce positive and negative spikes at the op-amp INV terminal as shown in fig 1.

* The negative spike is clipped at −0.7V by diode D_1, so that it has no effect on the circuit.

The +ve spike rises the voltage at the INV I/p terminal beyond that at the Non-INV terminal and op-amp o/p switches to $-V_{sat}$.

* The spikes has a relatively short time duration, so the INV I/p terminal quickly returns to the zero voltage level.

When o/p goes to $-V_{sat}$, the Non-INV I/p terminal voltage is held at a -ve potential of

$$V_t = -V_{sat} - V_{C2}$$

* Now capacitor C_2 discharges via R_1 and R_2 thus gradually raising the Non-INV I/p terminal toward ground level. When the Non-INV terminal voltage goes slightly above ground, the op-amp o/p immediately switches back to $+V_{sat}$. & the ckt is returned to its original state.

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* The ckt produces a negative going o/p pulse each time it is triggered. The pulse width (PW) of the o/p depends on C_2, V_{R2} & the resistance of R_1 & R_2.

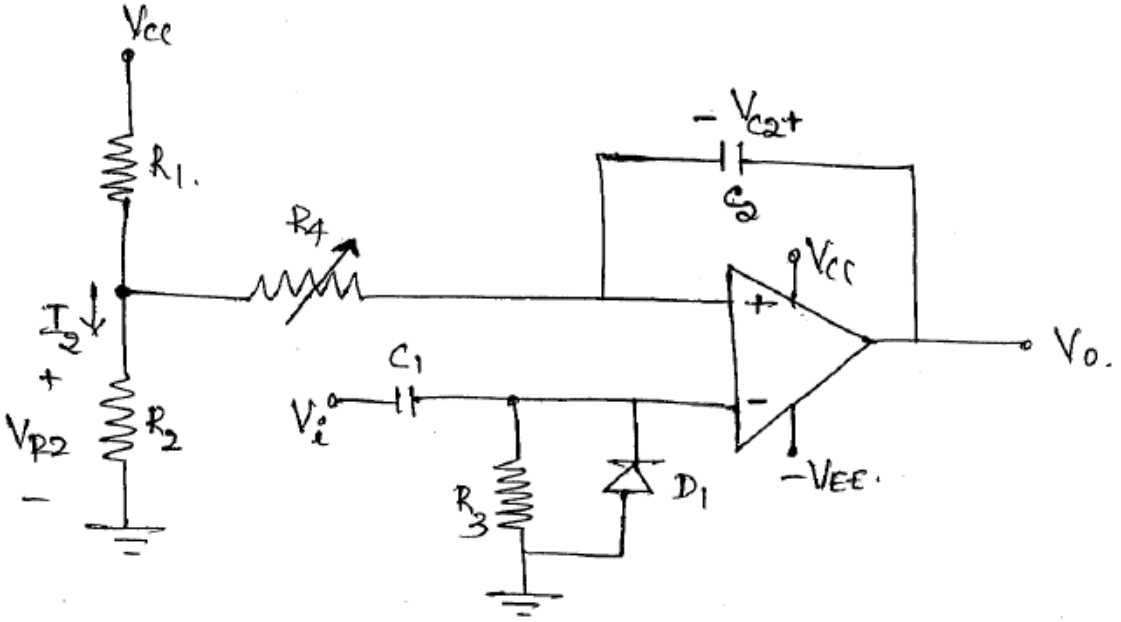

fig ② Modification to provide pulse-width adjustment.

* To control the pulse width (PW) a resistor R_4 can be included in the ckt as shown in fig ②.

The total resistances in series with the capacitor is now $(R_4 + R_1 \| R_2)$. Usually, R_4 is selected to be much larger than $(R_1 \| R_2)$. So that the capacitor charge/discharge resistance is effectively R_4.

* By adjusting R_4, the charge/discharge time can be altered thus controlling the o/p pulse width.

Design :-

1) Let $I_2 = 100 \times I_{B(max)}$

2) The voltage V_{R2} is chosen to be in the range 0.5 to 1 volts.

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$$R_2 = \frac{V_{R2}}{I_2}.$$

3) Determine R_1.

Applying KVL from V_{CC}, R_1 & R_2

$$V_{CC} - I_2 R_1 - I_2 R_2 = 0.$$

$$V_{CC} - I_2 R_2 - V_{R2} = 0$$

$$I_2 R_2 = V_{CC} - V_{R2}$$

$$\boxed{R_2 = \frac{V_{CC} - V_{R2}}{I_2}}$$

4) To design the differentiator ckt, the time constant $R_3 C_1$ is assumed to be 10% of input pulse width 't' to generate suitable spikes from the pulses.

$$R_3 C_1 = 10\% \text{ of } t$$

$$R_3 C_1 = 0.1\, t$$

$$\boxed{C_1 = \frac{0.1\, t}{R_3}}$$

Or. C_1 might be first selected much larger than stray capacitance then R_3 can be calculated from below equation. i.e. $\boxed{R_3 = \frac{0.1\, t}{C_1}}$

* $\boxed{R_3 = \frac{0.1\, V_{BE}}{I_{B(max)}}}$

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* The capacitance C_2 is given by.

$$C_2 = \frac{PW}{(R_1 \| R_2) \ln\left[(E - E_0)/(E - e_c)\right]}$$

Where PW → desired o/p pulse width

E → capacitor charging voltage &

E_0 → initial capacitor voltage before Triggering

* $E = V_{R2} + V_{sat}$

* $E_0 = V_{R2} - V_{sat}$

* The final capacitor voltage e_c is

$$\boxed{e_c = V_{sat}}$$

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1) Design a monostable multivibrator circuit to have an o/p pulse width of 1msec when triggered by a 2V, 100 μsec input pulse. Use a 741 op-amp with a ±12V supply.

Given: $V_{cc} = 12V$, $PW = 1msec$

$V_{sat} = (V_{cc} - 1V) = (12V - 1V)$

$\boxed{V_{sat} = 11V.}$ (or) $\boxed{-V_{sat} = -11V}$

$V_i = 2V$, $t = 100\mu sec.$

Sol:- For 741 op-amp: $I_{B(max)} = 500nA$.

* Let $\boxed{V_{R2} = 0.5V}$

* Let $I_2 = 100 \times I_{B(max)} = 100 \times 500nA$

$\boxed{I_2 = 50\mu A}$

* $R_2 = \frac{V_{R2}}{I_2} = \frac{0.5V}{50\mu A}$

$\boxed{R_2 = 10K\Omega}$

* $R_1 = \frac{V_{cc} - V_{R2}}{I_2} = \frac{12V - 0.5V}{50\mu A} = 230K\Omega$

Choose, $\boxed{R_1 = 220K\Omega}$

* $E = V_{R2} + V_{sat} = 0.5V + 11V$

$\boxed{E = 11.5V}$

* $E_0 = V_{R2} - V_{sat} = 0.5V - 11V$

$\boxed{E_0 = -10.5V}$

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* $e_c = V_{sat}$

$$\boxed{e_c = 11V}$$

* $$C_2 = \frac{PW}{(R_1 \| R_2)\ln\left[\frac{(E-E_0)}{(E-e_c)}\right]} = \frac{1\ msec}{(220K \| 10K)\ln\left[\frac{11.5V-(-10.5V)}{11.5V-11V}\right]}$$

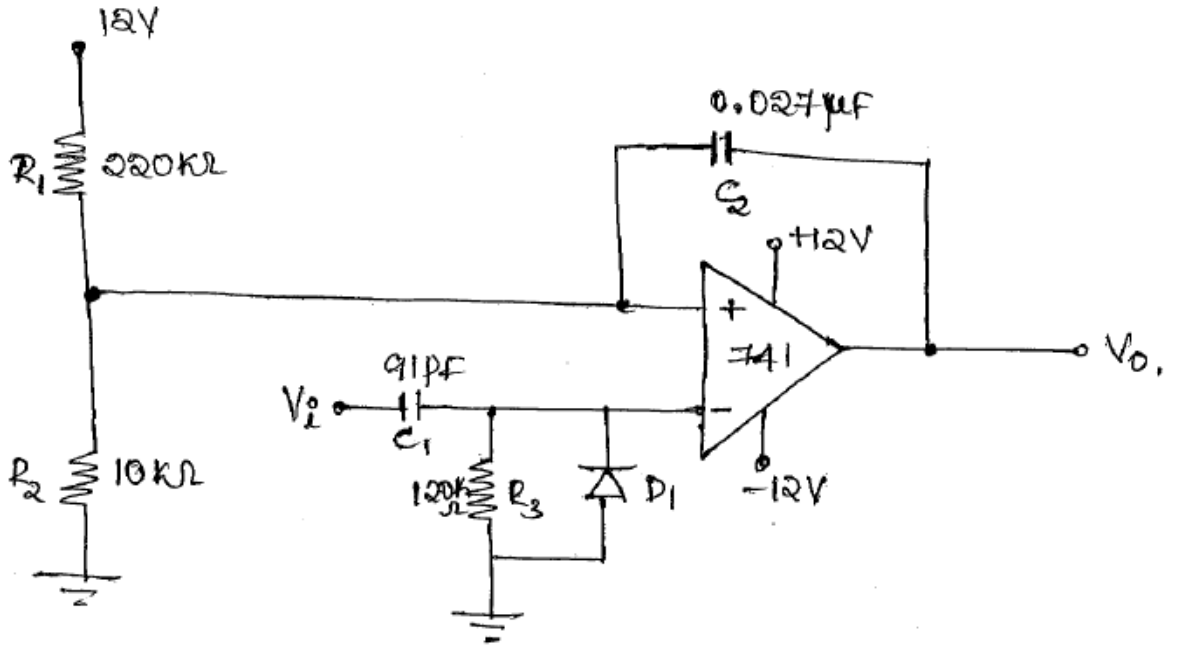
$$\boxed{C_2 = 0.027\ \mu F}$$

* $$R_{3(max)} = \frac{0.1\,V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7V}{500nA} = 140K\Omega$$

Choose $\boxed{R_{3(max)} = 120K\Omega}$

* $$C_1 = \frac{0.1t}{R_3} = \frac{0.1 \times 100\ \mu sec}{120K\Omega} = 83pF$$

Choose. $\boxed{C_1 = 91pF}$



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Filters :

Filters are circuits that pass only a desired band of frequencies & attenuates the undesired band of frequencies.

The filters are classified as :

1) Low pass filter.
2) High pass filter.
3) Band pass filter and
4) Band elimination or band reject or Band stop filter.

Filters can be of passive or active type. passive filters use only passive components such as resistors, capacitors & inductors.

Active filters use transistor or op-amps together with passive components. Active filters are further defined in terms of rate at which o/p falls off at the edge of the frequency range.

* If the fall off rate is 20dB/decade, the filters are called as first order filters.

If the fall off rate is 40dB/decade, the filters are called as Second order filters.

If the fall off rate is 60dB/decade, the filters are called as third order filters.

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Advantages of active filters over passive filters :-

1) What are the advantages of active filters over passive filters ? June - 10, 4M

1) Because of high input impedance & low o/p impedance of op-amp, the active filter does not cause loading of the source or load.

2) Active filters are more economical because of absence of inductors. (Inductors are bulky, costly & dissipate more power).

3) Due to availability of modern ICs, a variety of cheaper op-amps are available.

4) The op-amp gain can be easily controlled in the closed loop fashion, hence active filter input signal is not attenuated.

5) The active filter is easier to tune or adjust to any frequency compared to passive filters.

6) Active filters has excellent isolation between source and load.

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First order Low pass Active filter :-

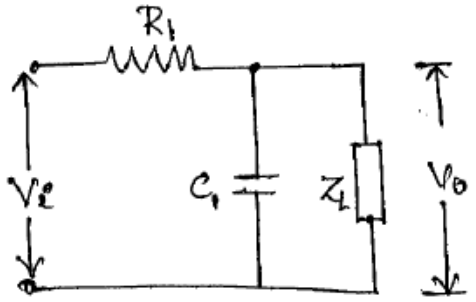
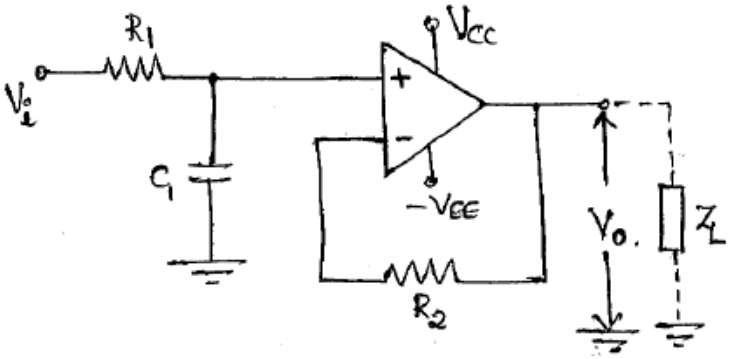


fig @ : passive low-pass filter.

A passive low pass filter ckt consisting of a resistor & a capacitor is shown in fig @. The filter load 'Z_L' is connected in parallel with a capacitor C_1.

Unless $Z_L \gg X_{C1}$, the load is likely to affect the filter performance.



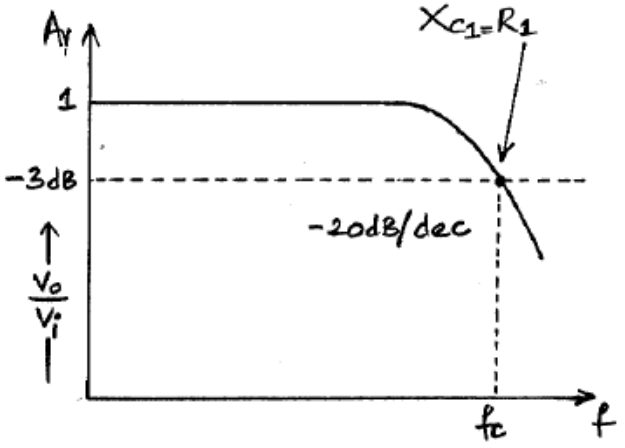


fig (b) : Active low-pass filter.

* Connecting a voltage follower to ckt of fig @ eliminates the load problem and converts the circuit into an active filter.

* The o/p voltage V_o of the active filter is given by : from fig @.

$$V_o = I \times (-jX_{C1})$$

$$= \frac{V_i}{R_1 - jX_{C1}} \cdot -jX_{C1}.$$

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Taking magnitude, $V_o = V_i \cdot \frac{\sqrt{X_{C1}^2}}{\sqrt{R_1^2 + X_{C1}^2}} = V_i \cdot \frac{X_{C1}}{\sqrt{R_1^2 + X_{C1}^2}}$

$$\boxed{\frac{V_o}{V_i} = \frac{X_{C1}}{\sqrt{R_1^2 + X_{C1}^2}}} \rightarrow (1)$$

* At low frequencies, $X_{C1} \gg R_1$, so eq (1) gives the gain as approximately 1.

* At higher frequencies, $X_{C1} \approx R_1$, the gain decreases. The frequency at which the o/p voltage is down by 3 dB from its pass frequency is defined as cut-off frequency 'f_c' of the filter.

* In fig (c), f_c is the frequency at which $X_{C1} = R_1$

Now eq (1) becomes

$$\boxed{A_V = \frac{V_o}{V_i} = \frac{1}{\sqrt{2}}}$$

$$\left\{ \because \frac{V_o}{V_i} = \frac{X_{C1}}{\sqrt{R_1^2 + X_{C1}^2}} = \frac{X_{C1}}{\sqrt{X_{C1}^2 + X_{C1}^2}} \right.$$

$$= \frac{X_{C1}}{\sqrt{2 X_{C1}^2}} = \frac{X_{C1}}{X_{C1}\sqrt{2}}$$

$$\left. \frac{V_o}{V_i} = \frac{1}{\sqrt{2}}. \right\}$$

* At frequencies higher than f_c, the gain of the ckt falls off at a rate of 20 dB / decade i.e. a fall of 20 dB each time the frequency is increased by a factor of 10.

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Design steps :-

1) $R_1 = \frac{0.1\, V_{BE}}{I_{B(max)}}$

2) $R_1 = R_2$

3) $X_{C1} = R_1$ at f_c.

$\frac{1}{2\pi f_c C_1} = R_1$.

$$C_1 = \frac{1}{2\pi f_c R_1}$$

1st order active loco pass active filter :-

FORMULAE :-

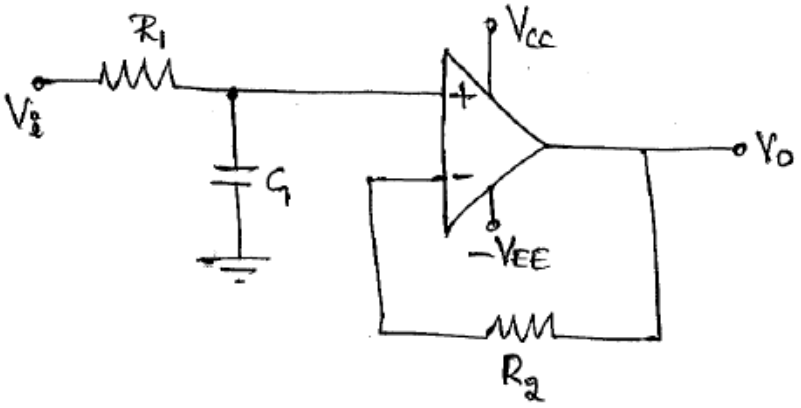
1) $R_1 = \frac{0.1\, V_{BE}}{I_{B(max)}}$

2) $R_1 = R_2$

3) $X_{C1} = R_1$ at f_c.

$\frac{1}{2\pi f_c C_1} = R_1$.

$$C_1 = \frac{1}{2\pi f_c R_1}$$



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1) Using a 741 op-amp, design a first-order active low pass filter to have a cut off frequency of 1KHz.

Given: $f_c = 1\,KHz$.

Sol:- For op-amp 741: $I_{B(max)} = 500nA$

Assume $V_{BE} = 0.7\,V$

* $R_1 = \frac{0.1 V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7V}{500nA}$

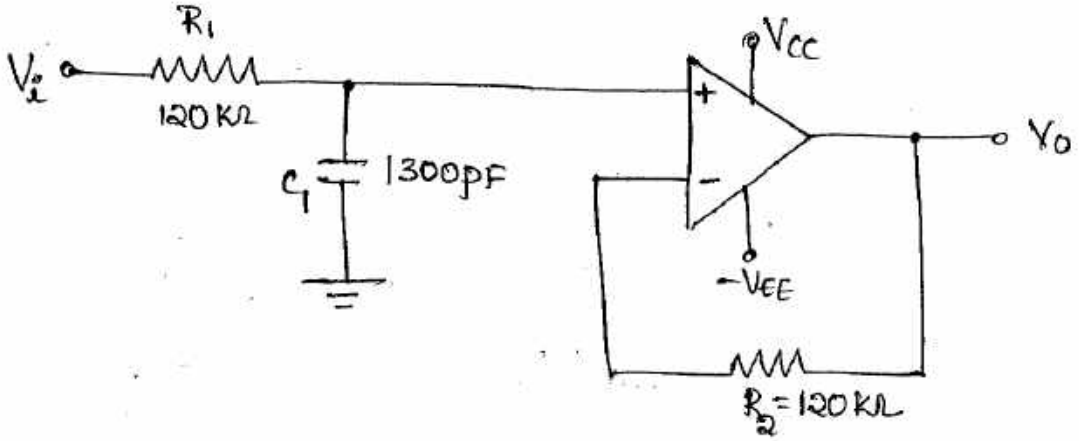
$R_1 = 140\,K\Omega$

choose $\boxed{R_1 = 120\,K\Omega}$

* $\boxed{R_2 = R_1 = 120K\Omega}$

* $C_1 = \frac{1}{2\pi f_c R_1} = \frac{1}{2\pi \times 1KHz \times 120K\Omega} = \underline{1326\,pF}$

choose $\boxed{C_1 = 1300pF}$



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2) Design a first order active low pass filter using 715 op-amp having a cut-off frequency of 4KHz. [$I_{B(max)} = 1.5\,\mu A$ for 715 op-amp].

Given: $f_c = 4KHz$, $I_{B(max)} = 1.5\,\mu A$

Assume: $V_{BE} = 0.7V$

Sol:-

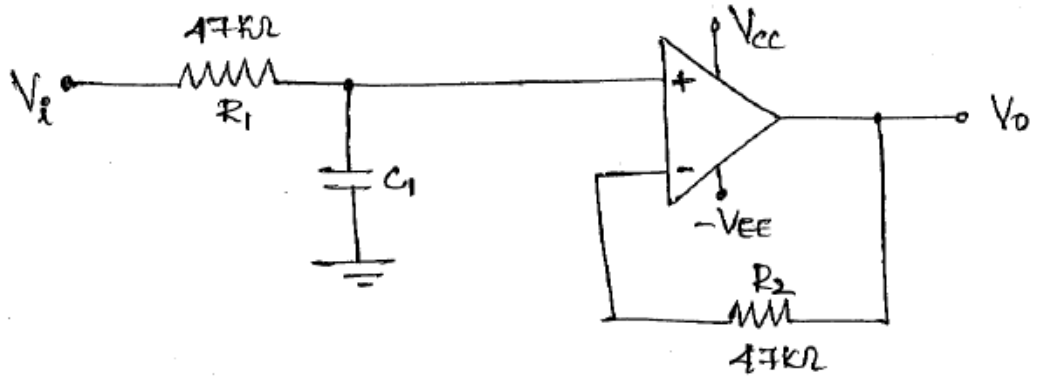
* $R_1 = \frac{0.1 V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7V}{1.5\,\mu A} = 46.67\,K\Omega$

choose $\boxed{R_1 = 47K\Omega}$

* $\boxed{R_2 = R_1 = 47K\Omega}$

* $C_1 = \frac{1}{2\pi f_c R_1} = \frac{1}{2\pi \times 4KHz \times 47K\Omega} = 846.57\,pF.$

Choose. $\boxed{C_1 = 820pF}$



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Second order low-pass active filter :-

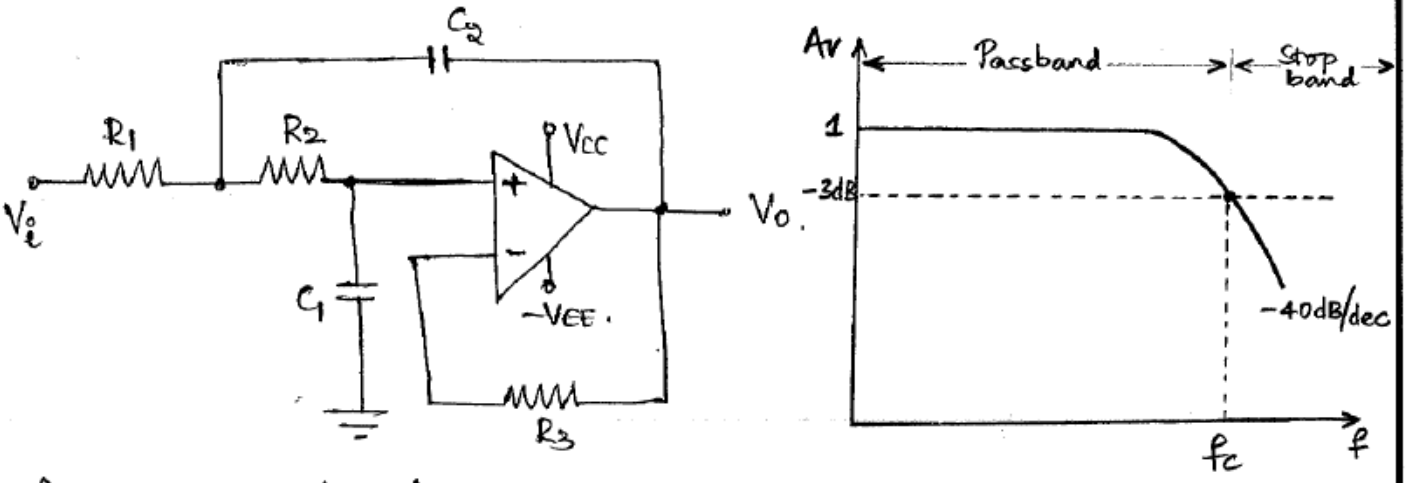

fig @ : Second order LPF ckt.

* In first-order low pass filter after cutoff freq the voltage gain decreases at the rate of 20dB/decade.

{ * In second-order low pass filter, after cut-off frequency, the voltage gain decreases at the rate of 40 dB/decade. }

* Fig @ shows a second order low pass filter, which has a frequency response that falls off at the rate of 40 dB per decade above the upper cut-off frequency.

* This stepper roll-off rate is achieved by using the C_1R_2 together with feedback from the o/p via capacitor C_2 to the junction of R_1 and R_2.

* At low frequencies, X_{C1} & X_{C2} are much larger than R_1 & R_2 and they have no effect on the ckt. So, the o/p voltage is equal to the I/p giving a voltage gain of 1 $\left(\because A_V = \frac{V_o}{V_i}\right)$.

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* At high frequencies, the effect of C_1 & R_2 causes the o/p to fall off at a rate of 20 dB per decade as the frequency increases.

* The R_2 & C_1 introduces a phase lag.

The C_2 combined with R_1 & R_2 introduces a phase lead.

The result of these phase difference is that the feedback via C_2 produces a further fall off of 20dB per decade.

Thus second order low pass filter produces a fall-off rate of 40dB per decade.

Design steps :-

1) $R_1 + R_2 = \dfrac{0.1\, V_{BE}}{I_{B(max)}}$

2) $R_1 = R_2$

3) $X_{C_1} = \sqrt{2}\, R_2$ at f_c

$$\frac{1}{2\pi f_c C_1} = \sqrt{2}\, R_2.$$

$$\boxed{C_1 = \frac{1}{2\pi f_c \sqrt{2} R_2}}$$

4) $R_3 = R_1 + R_2$

5) $C_2 = 2C_1$

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Second order low pass active filter :-

FORMULAE

1) $R_1 + R_2 = \dfrac{0.1\,V_{BE}}{I_{B(max)}}$ usually $R_1 = R_2$.

2) $X_{C1} = \sqrt{2}\,R_2$ at f_c

$$\frac{1}{2\pi f_c C_1} = \sqrt{2}\,R_2$$

$$C_1 = \frac{1}{2\pi f_c \sqrt{2} R_2}$$

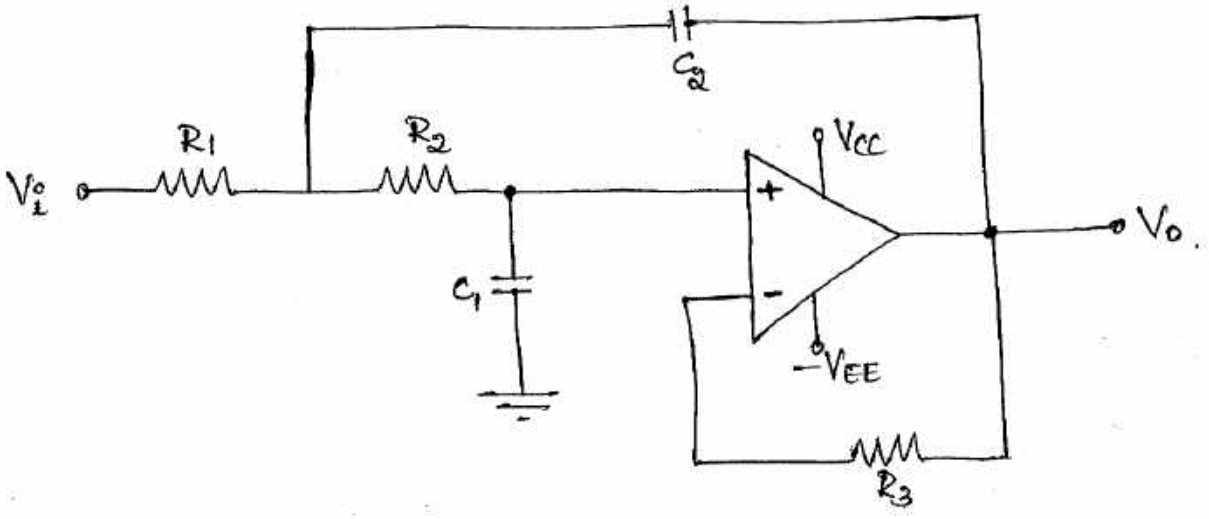
3) $R_3 = R_1 + R_2$

4) $C_2 = 2C_1$

NOTE :- The resistance R_1 satisfies the equation.

$$R_1 = \sqrt{2}\,X_{C2}$$

$$R_1 = \frac{\sqrt{2}}{2\pi f_c C_2}$$



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PROBLEMS :

1) Design a second order loco pass filter circuit to have a cut-off frequency of 1 KHz.

Given : $f_c = 1KHz$, assuming $V_{BE} = 0.7V$

Sol : for 741 op-amp : $I_{B(max)} = 500nA$.

* $R_1 + R_2 = \frac{0.1\ V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7V}{500nA}$

$R_1 + R_2 = 140K\Omega$, $R_1 = R_2 = \frac{140K\Omega}{2}$.

If $R_1 = R_2 = 70K\Omega$, choose std value $\boxed{R_1 = R_2 = 68K\Omega}$

* $R_3 = R_1 + R_2 = 68K\Omega + 68K\Omega$

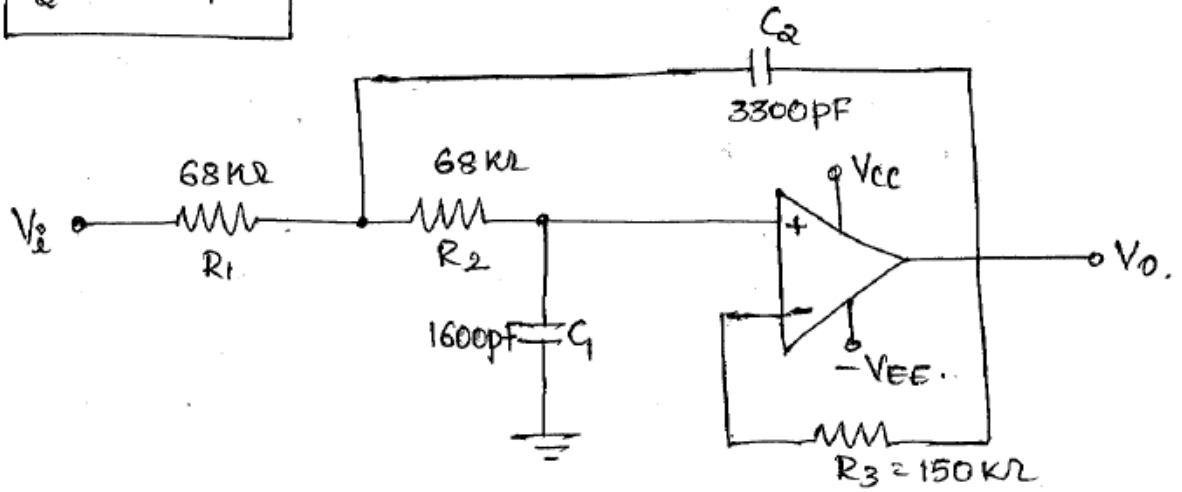
$R_3 = 136K\Omega$, choose $\boxed{R_3 = 150K\Omega}$

* $C_1 = \frac{1}{2\pi f_c \sqrt{2} R_2} = \frac{1}{2\pi \times 1KHz \times \sqrt{2} \times 68K\Omega} = 1655pF.$

choose, $\boxed{C_1 = 1600pF}$

* $C_2 = 2C_1 = 2 \times 1600pF = 3200pF$

use $\boxed{C_2 = 3300pF}$



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2) Design a second order low pass Active filter having a cut-off frequency of 2.5 KHz. Use 709 op-amp.

Given :- $f_c = 2.5\,KHz$

For op-amp 709 : $I_{B(max)} = 200\,nA$

Sol :-

* $R_1 + R_2 = \dfrac{0.1\,V_{BE}}{I_{B(max)}} = \dfrac{0.1\,V \times 0.7\,V}{200\,nA} = 350\,K\Omega$

$R_1 = R_2 = \dfrac{350\,K\Omega}{2} = 175\,K\Omega$

choose std value of $\boxed{R_1 = R_2 = 180\,K\Omega}$

* $R_3 = R_1 + R_2 = 180\,K\Omega + 180\,K\Omega = 360\,K\Omega$

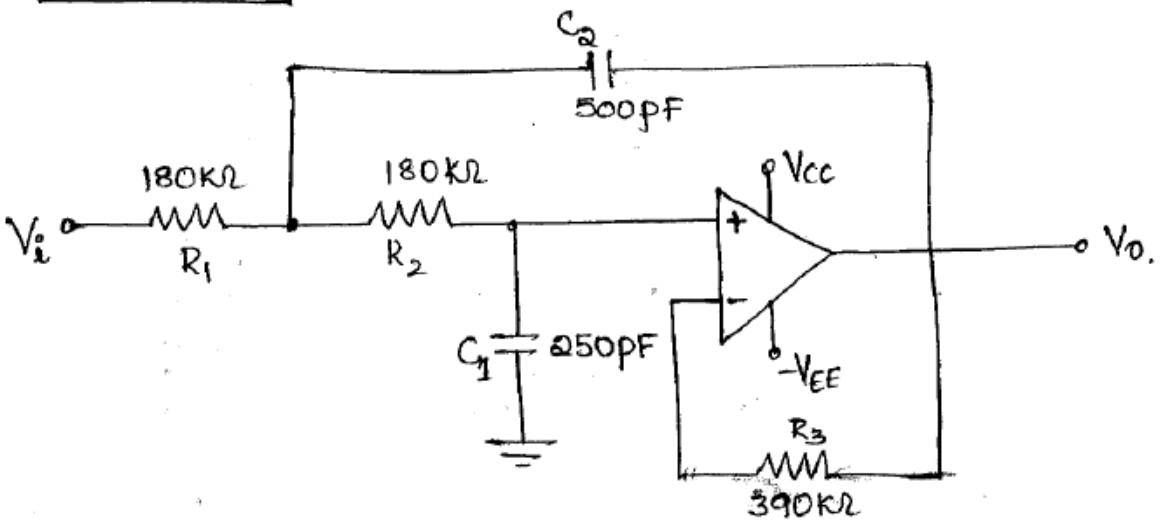
choose std value of $\boxed{R_3 = 390\,K\Omega}$

* $C_1 = \dfrac{1}{2\pi f_c \sqrt{2} R_2} = \dfrac{1}{2\pi \times 2.5\,KHz \times \sqrt{2} \times 180\,K\Omega}$

$\boxed{C_1 = 250\,pF}$

* $C_2 = 2C_1 = 2 \times 250\,pF$

$\boxed{C_2 = 500\,pF}$



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3) Using a 741 op-amp, design a second order low pass filter to have a cut-off frequency of 5 KHz.

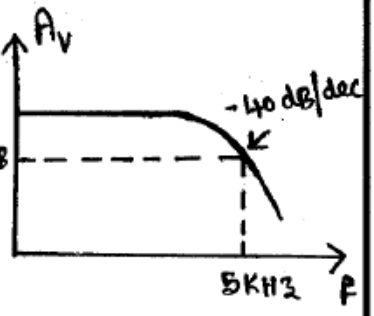
Jan-09, 6M (EE)

Dec-10, 8M

Given: $f_c = 5\,KHz$

Sol: For 741 op-amp: $I_{B(max)} = 500nA$

Assume $V_{BE} = 0.7\,V$.



* $R_1 + R_2 = \frac{0.1\,V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7V}{500nA} = 140\,K\Omega$

$R_1 = R_2 = \frac{140K\Omega}{2} = 70\,K\Omega$

Use std value $\boxed{R_1 = R_2 = 68\,K\Omega}$ ← (2m)

* $R_3 = R_1 + R_2 = 68\,K\Omega + 68\,K\Omega = 136\,K\Omega$

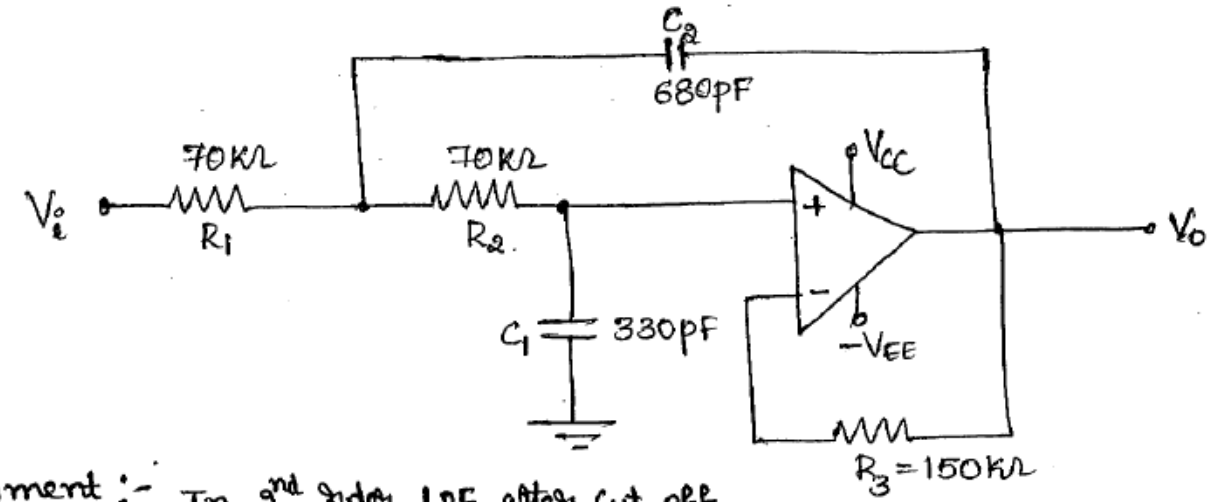
Use std value $\boxed{R_3 = 150\,K\Omega}$ ← (1m)

* $C_1 = \frac{1}{2\pi f_c \sqrt{2} R_2} = \frac{1}{2\pi \times 5KHz \times \sqrt{2} \times 68K\Omega} = 330.9\,pF$

Use std value, $\boxed{C_1 = 330\,pF}$ ← (1½ m)

* $C_2 = 2C_1 = 2 \times 330\,pF = 660pF$

Use std value $\boxed{C_2 = 680\,pF}$ ← (1½ m)



Comment:- In 2nd order LPF after cut-off frequency, the voltage gain decreases at the rate of 40 dB/decade.

* At cut-off freq, vtg gain drops by 3 dB from its maximum gain.

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4) Design a second order low pass filter ckt to have a cutoff frequency of 2KHz. Draw the ckt & indicate the frequency response of the filter.

Jan-10, 10M

Given: $f_c = 2KHz$

Sol: For 741 op-amp: $I_{B(max)} = 500nA$

Assume $V_{BE} = 0.7V$.

* $R_1 + R_2 = \frac{0.1 V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7V}{500nA} = 140K\Omega$

$R_1 = R_2 = \frac{140K\Omega}{2} = 70K\Omega$

Use std value $R_1 = R_2 = 68K\Omega$ ← (2M)

* $R_3 = R_1 + R_2 = 68K\Omega + 68K\Omega = 136K\Omega$

Use std value $R_3 = 150K\Omega$ ← (1M)

* $C_1 = \frac{1}{2\pi f_c \sqrt{2} R_2} = \frac{1}{2\pi \times 2KHz \times 68K\Omega \times \sqrt{2}} = 827.4pF$

Use std value $C_1 = 820pF$ ← (1½ M)

* $C_2 = 2C_1 = 2 \times 820pF = 1640pF$

Use std value $C_2 = 1600pF$ ← (1½ M)

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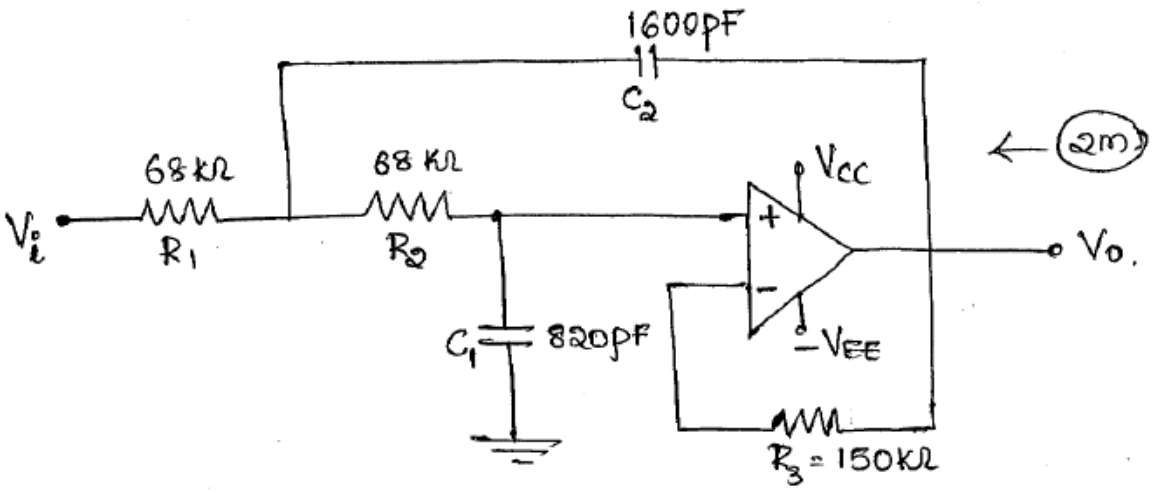

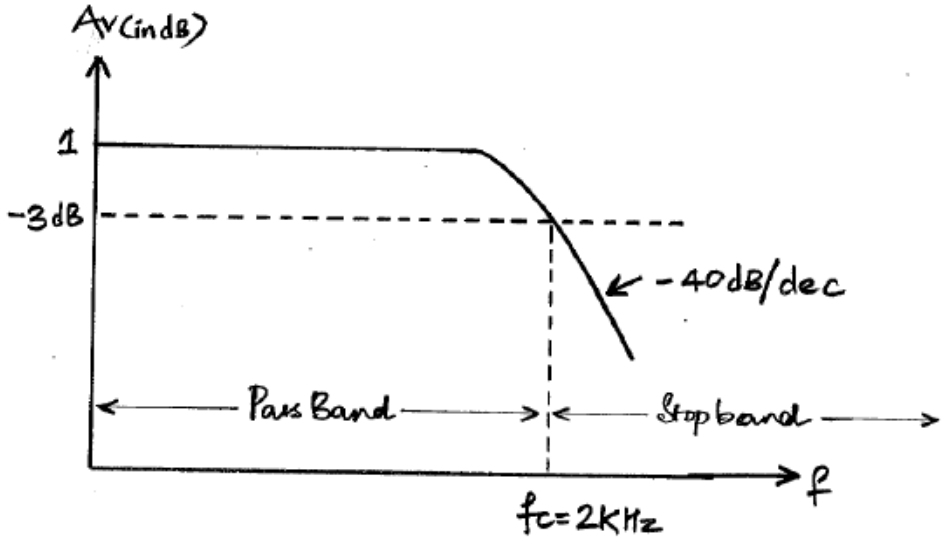

3) Design a 2nd order LPF using 741 for a cut-off frequency of 5KHz. Draw its frequency response & Comment on the same.

Dec-10, 8M

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First order High pass Active filter :-

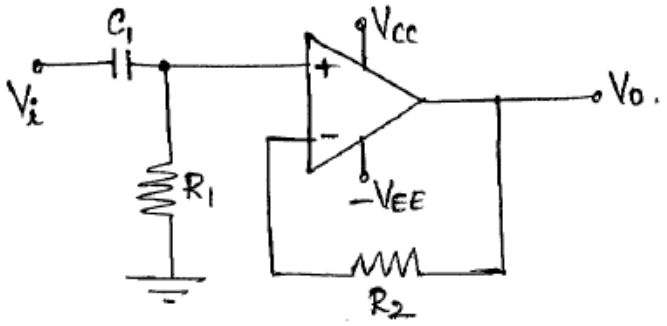
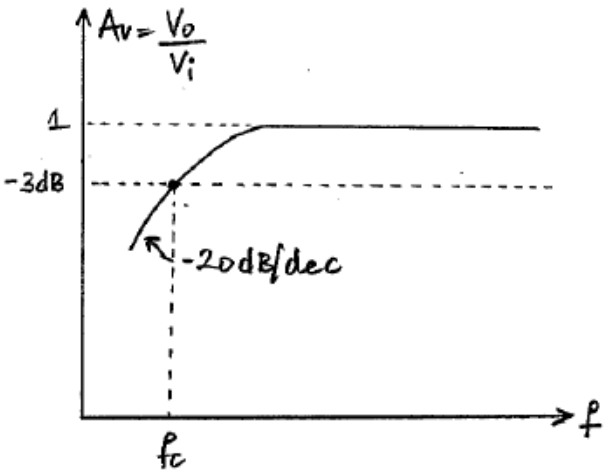


fig @ Active high pass filter.



* The first order high pass filter can be obtained by interchanging the elements R_1 & C_1 in a first order low pass filter circuit.

In fig @, the voltage follower isolates the load from R_1 & C_1.

* At high frequencies, X_{C1} is very much smaller than R_1 & voltage gain V_o/V_i is almost equal to 1 or 0 dB.

* When the frequency decreases to a value such that $X_{C1} = R_1$, the voltage gain drops by 3dB. As the frequency decreases further, the voltage gain rolls off at 20 dB per decade.

Design steps :

1) $R_1 = \dfrac{0.1\, V_{BE}}{I_{B(max)}}$ 2) $R_2 = R_1$.

3) $X_{C1} = R_1$ at f_c.

$\dfrac{1}{2\pi f_c C_1} = R_1$

$$C_1 = \frac{1}{2\pi f_c R_1}$$

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FORMULAE : 1st order HPF.

1) $R_1 = \dfrac{0.1\,V_{BE}}{I_{B(max)}}$

2) $R_2 = R_1$

3) $C_1 = \dfrac{1}{2\pi f_c R_1}$.

FOR BIFET op-amp.

FORMULAE :-

NOTE :- LM 108 has very low input bias current, it should be treated as BIFET op-amp.

1) Select C_1, very much larger than stray capacitance.

i.e. $\boxed{C_1 = 1000pF}$

2) $R_1 = \dfrac{1}{2\pi f_c C_1}$

3) $R_2 = R_1$

4) For LM 108 op-amp, the unity gain frequency

$\boxed{f_u = 1MHz}$ i.e. $f_2 = \dfrac{f_u}{A_V} = 1MHz$

ARUNKUMAR G M.Tech, Lecturer in E&CE Dept. S.T.J.I.T., Ranebennur.

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1) Design a first order active high-pass filter for a cut-off frequencies of 4.5 KHz. Use 741 op-amp.

Given :- $f_c = 4.5$ KHz

for 741 op-amp : $I_{B(max)} = 500nA$

Assume : $V_{BE} = 0.7V$

Sol :-

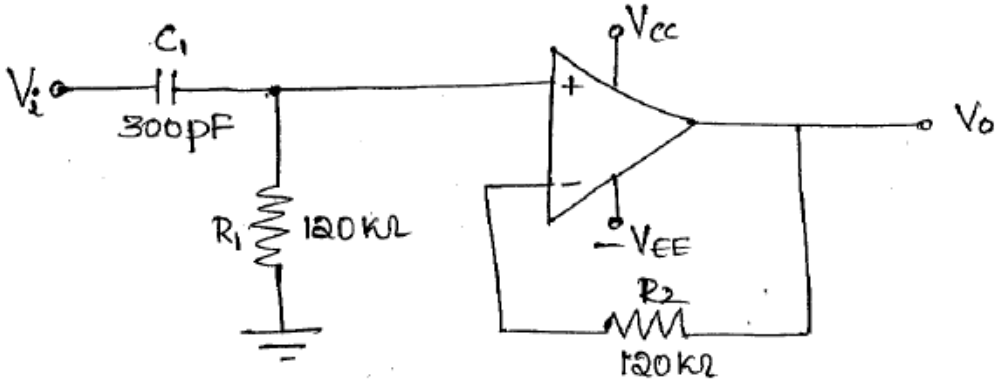
* $R_1 = \frac{0.1 V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7V}{500nA} = \underline{140K\Omega}$

Use std value $\boxed{R_1 = 120K\Omega}$

* $\boxed{R_2 = R_1 = 120K\Omega}$

* $C_1 = \frac{1}{2\pi f_c R_1} = \frac{1}{2\pi \times 4.5KHz \times 120K\Omega} = \underline{295pF}$

Use std value : $\boxed{C_1 = 300pF}$



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2) Design a first order high pass active filter ckt to have a cut-off frequency of 5 KHz. Use an LM 108 op-amp & estimate the highest frequency that can be passed.

Given: $f_c = 5KHz$.

Sol:

The LM 108 op-amp has very low input bias current, it should be treated as BIFET op-amp.

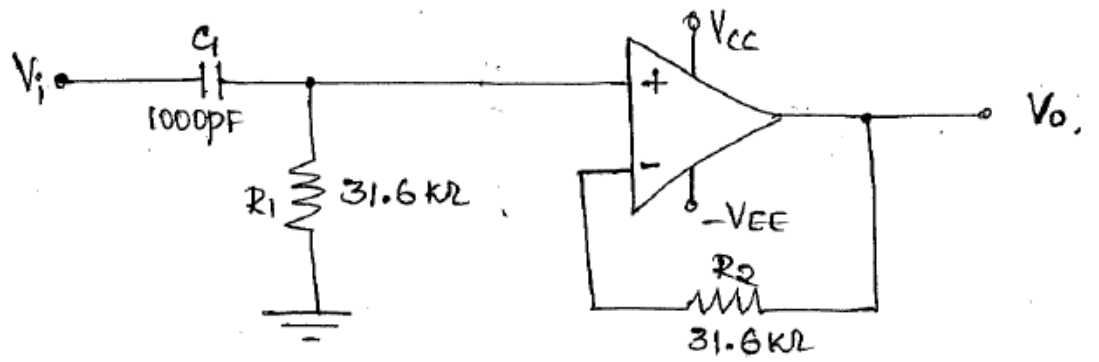
* Select C_1 very much larger than stray capacitance.

∴ $\boxed{C_1 = 1000pf}$

* $R_1 = \frac{1}{2\pi f_c C_1} = \frac{1}{2\pi \times 5KHz \times 1000pf} = \underline{31.8\,K\Omega}$

* Use std value $\boxed{R_1 = 31.6\,K\Omega}$ ±1%.

* $\boxed{R_2 = R_1 = 31.6\,K\Omega}$



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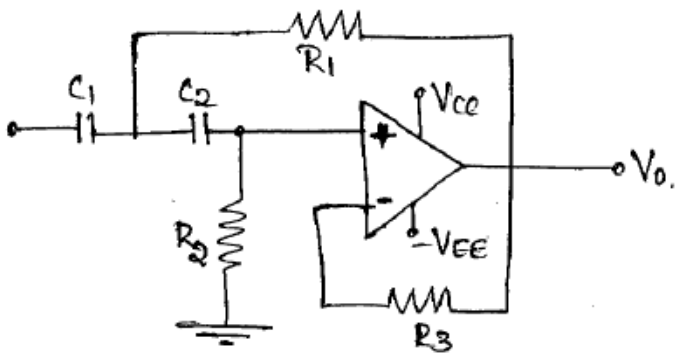
Second order high pass active filter :-

* Sketch the ckt of a second order active high pass filter, explain its working.

June - 10, 8M



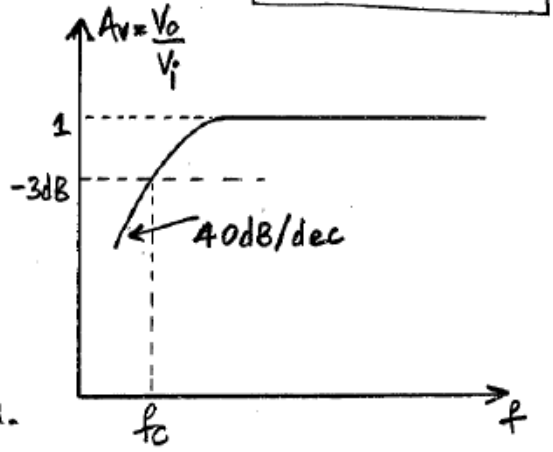


fig @ : Second order high pass filter.

* The second order high pass filter ckt is similar to the second order low-pass filter ckt, except that the resistor and capacitor positions are interchanged.

* At higher frequencies, X_{C1} & X_{C2} are much smaller than R_1 & R_2, consequently, C_1, C_2, R_1 & R_2 have no significant effect on the ckt.

The o/p voltage is then equal to the I/p, giving a voltage gain of 1.

* At low frequencies, the effect of C_2 & R_2 causes the o/p to fall off at a rate of 20dB per decade. A phase lead is produced by C_2 & R_2 & a phase lag is generated by R_1 combined with C_1 & C_2. So, feedback via R_1 produces a further roll-off of 20 dB per decade.

Thus the total roll-off rate is 40dB per decade.

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Design steps :-

1) $R_2 = \dfrac{0.1\, V_{BE}}{I_{B(max)}}$

2) $R_2 = \sqrt{2}\, X_{C_2}$ at f_c

$$R_2 = \sqrt{2} \cdot \frac{1}{2\pi f_c C_2}$$

$$C_2 = \frac{\sqrt{2}}{2\pi f_c R_2} = \frac{1}{2\pi f_c \left(\frac{R_2}{\sqrt{2}}\right)}$$

3) $C_1 = C_2$

4) $R_1 = \dfrac{R_2}{2}$

5) $R_3 = R_2$

6) The impedance X_{C_1} satisfies the equation.

$$X_{C_1} = \sqrt{2}\, R_1 \text{ at } f_c$$

i.e. $$C_1 = \frac{1}{2\pi f_c \left(\frac{R_1}{\sqrt{2}}\right)}$$

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2nd order HPF :-

FORMULAE :

1) $R_2 = \dfrac{0.1\,V_{BE}}{I_{B(max)}}$

2) $C_2 = \dfrac{\sqrt{2}}{2\pi f_c R_2} = \dfrac{1}{2\pi f_c \left(\dfrac{R_2}{\sqrt{2}}\right)}$

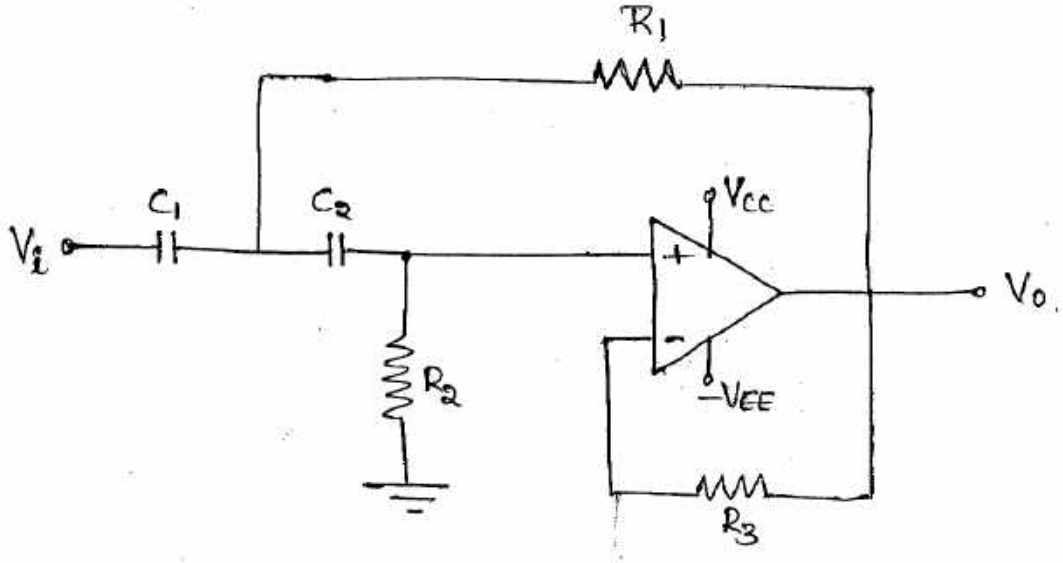
3) $C_1 = C_2$

4) $R_1 = \dfrac{R_2}{2}$

5) $R_3 = R_2$.

NOTE :- The impedance X_{C1} satisfies the equation.

$$\boxed{X_{C1} = \sqrt{2}\,R_1}$$



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1) Design a second order high pass active filter to have a cutoff frequency of 12 KHz. Use a 715 op-amp and estimate the highest signal frequency that will be passed.

Given:- $f_c = 12\ KHz$

Sol: for 715 op-amp : $I_{B(max)} = 1.5\ \mu A$

* $R_2 = \frac{0.1\ V_{EE}}{I_{B(max)}} = \frac{0.1\ V \times 0.7\ V}{1.5\ \mu A} = 46.66\ K\Omega$

Use std value $\boxed{R_2 = 47\ K\Omega}$

* $R_1 = \frac{R_2}{2} = \frac{47\ K\Omega}{2} = 23.5\ K\Omega$

Use std value $\boxed{R_1 = 22\ K\Omega}$

* $\boxed{R_3 = R_2 = 47\ K\Omega}$

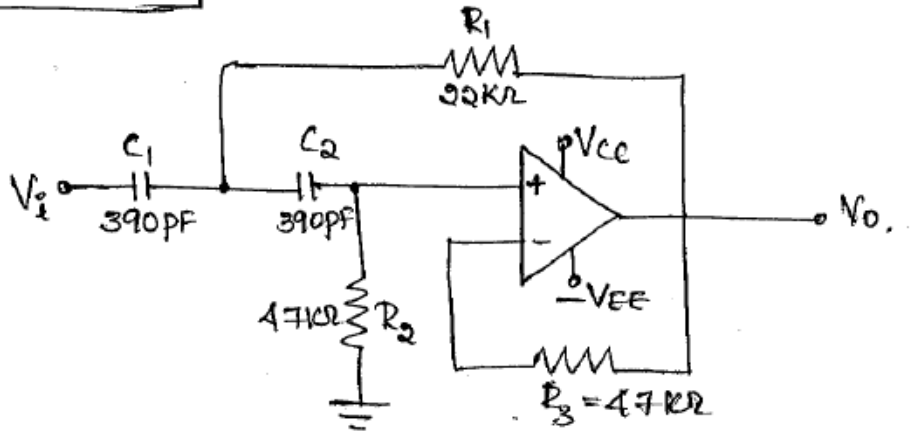
* $C_2 = \frac{1}{2\pi f_c \left(\frac{R_2}{\sqrt{2}}\right)} = \frac{1}{2\pi \times 12\ KHz \times \left(\frac{47\ K\Omega}{\sqrt{2}}\right)} = 398\ pF$

Use std value $\boxed{C_2 = 390\ pF}$

* $\boxed{C_1 = C_2 = 390\ pF}$

* From 715 data sheet, the op-amp unity gain cut-off frequency is $\boxed{f_u = 11\ MHz}$

$\boxed{f_2 = \frac{f_u}{A_V} = 11\ MHz}$



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2) Using op-amp, design a second order high pass filter to have a cut off frequency of 7KHz. June-08, 6M

Given :- $f_c = 7KHz$

Sol :- for 741 op-amp : $I_{B(max)} = 500nA$

Assume : $V_{BE} = 0.7V$

* $R_2 = \frac{0.1\,V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7V}{500\,nA} = 140K\Omega$

Use std value, $\boxed{R_2 = 120K\Omega}$

* $R_1 = \frac{R_2}{2} = \frac{120K\Omega}{2} = 60K\Omega$

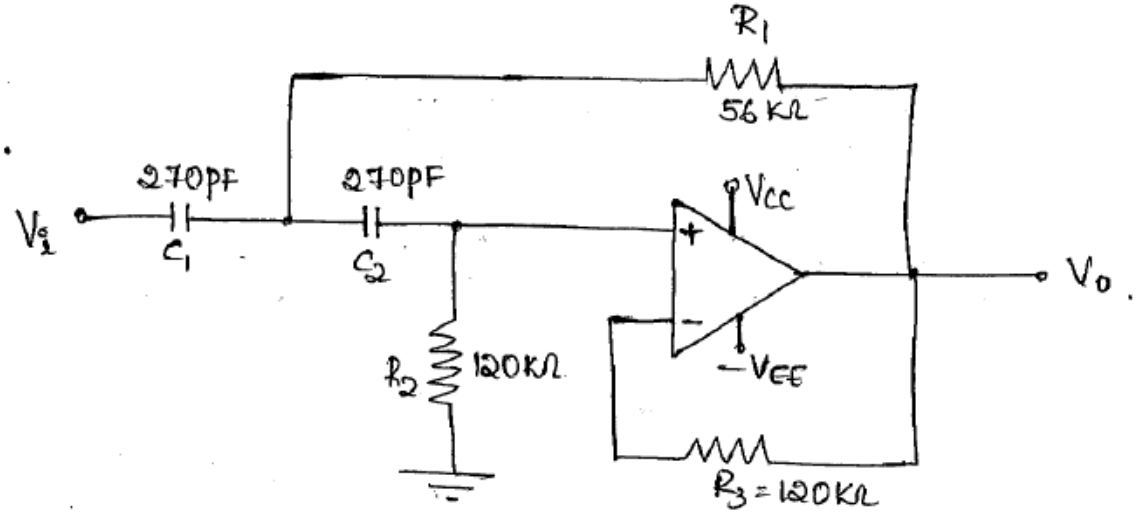
Use std value $\boxed{R_1 = 56K\Omega}$

* $\boxed{R_3 = R_2 = 120K\Omega}$

* $C_2 = \frac{1}{2\pi f_C \left(\frac{R_2}{\sqrt{2}}\right)} = \frac{1}{2\pi \times 7KHz \times \left(\frac{120K\Omega}{\sqrt{2}}\right)}$

* $\boxed{C_2 = 267.9pF}$ Use std value $\boxed{C_2 = 270pF}$

* $\boxed{C_1 = C_2 = 270pF}$



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3) Using a 741 op-amp, design a second order high-pass filter to have a cut off frequency of 15 KHz.

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Given :- $f_c = 15\ KHz$

Sol :- For 741 op-amp : $I_{B(max)} = 500nA$

Assume : $V_{BE} = 0.7V$

* $R_2 = \frac{0.1\ V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7V}{500\ mA} = 140\ K\Omega$

Use std value $\boxed{R_2 = 120K\Omega}$ ← (1M)

* $R_1 = \frac{R_2}{2} = \frac{120K\Omega}{2} = 60\ K\Omega$.

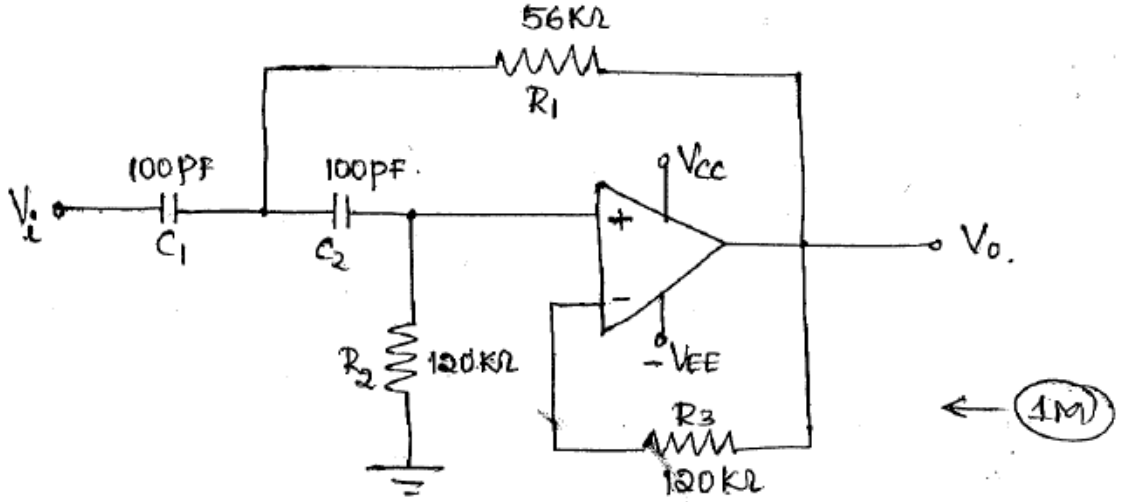
Use std value $\boxed{R_1 = 56\ K\Omega}$

* $\boxed{R_3 = R_2 = 120K\Omega}$ ← (1m)

* $C_2 = \frac{1}{2\pi f_c \frac{R_2}{\sqrt{2}}} = \frac{1}{2\pi \times 15\ KHz \times \left(\frac{120K\Omega}{\sqrt{2}}\right)}$

$\boxed{C_2 = 125\ pF}$ ← (1M) choose $\boxed{C_2 = 100\ pf}$

* $\boxed{C_1 = C_2 = 100pF}$ ← (1M)



← (1M)

ARUNKUMAR G M.Tech, Lecturer in E&CE Dept. S.T.J.I.T., Ranebennur.

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Voltage Regulators

A voltage regulator is an electronic CKT that provides a constant dc o/p voltage independent of the [change in] the load current, temperature and ac line voltage variations.

Voltage regulators are classified as

1) Series regulator
2) Switching regulator

Series op-amp regulator :-

Show how op-amp can be used as series regulator

Model paper 1 - 6M

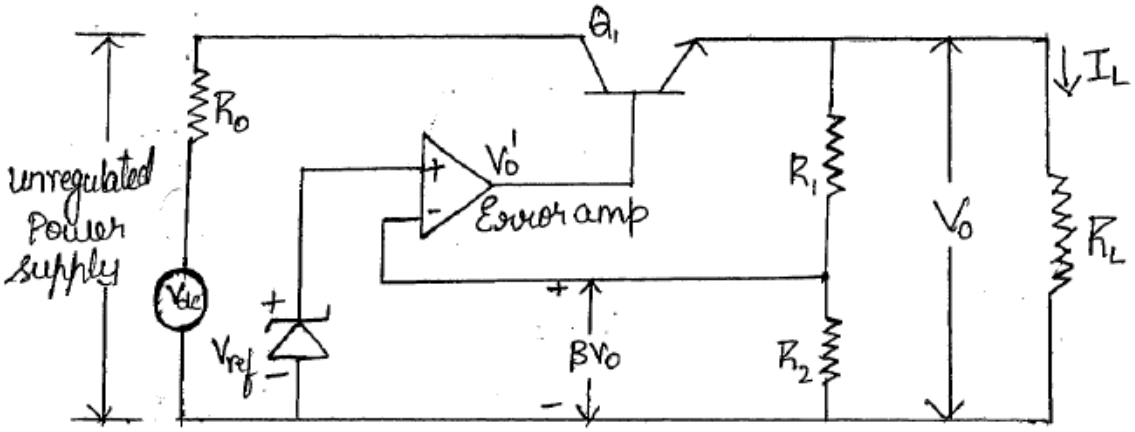

fig (1) A regulated power supply

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* A voltage regulator is an electronic ckt that provides a constant dc o/p voltage independent of the [change in] the load current, temperature & ac line voltage variations

fig (1) shows a regulated power supply. The ckt consists of four major components.

1) Reference voltage 'V_{ref}' [Zener diode]

2) Error amplifier [Difference amplifier]

3) Series pass transistor [Q_1]

4) Feedback network [R_1 & R_2]

* The power transistor Q_1 is in series with the unregulated dc voltage 'V_{in}' and the regulated o/p voltage 'V_o'. Any variation in o/p voltage is absorbed by this transistor

* The transistor Q_1 connected as an emitter follower and therefore provide sufficient current gain to drive the load.

The o/p voltage is sampled by potential divider R_1 and R_2 [feedback N/w] and fed back to the INV input terminal of the op-amp error amplifier

* The sampled voltage is compared with the reference voltage V_{ref}. The o/p 'V_o' of the error amplifier drives the series transistor Q_1.

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When the o/p voltage tends to increase, then the feedback voltage βV_o also increases.

where $\beta = \frac{R_2}{R_1 + R_2}$

* The voltage at INV input terminal of op-amp increases and as a result the o/p voltage V_o' of the op-amp decreases. Since Q acts as emitter follower, the o/p voltage V_o which follows V_o', thus the V_o also reduces.

Thus o/p voltage V_o remains constant.

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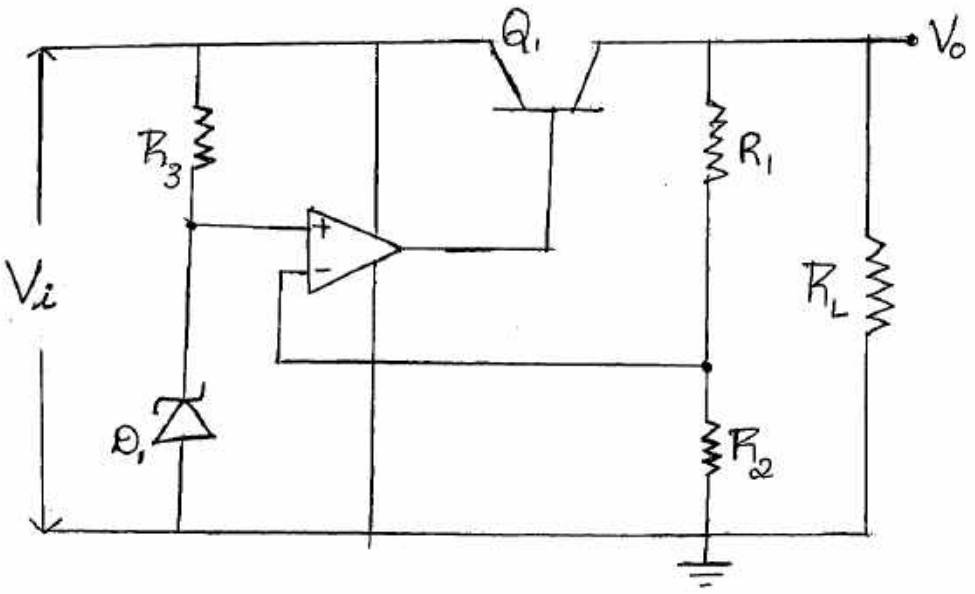
Problem :

Series Pass regulator :-



Formulae :

$I_2 = 50\,\mu A$

1) $V_{S(min)} = V_o + 3V$

2) $R_3 = \dfrac{V_o - V_z}{I_{z(max)}}$

3) $R_1 = \dfrac{V_o - V_z}{I_2}$

4) $R_2 = \dfrac{V_z}{I_2}$

$V_{CE} = 0.7V$

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Design a series pass regulator to given an o/p of 9 volts to a minimum and load resistance of 36Ω for a two-in-one radio. The input dc coming from a rectifier filter varies between 9 volts to 15 volts. The op-amp available has a bias current of 12 mA and requires $V_{S\,min} = \pm 7V$ & $V_{Smax} = \pm 18V$. The available zener diode is of 4.7V with $I_{Zmax} = 20mA$. Specify the ratings required of series pass element and constant current short ckt protection transistor.

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Given:- $V_o = 9V$, $V_Z = 4.7V$, $I_B = 12mA$,

$I_{Z(max)} = 20mA$, $V_{S(min)} = \pm 7V$, $V_{S(max)} = \pm 18V$

Sol:

Choosing $\boxed{I_2 = 50\mu A}$

* $R_3 = \dfrac{V_o - V_Z}{I_{Z(max)}} = \dfrac{9V - 4.7V}{20\,mA} = 430\Omega$ [215Ω] rit ans

* Choose $\boxed{R_3 = 440\Omega}$

$R_1 = \dfrac{V_o - V_Z}{I_2} = \dfrac{9 - 4.7V}{50\mu A} = 86K\Omega$

choose $\boxed{R_1 = 82K\Omega}$

* $R_2 = \dfrac{V_Z}{I_2} = \dfrac{4.7}{50\mu A} = 94K\Omega$

Choose $\boxed{R_2 = 91K\Omega}$

* $V_{CE} = 0.7V$

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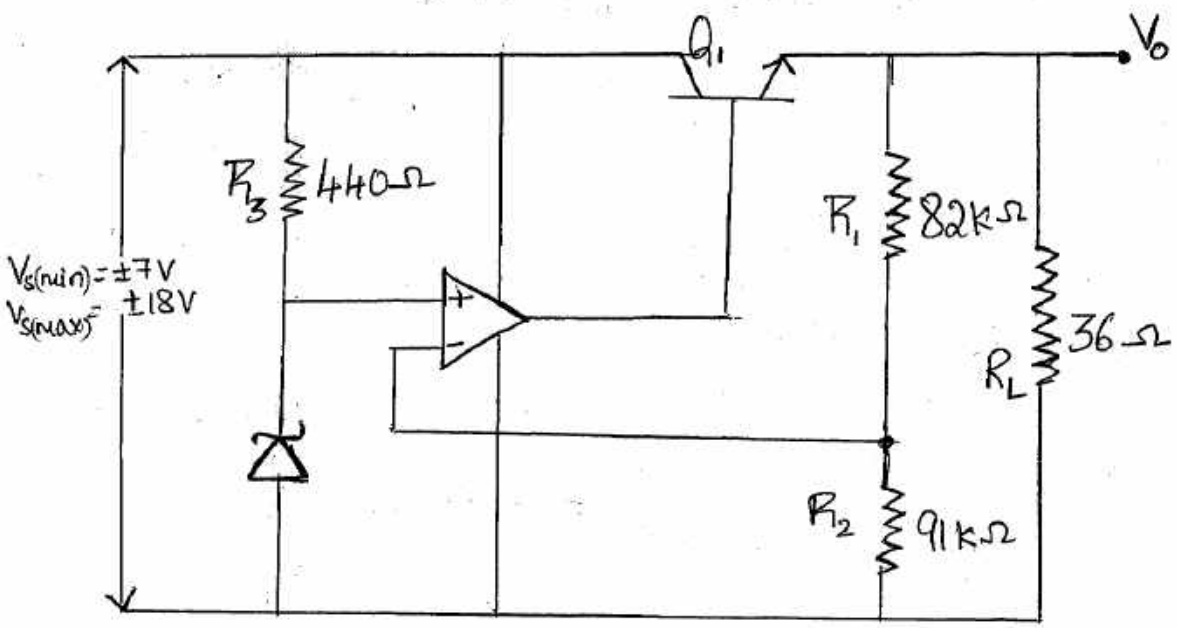

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IC Voltage Regulators :-

* IC voltage regulator replaces discrete component ckts op-amp regulator with IC, which gives low cost, high reliability, reduction in size & excellent performance.

Eg: i) 78xx | 79xx Fixed voltage series regulators

ii) 723 general purpose regulators.

Fixed Voltage Series Regulator:

Briefly explain the standard representation / configuration of 78XX regulators.

Jan-2011, 6M

* 78XX series are three terminals positive fixed voltage regulators. In 78xx, the last two numbers 'xx' indicate the o/p voltage.

7805 → +5V
7806 → +6V
7808 → +8V
7812 → +12V
7815 → +15V
7818 → +18V
7824 → +24V

← (2M)

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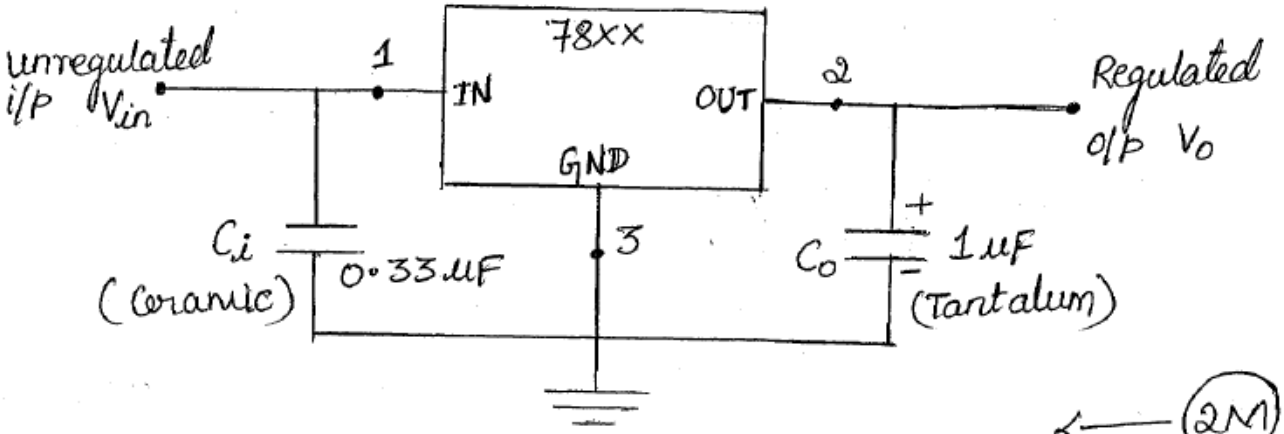
* 79xx series are three terminals negative fixed voltage regulators. In 78xx, the last two numbers 'xx' indicate the o/p voltage.

In 79xx series two extra voltage options of −2V and −5.2V available.

These regulators are available in two types of package:

1) Metal package
2) Plastic package



← (2M)

fig shows the standard representation of IC voltage regulator.

* A capacitor Ci is usually connected between input and ground terminal to cancel the inductive effective due to long leads.
* The o/p capacitor Co improves the transient response.

↑ 2M

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Characteristics of IC regulators:

* List and briefly explain the characteristics of three terminal IC regulators. what are the limitations of these regulators ?

June-08, 7M

There are four characteristics of three terminal IC regulators:

1) V_o : [Regulated o/p voltage]

The regulated o/p voltage is fixed at a value as specified by the manufacturer.
There are various models available with different o/p voltages.

Eg: 78XX series has o/p voltage at 5, 6, 8, 12, 15, 18V etc

2) $|V_{in}| \geq |V_o| + 2$ volts :

The unregulated input voltage must be atleast 2V more than the regulated o/p voltage.

for example, if $V_o = 5V$, then $V_{in} = 7V$

3) Maximum o/p current '$I_{o(max)}$' :

The load current may vary from '0' to rated maximum o/p current. The IC is usually provided with a heat sink, otherwise it may not provide the rated maximum o/p current.

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4) Thermal Shutdown:

The IC has a built-in temperature sensor which turn-off the IC when it becomes too hot. The O/p current will drop and remains there until the IC has cooled significantly.

(HM)

Limitations:

1) No short ckt protection
2) O/p voltage is fixed

(2M)

Advantages of IC voltage Regulators:

1) Easy to use
2) Simplifies power supply design
3) Low cost
4) Conveniently used for local regulations.
5) Over-current protection
6) Thermal overload protection.

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Important Perfomance Parameter:

* Explain the important parameters listed in the data sheet of 78XX.
* Define and explain the following terms, used in a voltage regulator.
  i) Line regulation ii) Load regulation

Jan-09, 4M

* Explain the terms line regulation, load regulation and ripple rejection for a dc voltage regulator

June-09, 6M

The important perfomance parameters of a 3-terminal IC regulators are:

1) Line / Input Regulation
2) Load regulation
3) Ripple Rejection

1) Line regulation:

It is defined as the percentage change in the o/p voltage for a change in the input voltage. It is usually expressed in millivolt or as a percentage of the o/p voltage.

Typical value of line regulation from the data sheet of 7805 is 3mV.

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2) Load Regulation:

It is defined as the change in output voltage for a change in load current and is also expressed in millivolts or as percentage of V_o.

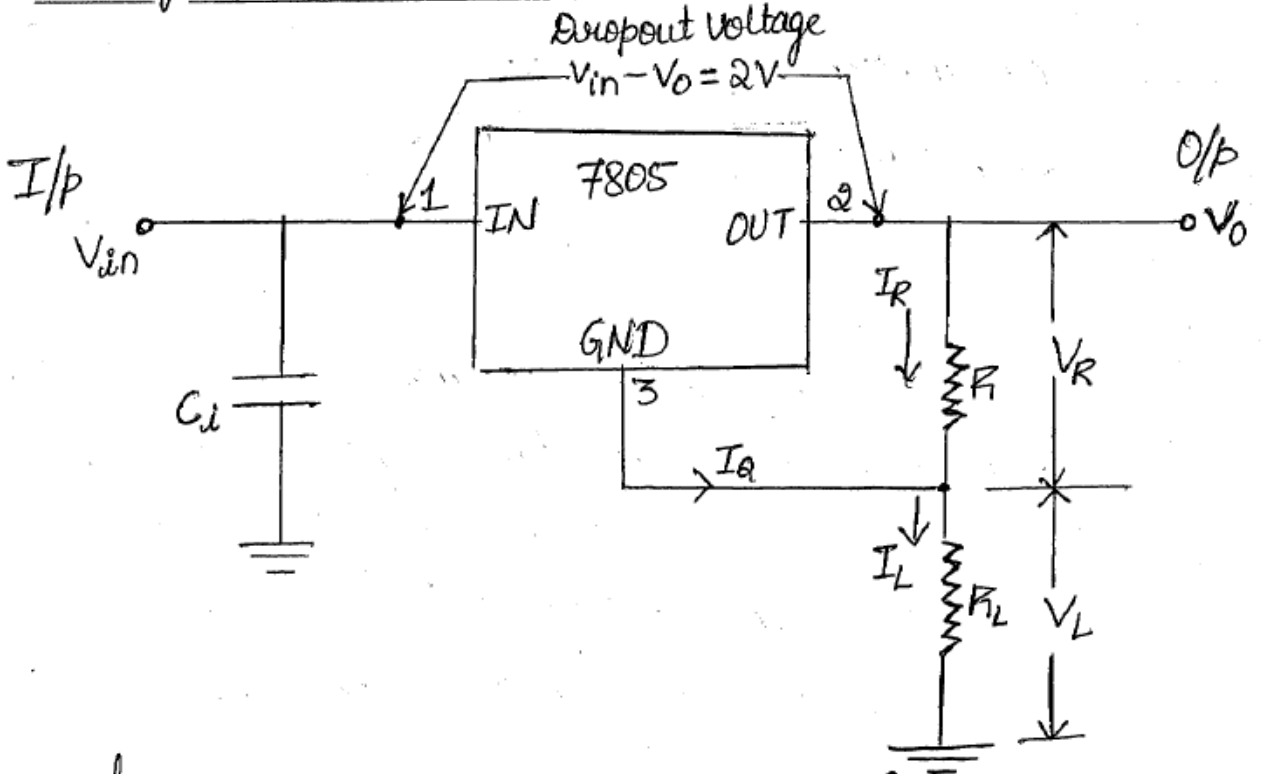
For 7805 regulator, the load regulation is 15mV for a load current variation for 5mA to 1.5 amps

3) Ripple rejection:

The IC regulator not only keeps the o/p voltage constant but also reduces the amount of ripple voltage [in o/p]. It is usually expressed in dB.

For 7805, it is 78dB.

IC Regulator used as a current source :-



fig(i): IC 7805 as a current source

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The three terminal fixed voltage regulator can be used as a current source as shown in fig ①. from the ckt it is clear that,

$$I_L = I_R + I_Q \longrightarrow ①$$

where I_Q is the quiescent current.

For 7805, $I_Q = 4.2\ mA$

* The I_R is given by

$$I_R = \frac{V_R}{R} \longrightarrow ②$$

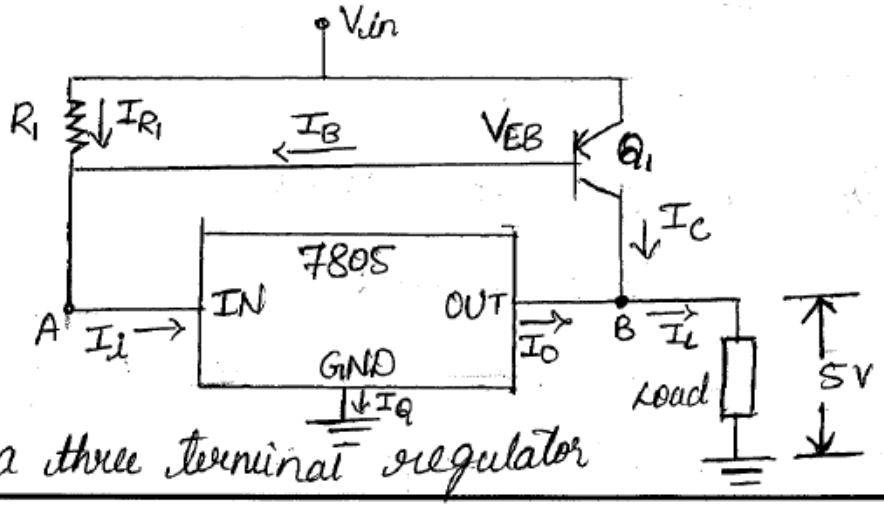
Sub eqn ② in eqn ①, we get

$$I_L = \frac{V_R}{R} + I_Q \longrightarrow ③$$

In eqn ③, V_R, I_Q are constant, R can be selected to provide a sufficient current.

Thus 78XX can be used as current source.

Boosting IC regulator o/p current:



fig②: Boosting a three terminal regulator

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It is possible to boost the o/p current of a three terminal regulator simply by connecting an external pass transistor in parallel with. The regulator as shown in fig ①.

Operation:

* For low load currents, the voltage drop across R_1 is insufficient [i.e; $V_{BE} < 0.7V$] to turn ON transistor Q_1 & the regulator itself is able to supply the load current.

* However when I_L increases, the voltage drop across R_1 increases. when this voltage drop [i.e $V_{BE} = 0.7V$] the transistor Q_1 turns ON & transistor Q_1 supplies the extra current needed to drive low resistance load.

* Applying KCL at node B, we get

$$I_C + I_O - I_L = 0$$

$$\boxed{I_L = I_O + I_C} \longrightarrow ①$$

(WKT $I_C = \beta I_B$)

* For regulator (for 7805)

$$\boxed{I_i = I_Q + I_O} \longrightarrow ②$$

Since I_Q is very small, we can neglect it

$$\therefore \boxed{I_i = I_O} \longrightarrow ③$$

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* Applying KCL at node A, we get

$$I_{R_1} + I_B - I_i = 0$$

$$\boxed{I_B = I_i - I_{R_1}} \rightarrow (4)$$

WKT $I_{R1} = \dfrac{V_{EB(ON)}}{R_1}$

Sub eqn (3) & I_{R_1} value in eqn (4), we get

$$I_B = I_0 - \frac{V_{EB(ON)}}{R_1}$$

WKT $\boxed{I_C = \beta I_B}$

Sub I_B value, we get

$$I_C = \beta \left[I_0 - \frac{V_{(ON)}}{R_1} \right]$$

$$\boxed{I_C = \beta I_0 - \beta \frac{V_{EB(ON)}}{R_1}} \rightarrow (5)$$

Sub eq (5) in eqn (1), we get

$$I_L = I_0 + \beta I_0 - \beta \frac{V_{EB(ON)}}{R_1}$$

$$\boxed{I_L = I_0 (1+\beta) - \beta \frac{V_{EB(ON)}}{R_1}}$$

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Boosting IC regulator o/p current problems:

FORMULAE:

i) When Q_1 is OFF [i.e; when $V_{BE} < 0.7V$]

1) $I_L = I_{R1}$

2) $I_L = \frac{V_0}{R_L}$

3) $V_{EB} = I_{R_1} \times R_1$

$$\boxed{V_{EB} = I_L \times R_1}$$

4) $I_0 = I_L = I_i$

ii) when Q_1 is ON [i.e; when $V_{EB} \geq 0.7V$]

1) $I_L = I_{R_1}$

2) $I_L = \frac{V_0}{R_L}$

3) $V_{BE} = I_L R_1$

4) $I_L = I_0(1+\beta) - \beta \frac{V_{EB(ON)}}{R_1}$

$$I_0(1+\beta) = I_L + \beta \frac{V_{EB(ON)}}{R_1}$$

$$\boxed{I_0 = \frac{I_L + \beta \frac{V_{EB(ON)}}{R_1}}{(1+\beta)}}$$

5) W.K.T. $I_L = I_0 + I_C$ $\boxed{I_C = I_L - I_0}$

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Design of current source:

FORMULAE:

1) V_R = voltage b/w pin 2 & 3

Eg: For 7805, $V_R = 5V$

For 7806, $V_R = 6V$

2) $I_L = \frac{V_R}{R} + I_Q$

$\frac{V_R}{R} = I_L - I_Q$

$\therefore \boxed{R = \frac{V_R}{I_L - I_Q}}$

NOTE: For 7805, $I_Q = 4.2\ mA$

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1) Using 7805, design a current source to deliver 0.2A current to a 22 Ω, 10W load. Take quiescent current as 4.2 mA.

June – 10, 6M

Given:- $I_L = 0.2\,A$, $R_L = 22\,\Omega$

For 7805 : $V_o = V_R = 5V$ &

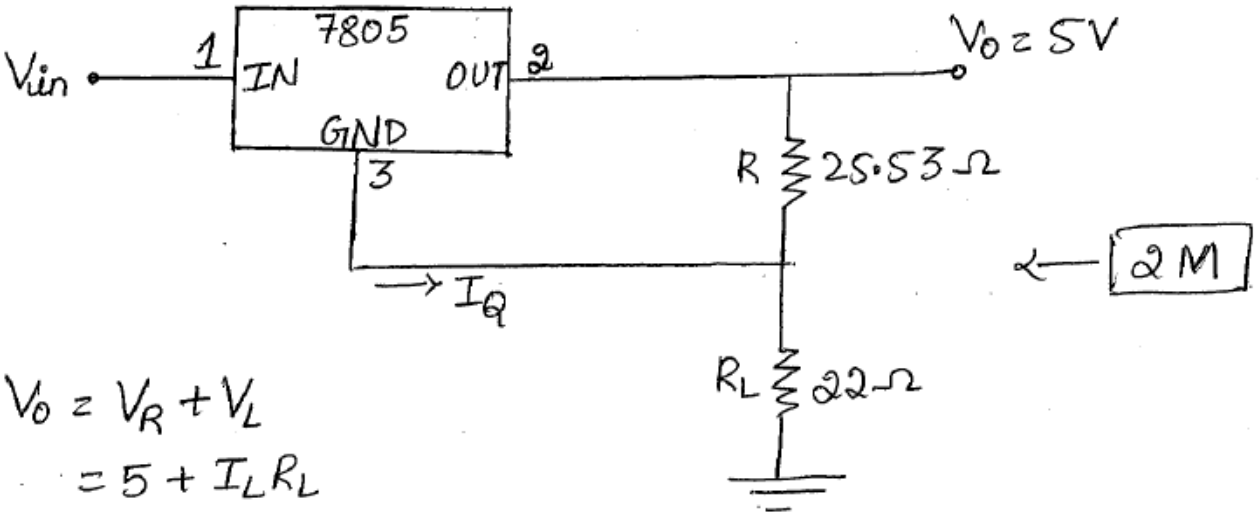
$I_Q = 4.2\,mA$

Sol:

$$I_L = \frac{V_R}{R} + I_Q$$

$$R = \frac{V_R}{I_L - I_Q} = \frac{5\,V}{0.2A - 4.2mA}$$

$R = 25.53\,\Omega$ ← (2M)



$V_o = V_R + V_L$

$= 5 + I_L R_L$

$= 5 + 0.2 \times 22\,\Omega$

$V_o = 9.4V$ ← 2M

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2. For the current booster circuit using 7805, Calculate the o/p current coming from 7805 & I_C coming from transistor Q_1 for loads 100Ω, 5Ω, 1Ω. Assume $V_{BE(ON)} = 1V$, $\beta = 15$, $R_1 = 7\Omega$

Given:- $V_{EB(ON)} = 1V$, $\beta = 15$, $R_1 = 7\Omega$

For 7805 : $V_o = 5V$

load : i) $R_L = 100\Omega$

ii) $R_L = 5\Omega$

iii) $R_L = 1\Omega$

Sol :-

i) $R_L = 100\Omega$

* $I_L = \frac{V_o}{R_L} = \frac{5V}{100\Omega}$

$$\boxed{I_L = 50mA}$$

$V_{EB} = I_L \times R_1 = 50mA \times 7\Omega$

$$\boxed{V_{EB} = 0.35V}$$

Since $V_{EB} < 0.7V$. Hence Q_1 is OFF

So $\boxed{I_o = I_L = I_i = 50mA}$

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ii) $R_L = 5\Omega$

* $I_L = \frac{V_o}{R_L} = \frac{5V}{5\Omega}$

$$\boxed{I_L = 1A}$$

* $V_{EB} = I_L R_1 = 1 \times 7\Omega$

$$\boxed{V_{EB} = 7V}$$

since $V_{EB} > 0.7V$

$\therefore$ $\boxed{Q_1 \text{ is ON}}$

Now

$$I_L = (1+\beta) I_o - \beta \frac{V_{EB(ON)}}{R_1}$$

$$I_o = \frac{I_L + \beta \frac{V_{EB(ON)}}{R_1}}{(1+\beta)} = \frac{1 + 15 \times \frac{1V}{7}}{1+15}$$

$$\boxed{I_o = 196mA}$$

* $I_C = I_L - I_o = 1A - 196mA$

$$\boxed{I_C = 804mA}$$

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iii) $R_L = 1\Omega$

* $I_L = \frac{V_o}{R_L} = \frac{5V}{1\Omega}$

$$\boxed{I_L = 5A}$$

* $V_{EB} = I_L R_1 = 5A \times 7\Omega$

$$\boxed{V_{EB} = 35V}$$

Since $V_{EB} > 0.7V$

$\therefore$ $\boxed{Q_1 \text{ is ON}}$

* $I_o = \frac{I_L + \beta \frac{V_{EB(ON)}}{R_1}}{1+\beta} = \frac{5A + 15 \times \frac{1V}{7V}}{(1+15)}$

$$\boxed{I_o = 446\,mA}$$

* $I_C = I_L - I_o = 5A - 446\,mA$

$$\boxed{I_C = 4.55A}$$

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Fixed Regulator used as adjustable Regulator:

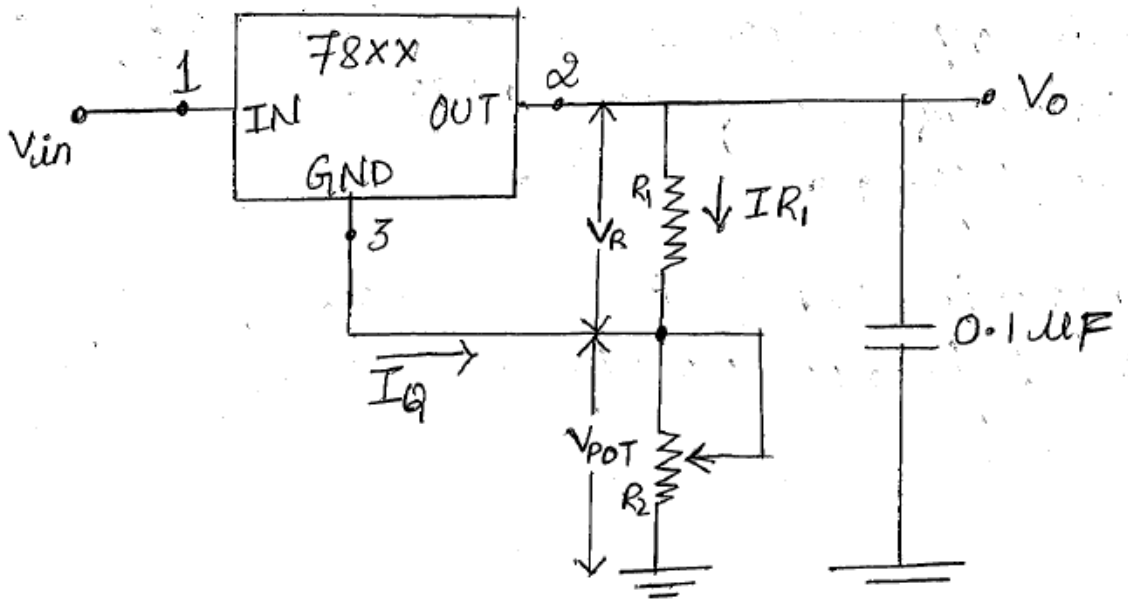


fig ①: Adjustable Regulator

* Fixed Regulator can be made use as a variable regulated voltage regulator. The CKT is shown in fig①

The o/p vltg of the CKT is

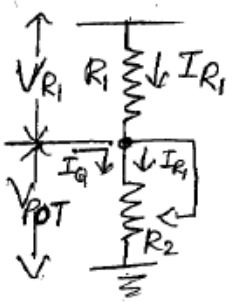
$$V_o = V_R + V_{POT}$$

$$V_o = V_R + (I_Q + I_{R_1}) R_2$$

$$V_o = V_R + I_Q R_2 + \underline{I_{R_1}} R_2$$

$$V_o = \underline{V_R} + I_Q R_2 + \frac{V_R}{R_1} R_2$$

$$\boxed{V_o = V_R\left(1 + \frac{R_2}{R_1}\right) + I_Q R_2} \rightarrow ①$$



$\therefore$ $V_{POT} = [I_Q + I_{R_1}] R_2$

&

$V_R = I_{R_1} \times R_1$

$$\boxed{I_{R_1} = \frac{V_R}{R_1}}$$

where V_R is the regulated voltage difference b/w the OUT and GND terminals.

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* The effect of I_Q is minimized by choosing R_2 as small as possible (i.e; neglecting $I_Q R_2$)

The minimum o/p voltage of the adjustable regulator is the value of the fixed voltage available from the regulator.

Hence neglecting $I_Q R_2$, it is possible to get an adjustable regulated voltage of any value.

NOTE:

* The LM117, 217, 317 '+'ve regulators and LM137, 237, 337 '−'ve regulators are used for obtaining adjustable o/p voltages.
* The o/p voltage can be adjusted from 1.2V to 40V & current upto 1.5A.

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FORMULAE:

1) $R_1 = \frac{V_R}{I_{R_1}}$

2) $R_2 = \frac{V_{POT}}{(I_Q + I_{R_1})}$

3) $V_o = V_R \left[1 + \frac{R_2}{R_1}\right]$

4) WKT in general $V_o = V_R + V_{POT}$

$$\boxed{V_{POT} = V_o - V_R}$$

NOTE :- For 7805, $I_Q = 4.2\ mA$

Assume: $I_{R_1} = 25mA$

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1) Specify suitable component values to get $V_o = 7.5V$ using a 7805 regulator.

Given: $V_o = 7.5V$

For 7805, o/p Vtg is 5V i.e; $\boxed{V_R = 5V}$ &

$\boxed{I_Q = 4.2mA}$

Assume: $I_{R_1} = 25mA$

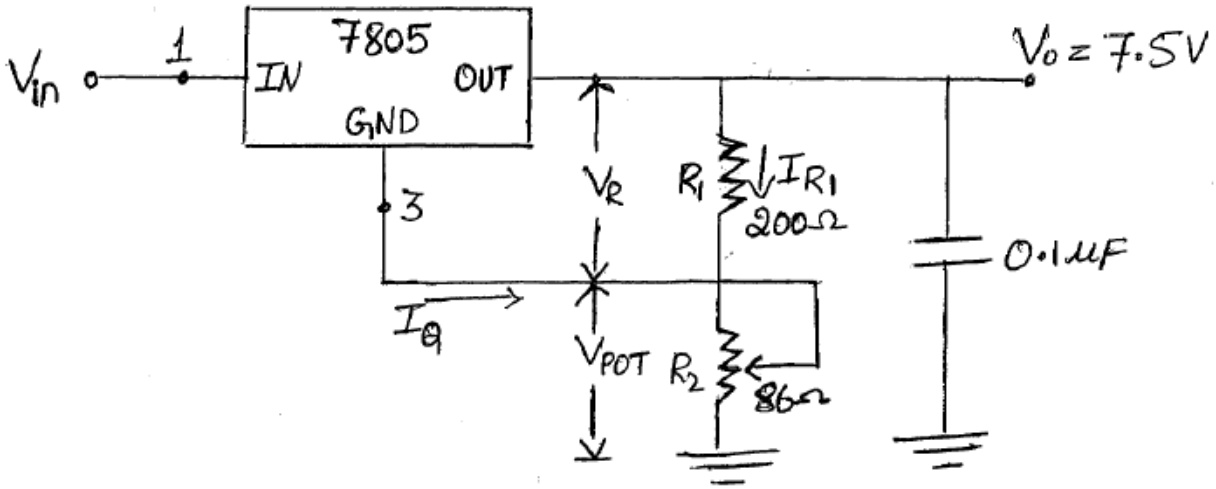
Sol: $V_{POT} = V_o - V_R = 7.5V - 5V$

$\boxed{V_{POT} = 2.5V}$

* $R_1 = \frac{V_R}{I_{R_1}} = \frac{5V}{25mA} = \underline{200\Omega}$

* $R_2 = \frac{V_{POT}}{(I_Q + I_{R_1})} = \frac{2.5V}{(4.2mA + 25mA)} = \underline{85.6\Omega}$

Choose $\boxed{R_2 = 86\Omega}$



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2) Design a 7805 regulator to get the o/p $V_o = 6.5V$

Given: $V_o = 6.5V$

For 7805, o/p vtg is 5V i.e; $\boxed{V_R = 5V}$ &

$\boxed{I_Q = 4.2mA}$

Assume: $I_{R_1} = 25mA$

Sol: $V_{POT} = V_o - V_R = 6.5V - 5V$

$\boxed{V_{POT} = 1.5V}$

* $R_1 = \frac{V_R}{I_{R_1}} = \frac{5V}{25mA}$

$\boxed{R_1 = 200\Omega}$

* $R_2 = \frac{V_{POT}}{[I_Q + I_{R_1}]} = \frac{1.5V}{(4.2mA + 25mA)}$

$\boxed{R_2 = 51.37\Omega}$

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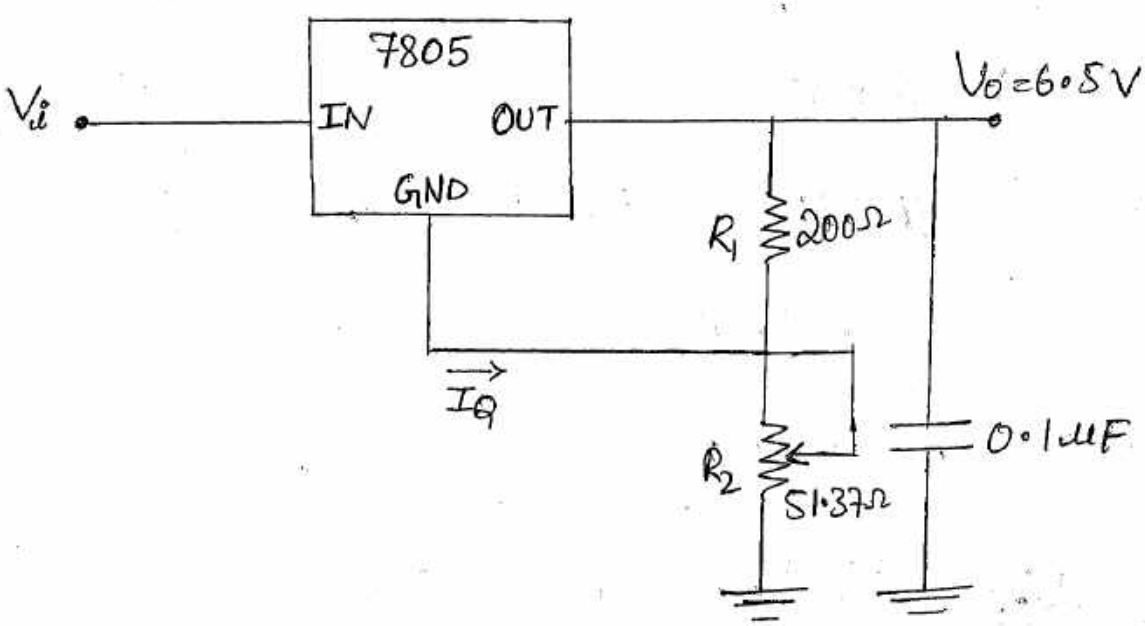

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Dual Voltage Supply:

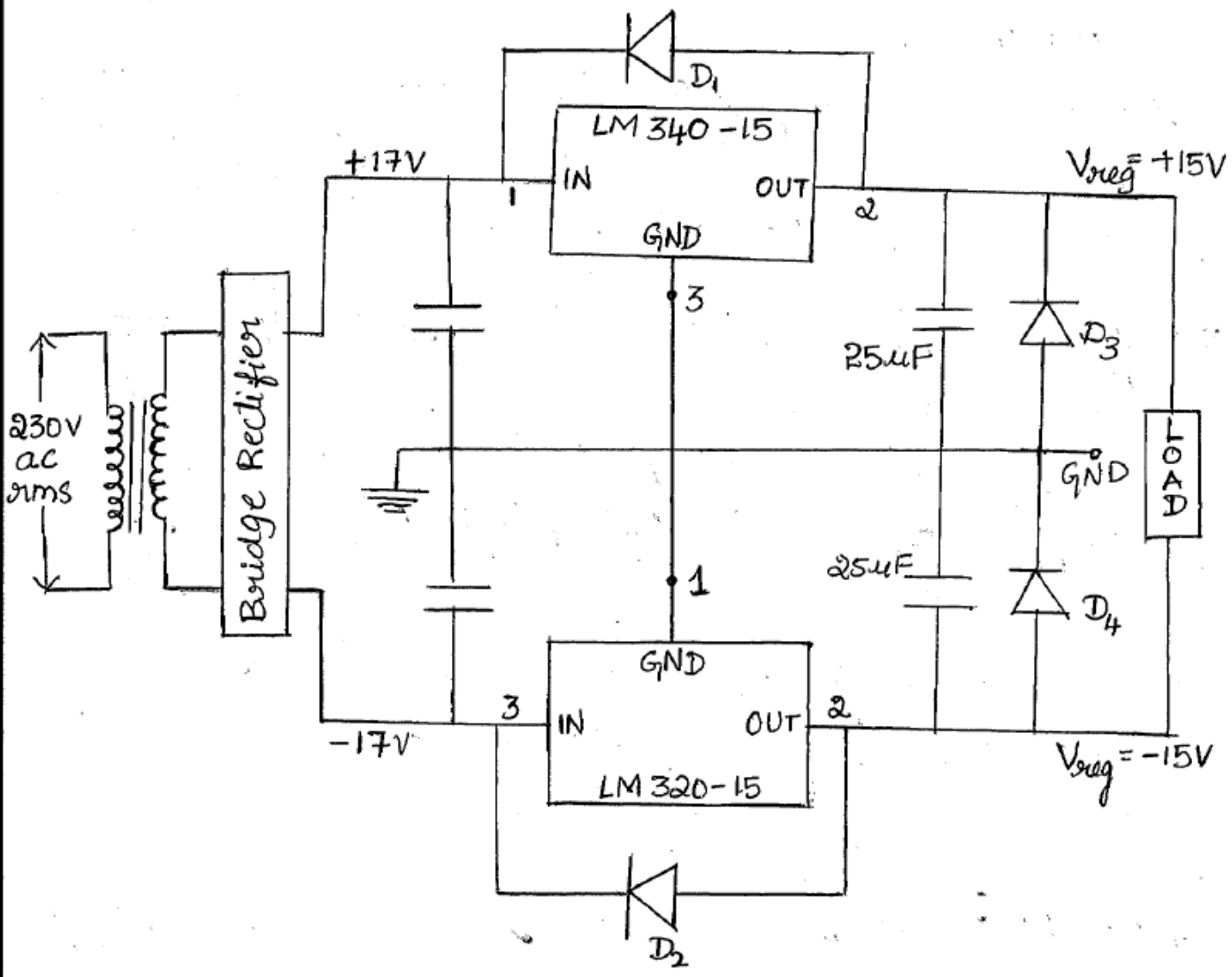

fig ①: Dual voltage ±15V Supply

* Three terminal fixed voltage regulators can be used to provide dual power supply required for op-amp.

The CKT shows a bipolar ±15V supply provided by two fixed voltage regulators LM 340-15 & LM-320-15.

The LM 340-15 is a +15V regulator &
LM 320-15 is a -15V regulator

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The pin configuration of LM340 & LM320 is different

* The diodes D_1 & D_2 in the CKt protect the regulator against short circuit occuring at its input terminals.

  Diodes D_3 & D_4 provide protection against the situation when both the regulators may not turn ON simultaneously.

* If there is a load between two o/p's, the faster one will reverse the polarity of other & causes it to latch up unless it is properly clamped and this clamping is done by the diodes.

* once the regulator starts operating properly, diodes are reverse biased & have no effect on circuit.

NOTE: LM325H is a dual tracking ±15V supply & is available in a IC [10-pin]

Demerits of 3-terminal IC regulators:

The three terminal IC regulators have the following limitation [drawback or demerits]

1) No short circuit protection

2) output voltage is fixed [either +ve or -ve]

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723 General purpose regulator :

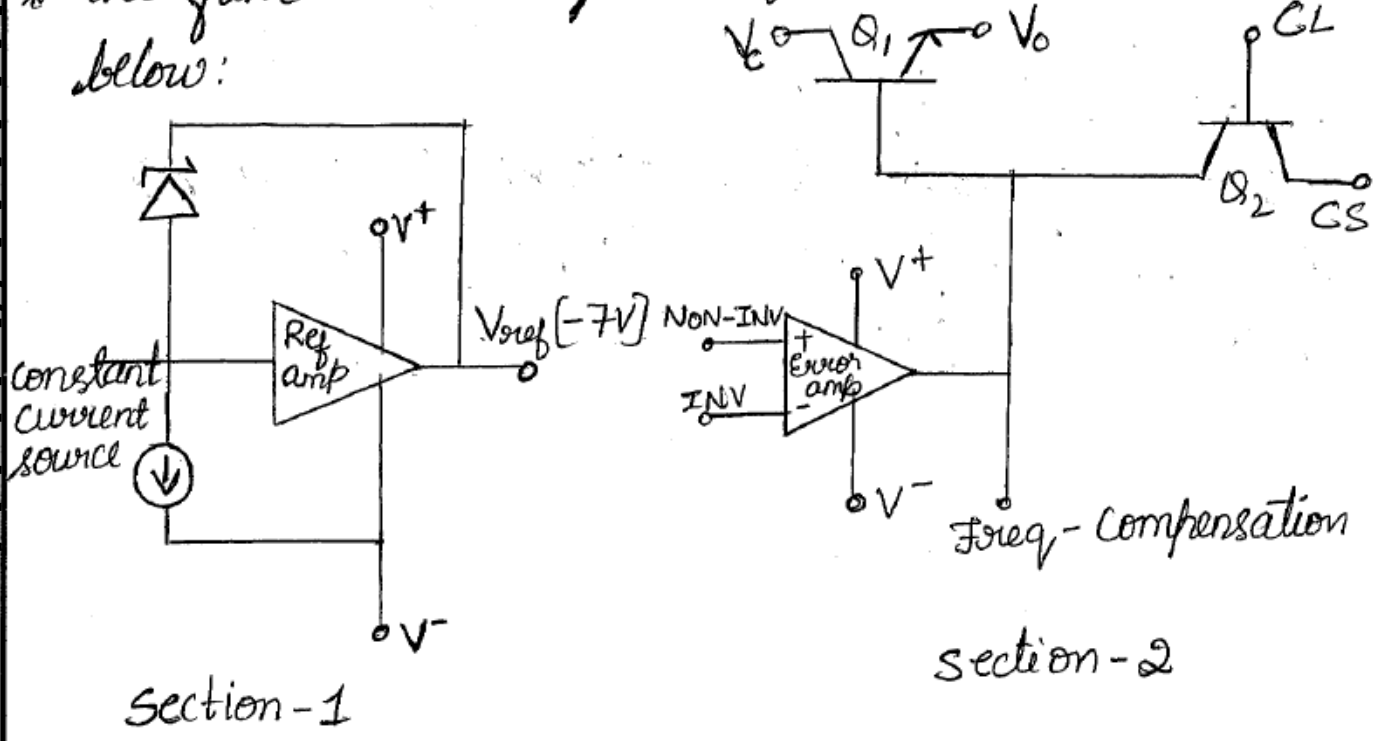
* Draw and explain the functional diagram of 723 IC

Model paper-1, 8M

or

* Draw the functional diagram of 723 regulator and explain it.

* IC 723 is a general purpose regulator, which can be adjusted over a wide range of both +ve & -ve regulated o/p voltage.
* IC 723 has a limitation that it has no inbuilt thermal protection. It also has no short circuit limits
* The functional diagram of IC 723 is as shown below:



* IC 723 has two sections. The section 1 has zener diode, a constant current source & reference amplifier produces a fixed voltage of 7V at V_{ref} terminal.

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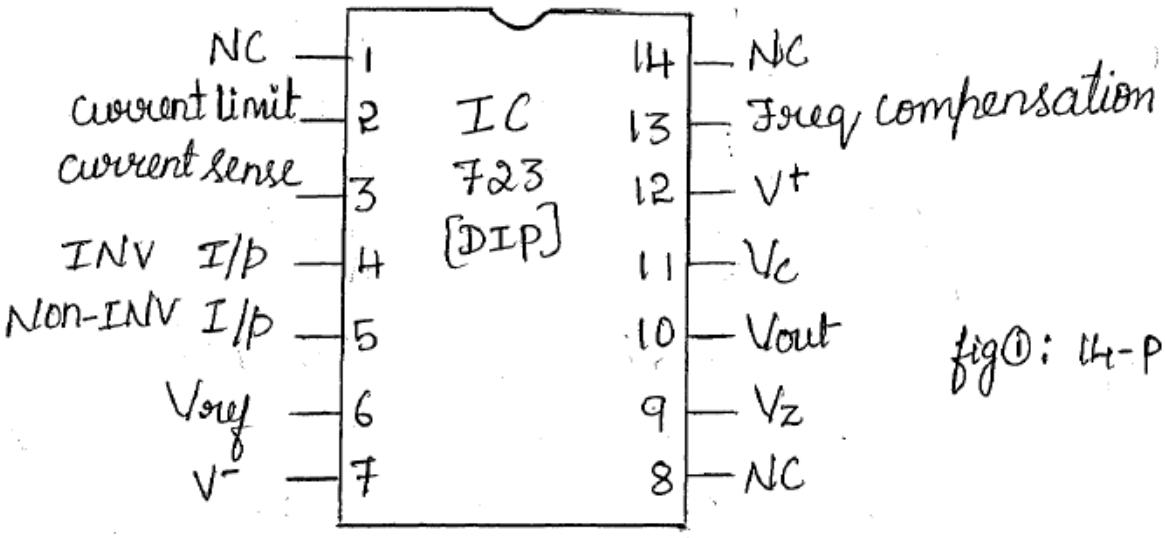
* The constant current source forces the zener to operate at fixed point so that the zener o/p's a fixed voltage.
* The section-2 consists of an error amplifier, a series pass transistor Q_1 and a current limit transistor Q_2
  The error amplifier compares a sample of the o/p voltage applied at the INV terminal with that of reference voltage [V_{ref}] applied at the Non-INV terminal.
* The error signal controls the conduction of Q_1. These two sections are internally not connected but are available on 723 IC regulator.

IC-723 Pin diagram:

* 723 IC regulator is available in a 14-pin Dual-in-line package & 10 pin metal-can package as shown below:



fig①: 14-pin DIP

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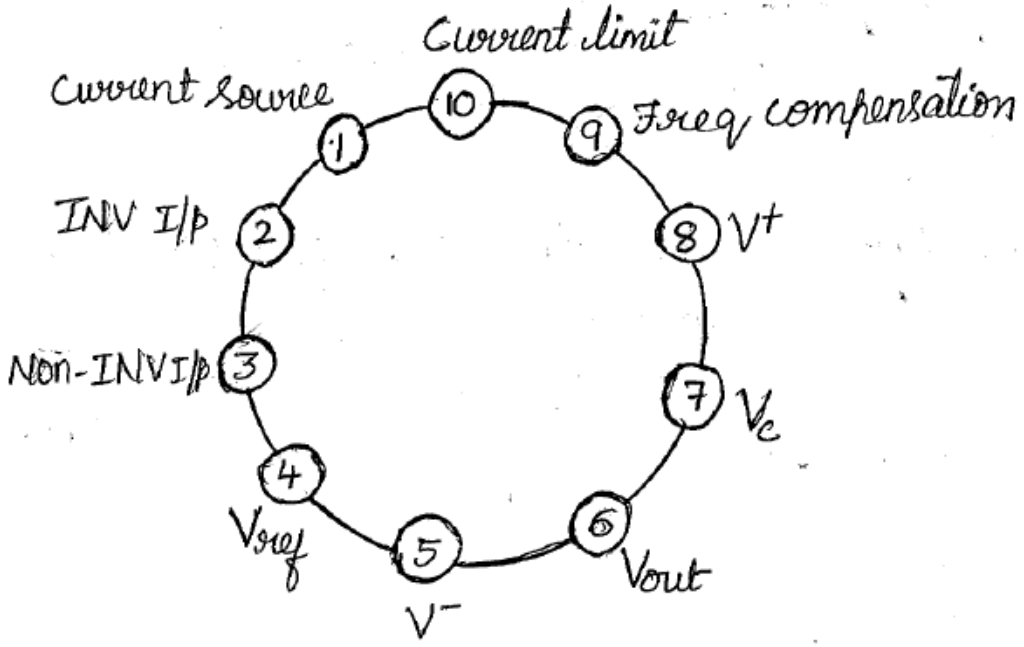

fig ②: 10-pin metal-can package

Low voltage regulator using 723 IC :-

1. Explain the application of IC 723 as basic low voltage regulator.

May-10, 6M

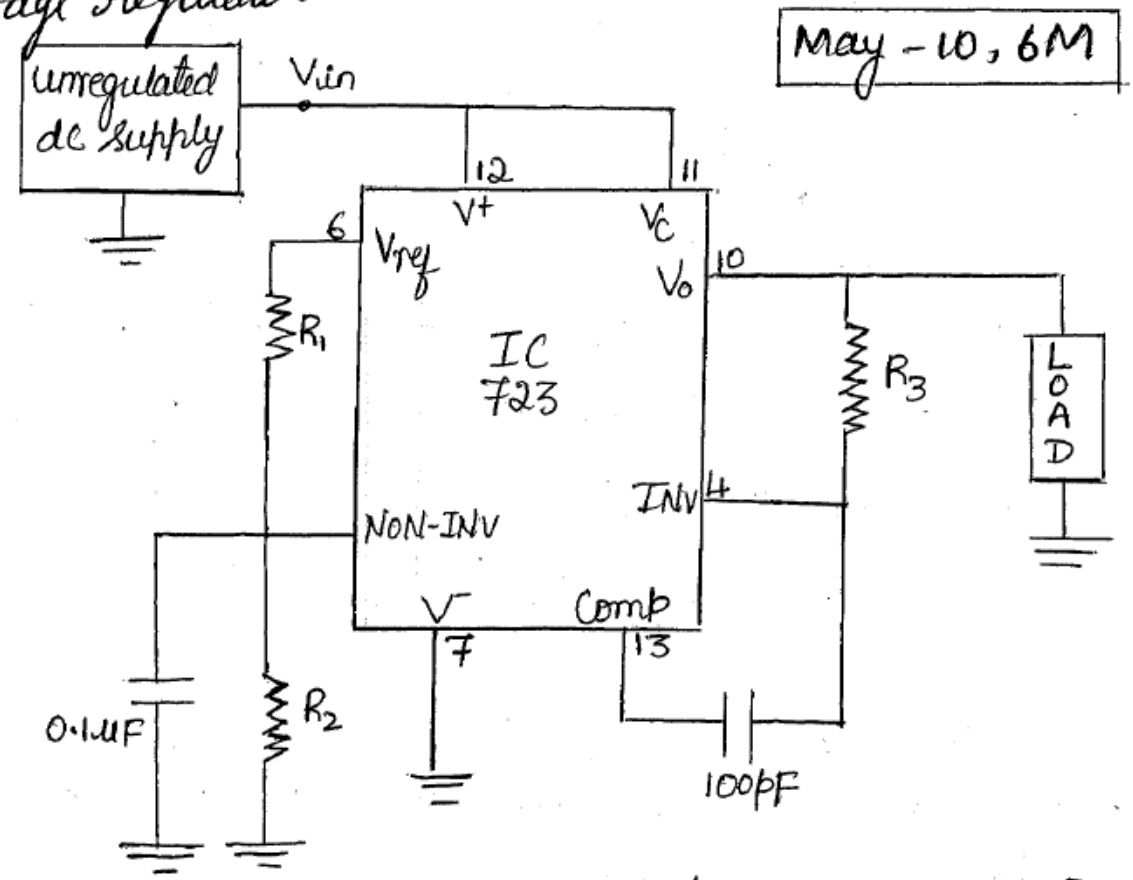

fig ④: A low voltage regulator using IC 723

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A simple positive low voltage [2V to 7V] regulator can be made using 723 as shown in fig @

* The voltage at the Non-INV terminal of the error amplifier due to R_1 & R_2 is

$$V_{NI} = V_{ref} * \frac{R_2}{R_1+R_2}$$

$\therefore V_{NI} = I \times R_2$

$V_{NI} = \frac{V_{ref}}{R_1+R_2} \cdot R_2$

* The difference b/w the voltage at NON-INV terminal and o/p voltage V_o (directly fed back) at INV terminal are the I/ps to the error amplifier.

* The o/p of the error amplifier drives the pass transistor Q_1. Since Q_1 is operating as emitter follower

$$V_o = V_{ref} \cdot \frac{R_2}{R_1+R_2}$$

* If o/p voltage becomes low i.e voltage at INV terminal goes down, this makes the o/p of the error amplifier to be more positive, thereby increasing the conduction of pass transistor Q_1 & thus o/p voltage across load increases.

Thus initial drop in voltage is <u>compensated</u>. Similarly any increase in load voltage or change in i/p voltage gets regulated.

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* The reference voltage is typically 7.15V, so o/p voltage is

$$V_o = 7.15 \cdot \frac{R_2}{R_1+R_2}$$

So o/p voltage will be always less than 7.15V. Thus fig @ is used as low voltage regulator.

FORMULAE

1) $V_o = V_{ref} \frac{R_2}{R_1+R_2}$

2) From above equation determine R_2 by assuming R_1 or vice versa.

3) $R_3 = R_1 \| R_2$

NOTE: $V_{ref} = 7V$

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1) Design a voltage regulator using IC 723 to get a voltage o/p of 3V.

Given: $V_o = 3V$

WKT $V_{ref} = 7V$

Soln: WKT

$$V_o = V_{ref} \frac{R_2}{R_1+R_2}$$

$$3 = 7 \frac{R_2}{R_1+R_2}$$

$$3R_1 + 3R_2 = 7R_2$$

$$4R_2 = 3R_1$$

$$R_2 = \frac{3}{4} R_1$$

Assume $\boxed{R_1 = 10K\Omega}$

$$R_2 = \frac{3}{4} \times 10K\Omega$$

$$\boxed{R_2 = 7.5K\Omega}$$

* $R_3 = R_1 \parallel R_2$

$$= \frac{R_1 \times R_2}{R_1+R_2}$$

$$= \frac{10K\Omega \times 7.5K\Omega}{10K\Omega + 7.5K\Omega}$$

$$\boxed{R_3 = 4.2K\Omega}$$

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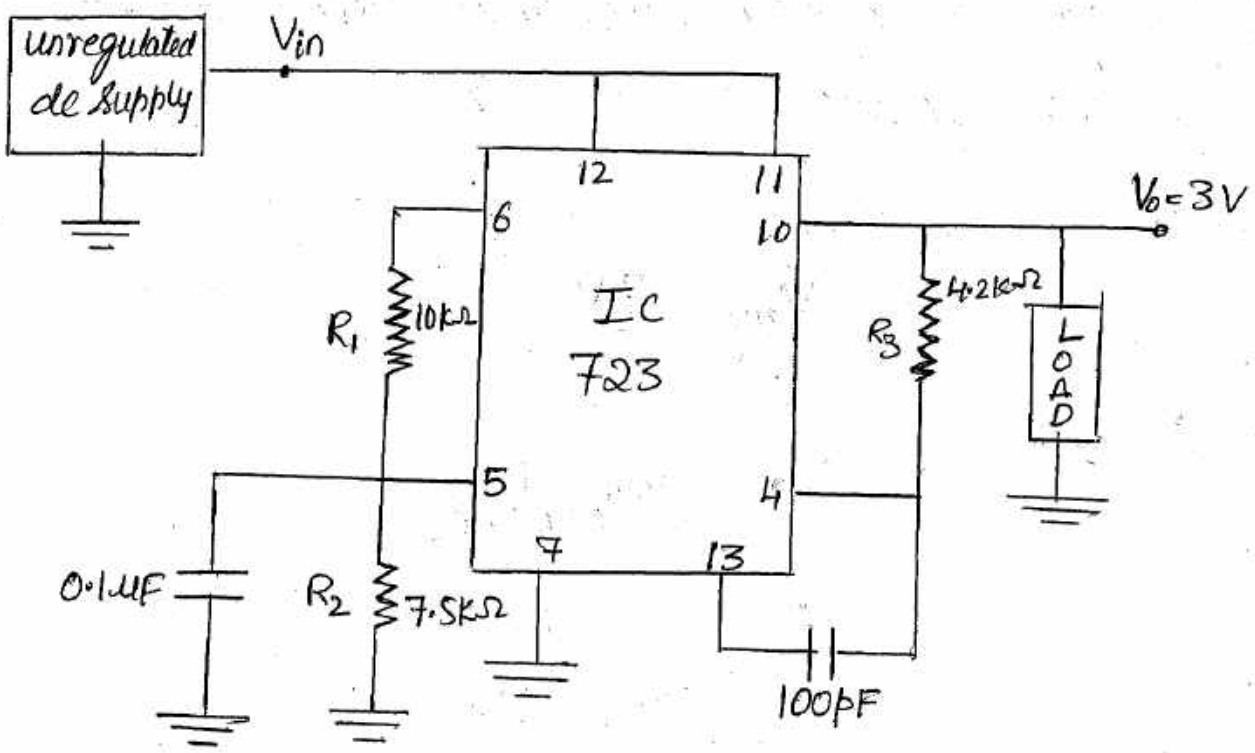

2) Design a voltage regulator using IC 723 to get a voltage o/p of 5V.

Jan-10, 8M

Given: $V_o = 5V$

WKT $V_{ref} = 7V$

Sol:

$$V_o = V_{ref} \cdot \frac{R_2}{R_1+R_2}$$

$$5 = 7 \cdot \frac{R_2}{R_1+R_2}$$

$$5R_1 + 5R_2 = 7R_2$$

$$5R_1 = 7R_2 - 5R_2$$

$$5R_1 = 2R_2$$

$$R_2 = \frac{5}{2} R_1$$

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$R_2 = 2.5 R_1$

Assume $\boxed{R_1 = 10K\Omega}$

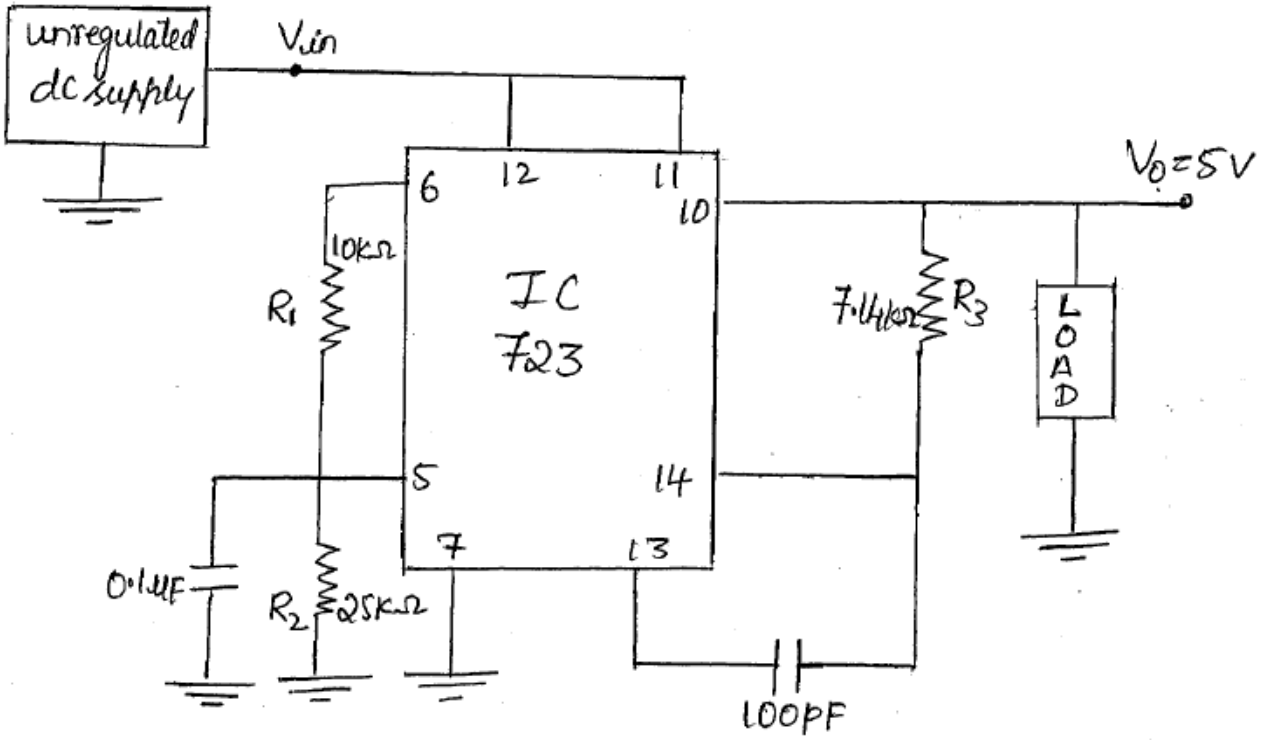
$R_2 = 2.5 \times 10K\Omega$

$\boxed{R_2 = 25K\Omega}$

* $R_3 = R_1 \| R_2 = \dfrac{R_1 \times R_2}{R_1 + R_2}$

$R_3 = \dfrac{10K\Omega \times 25K\Omega}{10K\Omega + 25K\Omega}$

$\boxed{R_3 = 7.14K\Omega}$



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IC 723 as High Voltage Regulator : [$V_o > 7V$]

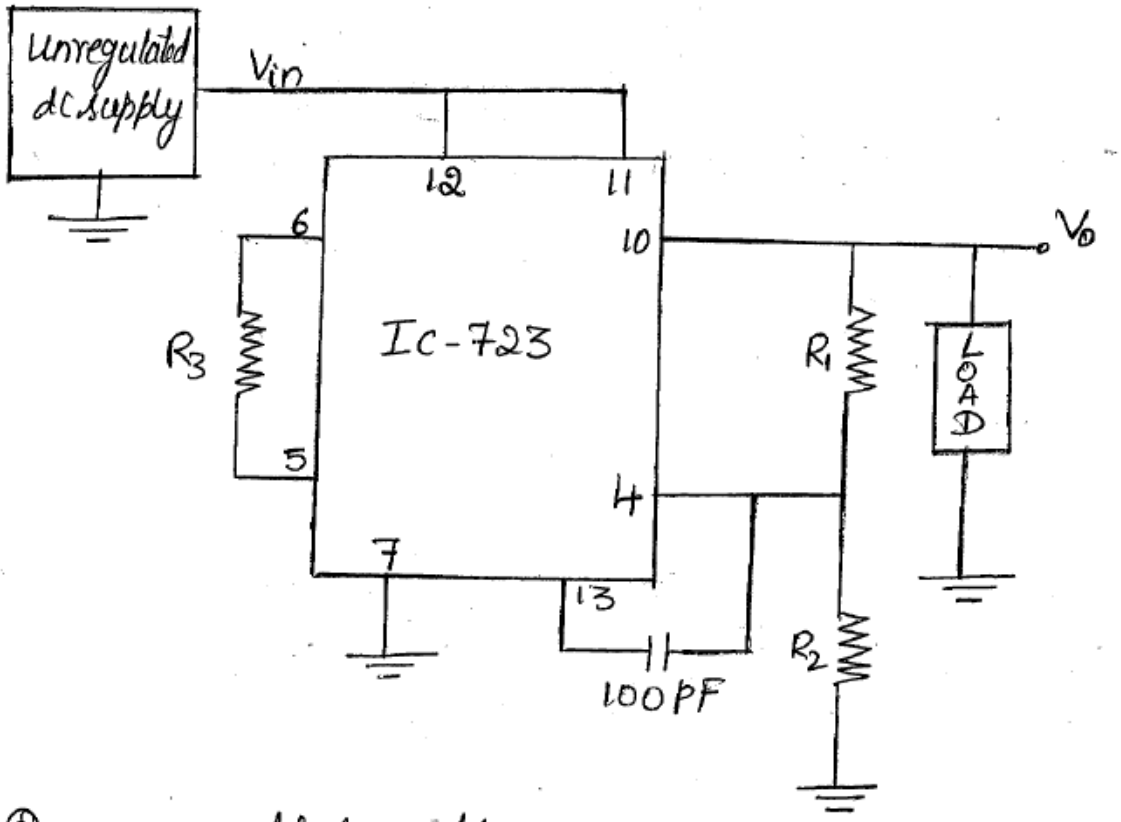

fig @ : Basic high voltage 723 regulator

Fig @ show the basic high voltage 723 voltage to get o/p voltage greater than 7V.

* The Non-INV terminal is directly connected to V_{ref} through R_3. Hence voltage at Non-INV terminal is

$$V_{NI} = V_{ref} = 7.15\,V$$

* The error amplifier acts as Non-INV amplifier with a voltage gain of

$$A_V = 1 + \frac{R_1}{R_2}$$

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* The o/p voltage of the ckt is

$$V_o = 7.15\left(1+\frac{R_1}{R_2}\right)$$

Thus regulated o/p voltage is greater than 7.15V

FORMULAE

1) $V_o = 7\left(1+\frac{R_1}{R_2}\right)$

2) From above equation determine R_2 by assuming R_1 or vice-versa.

3) $R_3 = R_1 R_2$

Note : $V_{ref} = 7V$

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1) Design a high voltage 723 regulator so as to get an o/p voltage of 25V.

June-08, 7M

Given: $V_o = 25V$

Assume $V_{ref} = 7V$

Sol: WKT

$$V_o = V_{ref}\left(1 + \frac{R_1}{R_2}\right) \leftarrow (1M)$$

$$25V = 7V\left(1 + \frac{R_1}{R_2}\right)$$

$$\frac{25V}{7V} = 1 + \frac{R_1}{R_2}$$

$$3.57 = 1 + \frac{R_1}{R_2}$$

$$\frac{R_1}{R_2} = 2.57$$

$$R_1 = 2.57 R_2 \leftarrow [1M]$$

Assume $R_2 = 10K\Omega$

$$R_1 = 2.57 \times 10K\Omega$$

$$R_1 = 25.7K\Omega \leftarrow [1M]$$

* $R_3 = R_1 R_2$

$= 25.71K\Omega \times 10K\Omega$

$R_3 = 257.14 M\Omega \leftarrow [1M]$

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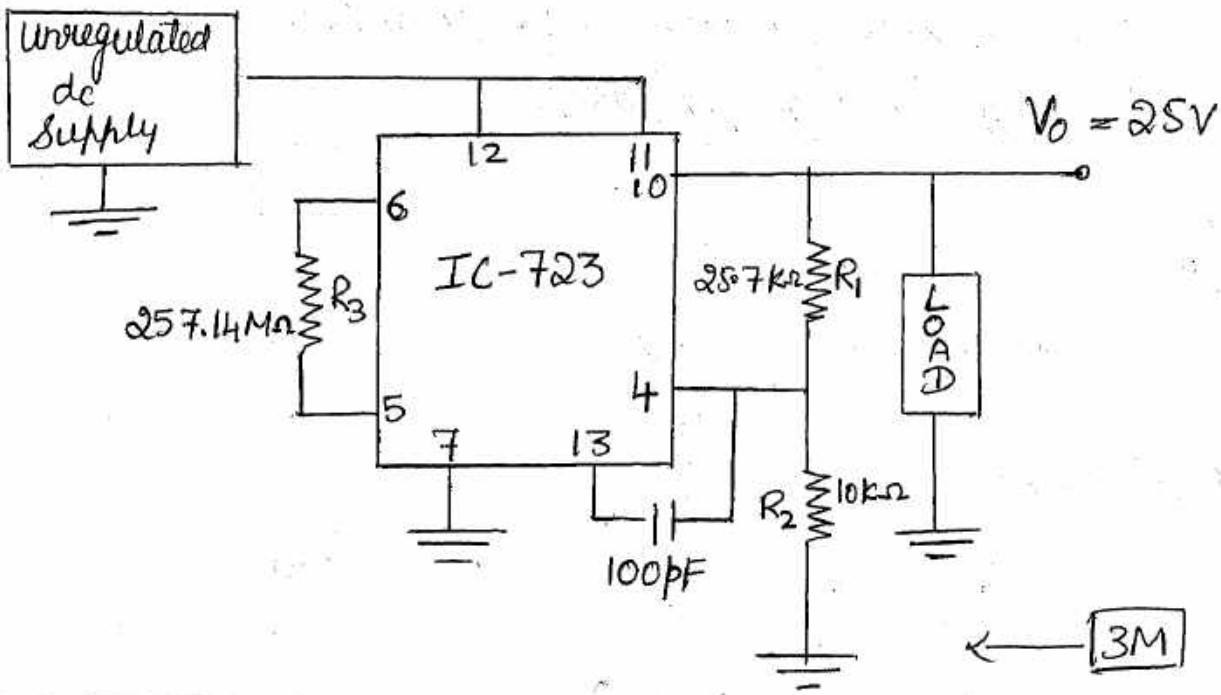

2) Design a high voltage regulator to get a o/p voltage of 28 volts.

Given: $V_o = 28V$

WKT $V_{ref} = 7V$

Sol: WKT $V_o = V_{ref}\left(1 + \frac{R_1}{R_2}\right)$

$28V = 7V\left(1 + \frac{R_1}{R_2}\right)$

$\frac{28}{7} = 1 + \frac{R_1}{R_2}$

$4 = 1 + \frac{R_1}{R_2}$

$\frac{R_1}{R_2} = 4 - 1$

$R = 3R_2$

assume $\boxed{R_2 = 1K\Omega}$

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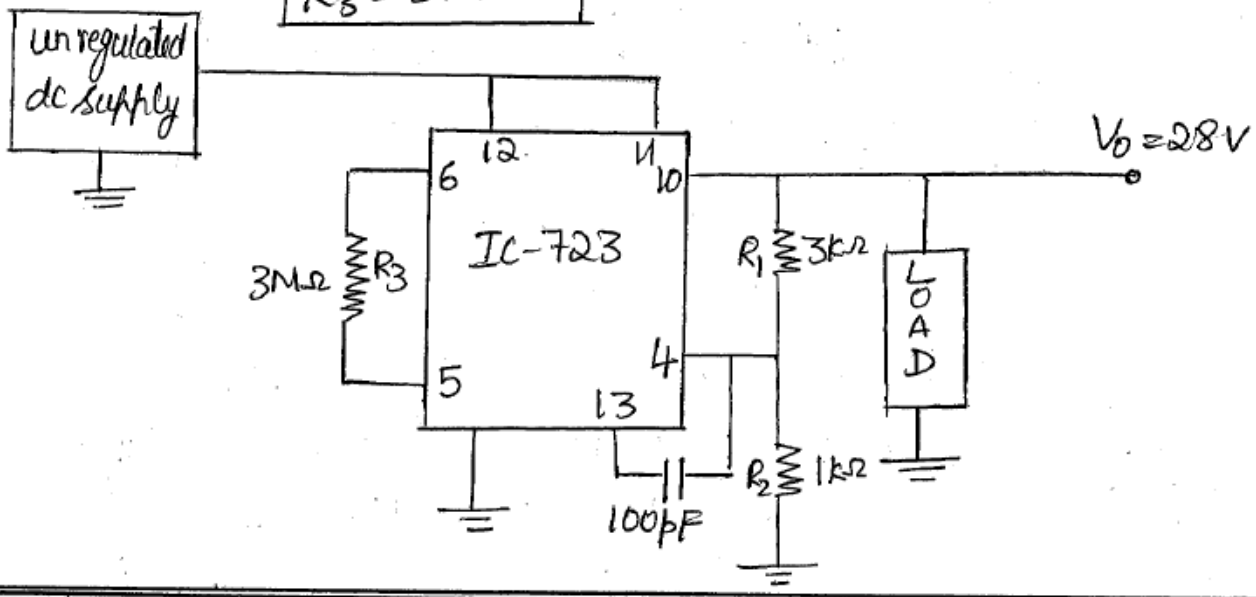
$R_1 = 3 \times 1K\Omega$

$\boxed{R_1 = 3K\Omega}$

* $R_3 = R_1 R_2 = 1K\Omega \times 3K\Omega$

$\boxed{R_3 = 3M\Omega}$



3) Design a 723 based voltage regulator to provide constant $V_o = 20V$ and $I_{o\,max} = 250mA$

Given $V_{in\text{-}unreg} = 30V \pm 10\%$.

Jan 2011, 6M

Given :- $V_o = 20V$ $I_{o\,max} = 250mA$

$V_{in\text{-}unreg} = 30V + 10\%$

Sol: WKT $V_o = 7.15\left(1 + \frac{R_1}{R_2}\right)$ ← 1M

$\frac{20V}{7.15V} = 1 + \frac{R_1}{R_2}$

$2.797 - 1 = \frac{R_1}{R_2}$

$R_1 = 1.797\, R_2$

Assume $\boxed{R_2 = 10K\Omega}$ ← 1M

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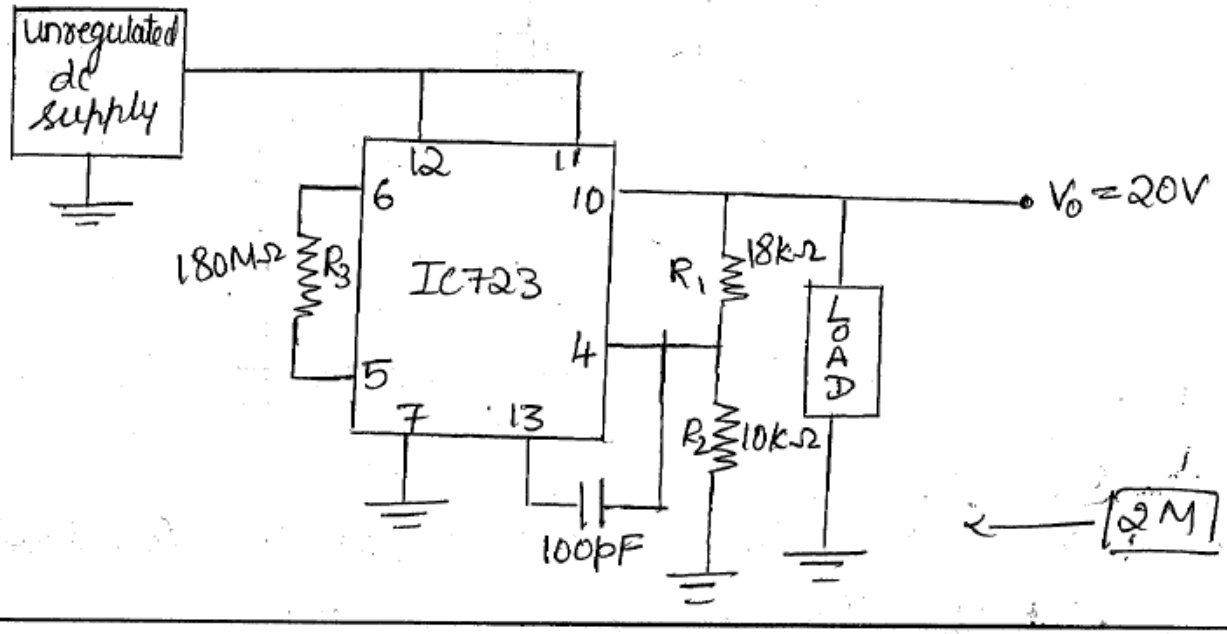
$R_1 = 1.797 \times 10K\Omega$

$R_1 = 17.97\ K\Omega$

Choose $\boxed{R_1 = 18K\Omega}$ ← 1M

* $R_3 = R_1 R_2 = 18K\Omega \times 10K\Omega$

$\boxed{R_3 = 180\ M\Omega}$ ← 1M



NOTE: Given $I_{o\,max} = 250mA$

& $V_{BE} = 0.7V$

$V_{CE\,max} = V_{in(max)} - V_o = 33V - 20V$

$\boxed{V_{CE\,max} = 13V}$

* $R_{sc} = \dfrac{V_{BE}}{I_{o\,max}} = \dfrac{0.7V}{250mA}$

$\boxed{R_{sc} = 2.8\Omega}$

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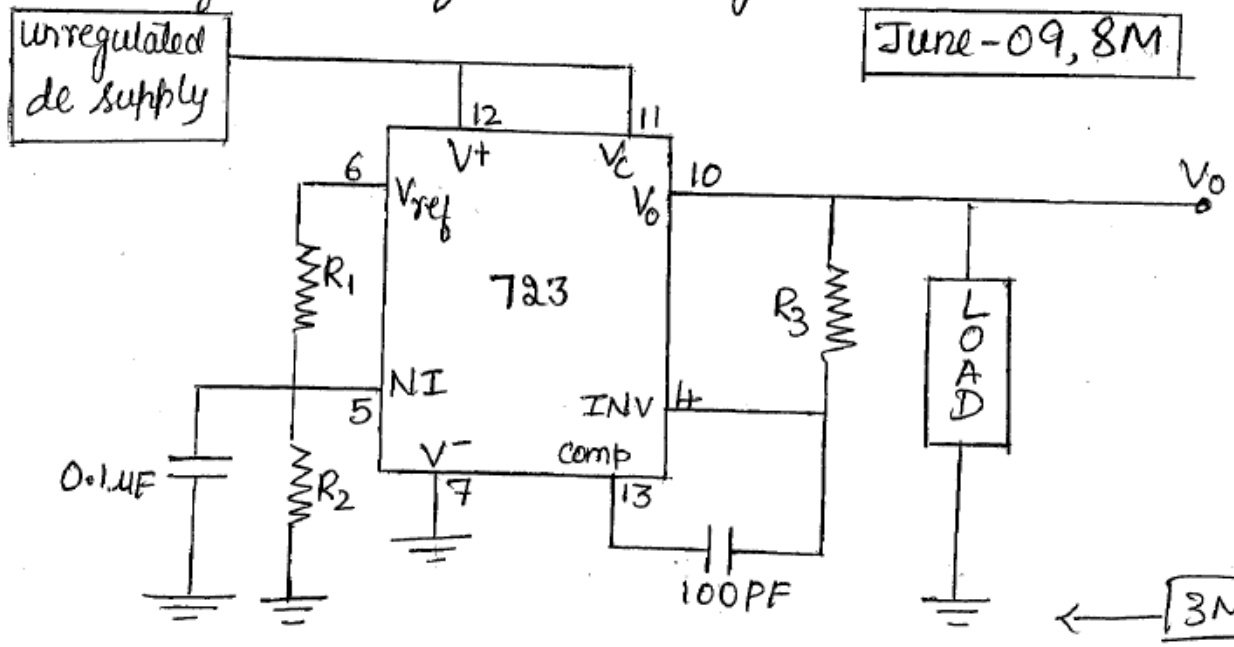
* With a neat schematic diagram, explain the salient features of a 723 regulator.

June-09, 8M



← 3M

The salient features of a 723 regulators are ← 5M

1) It works as voltage regulator at o/p voltage ranging from 2V to 37V at currents upto 150mA
2) Input and output short-circuit protection is provided.
3) It has good line and load regulation
4) Low temperature drift and high ripple rejection
5) Low stand by current drain
6) Small size, lower cost.
7) It can be used at load currents greater than 150 mA with external pass transistor.

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Current Limit protection :-

* Explain the working of a series voltage regulator, with current limit protection.

Jan-2011, 8M

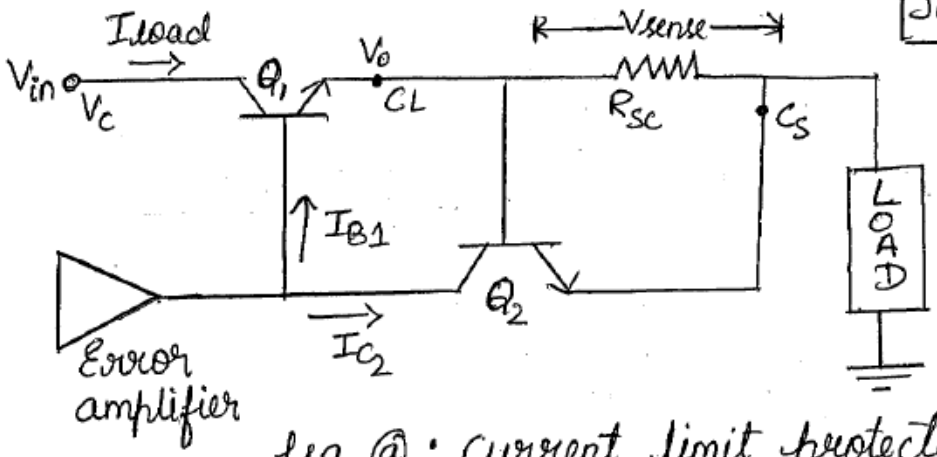

fig ⓐ : Current limit protection ckt → 3M

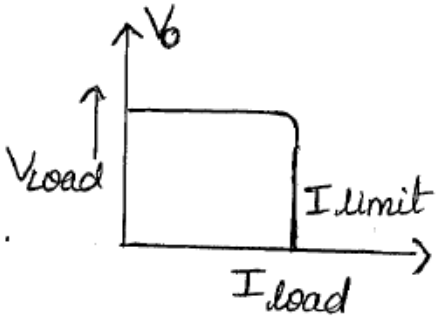

fig ⓑ : Characteristic curve for a current limited regulator

* The low and high voltage regulators using 723 IC have no short circuit protection. If the IC tries to drive very large current at constant o/p voltage then the IC gets hotter and may burn out.
* The IC is therefore, provided with a current limit facility. The ability of the regulator to prevent the load current from increasing beyond certain limit is called "current limiting" & is denoted by I_{limit}.
* The o/p voltage remains constant for load current below I_{limit}. As the current approaches to the limit,

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the o/p voltage drops to zero, as shown in fig (b), thus protecting the regulator from high current.

* The current limit I_{Limit} is set by connecting an external resistor R_{SC} between the terminals CL and CS terminals as shown in fig (a).

The CL terminal is also connected to the o/p terminal V_O and CS terminal to the load.

* The load current produces a small voltage drop V_{sense} across R_{SC}, when $V_{sense} \approx 0.5V$, the transistor 'Q_2' begins to turn ON [since - $V_{sense} = V_{BE2}$]

Now current I_{C_2} starts flowing into the collector of Q_2 and the base current to Q_1 reduces. As a result, the emitter current of Q_1 also decreases i.e; load current is decreased.

SO any increase in the load current will get nullified (& vice-versa)

* WKT $V_{sense} = V_{BE2} = 0.5V$

$$I_{limit} = \frac{V_{sense}}{R_{SC}}$$

$$R_{SC} = \frac{V_{sense}}{I_{limit}}$$

Explanation ← 5M

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1) Design a current limit circuit for a723 regulator to limit the current of 60mA

Given: $I_{sc} = 60mA$

WKT

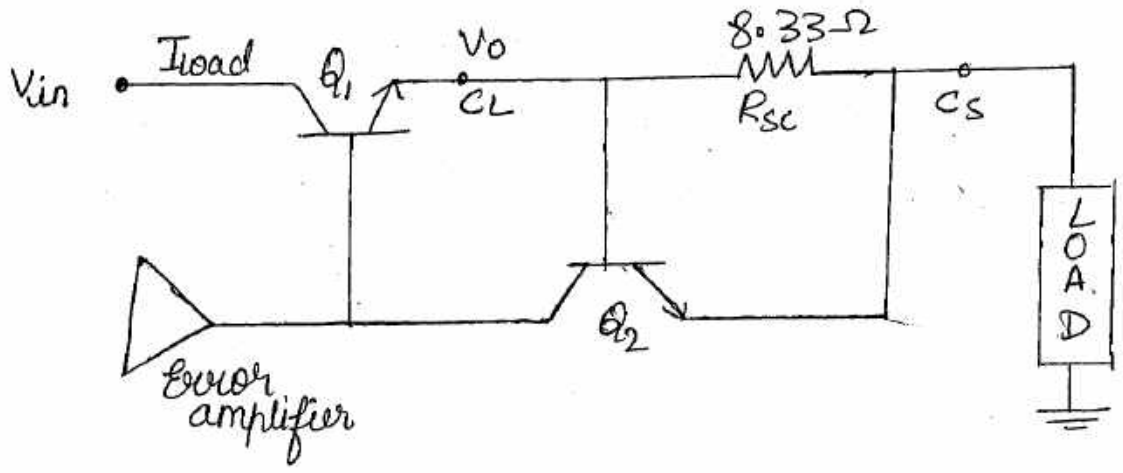
$V_{sense} = 0.5V$

Sol:

WKT

$$R_{sc} = \frac{V_{sense}}{I_{limit}} = \frac{0.5V}{60mA}$$

$$\boxed{R_{sc} = 8.33\Omega}$$



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Current fold back :

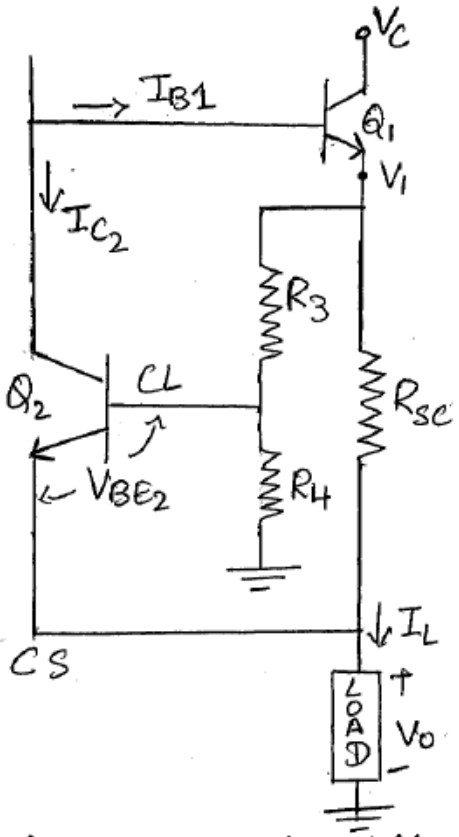

fig @ current foldback

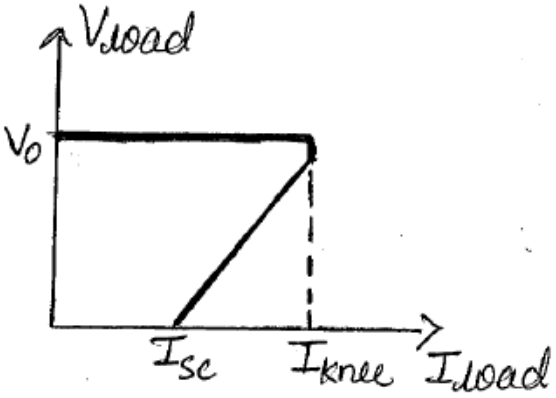

fig ⓑ : current fold back characteristic curve

* If the load is short circuited, the voltage V_o becomes zero and a large current flows through the regulator. To protect the regulator, current foldback method is used.
* Fig ⓑ shows the current fold back characteristic curve. when load goes on increasing, the o/p voltage V_o is held constant till a value I_{knee}. once the load current tries to increase beyond this, the current fold-back ckt decreases both o/p voltage and o/p current.
* Fig @ shows the current foldback CKT. The voltage at base of Q_2 is divided by R_3-R_4 network. Q_2 conducts only when $V_{BE2} = 0.5V$ i.e; the voltage drops across R_{sc}.

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* As Q_2 conducts, I_{C_2} flows more and thereby decreasing I_{B_1}. Thus Q_1 turns off and I_L decreases. This decreases V_1, thus voltage at base of Q_2 also drops i.e; $\frac{VR_4}{R_4+R_3}$

* This process continues till $V_0 = 0V$ & V_1 is equal to 0.5V.

Current Boosting in 723 IC :-

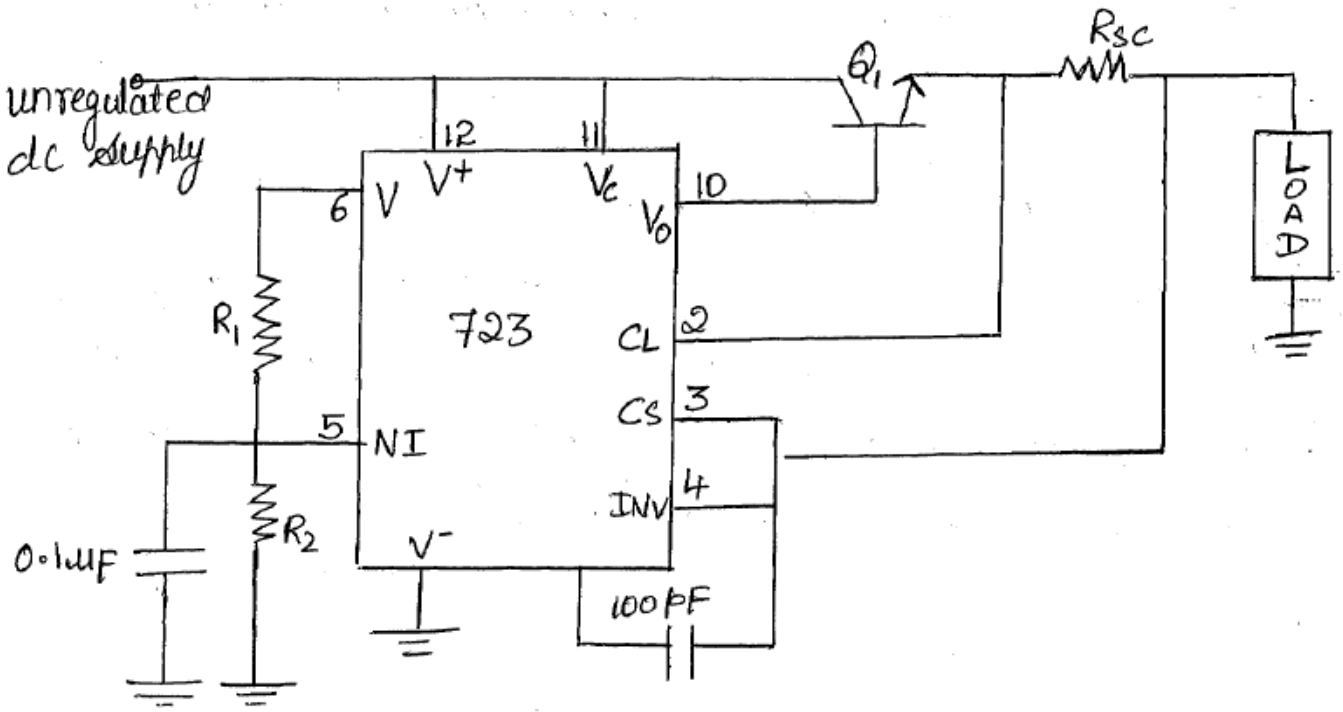

fig @ : current Boosted low voltage regulator

* The maximum current that 723 IC regulator can provide is 140mA. For many applications this current is not sufficient.

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It is possible to boost the current level by adding a boost transistor Q_1 to the voltage regulator as shown in fig @.

* The unregulated dc supply Vin supplies the collector current to Q_1.
The o/p current from pin-10 is connected to the base of pass transistor Q_1. This base current gets multiplied by β of pass transistor Q_1.

$$\therefore \boxed{I_L = \beta \times I_{O(723)}}$$

NOTE:

* β varies from 15 to 50
* $I_{O(723)} = 140\ mA$

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Limitation of Linear Voltage Regulators:

1) The required input step down transformer is bulky and expensive

2) Due to low line frequency (50 Hz), large values of filter capacitors are required.

3) The efficiency is very low.

4) I/p must be greater than the O/p voltage.

5) As large is the difference blw i/p & o/p voltage, more is the power dissipation in the series pass transistor

6) For higher t/p voltages, efficiency decreases.

7) The need for dual supply is not economical & flexible to achieve with the help of linear regulators.

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Switching Regulator or Switch mode power Supplies

1) Explain the principle of operation of a switching regulator. Discuss its advantages & disadvantages.

Jan-10, 8M

2) Explain the principle of switch mode power supplies. Enumerate their advantages and disadvantages.

June-10, 8M

3) What is the principle of Switch-mode power supplies? Discuss their advantages and disadvantages.

June-08, 6M
June-09, 6M

* In switching regulator, the pass transistor is used as a "controlled switch" and is operated at either cut off or saturated state. Hence power transmitted across the transistor is in discrete pulses (i.e; ⎍⎍⎍)
* when transistor is in cut-off region, there is no current & dissipates no power.

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* when transistor is in saturation region, a negligible voltage drop appears across it & thus power dissipation is very less. Hence power transmitted increases and also the efficiency (70% to 90%)

* Switching regulator uses concept of pulse width modulation to control the average value of o/p voltage.
If the duty cycle varied as shown in fig ①, the average value of the voltage changes w.r.t duty cycle.

$$\therefore \text{Duty cycle} = \frac{t_{ON}}{t_{ON} + t_{off}}$$

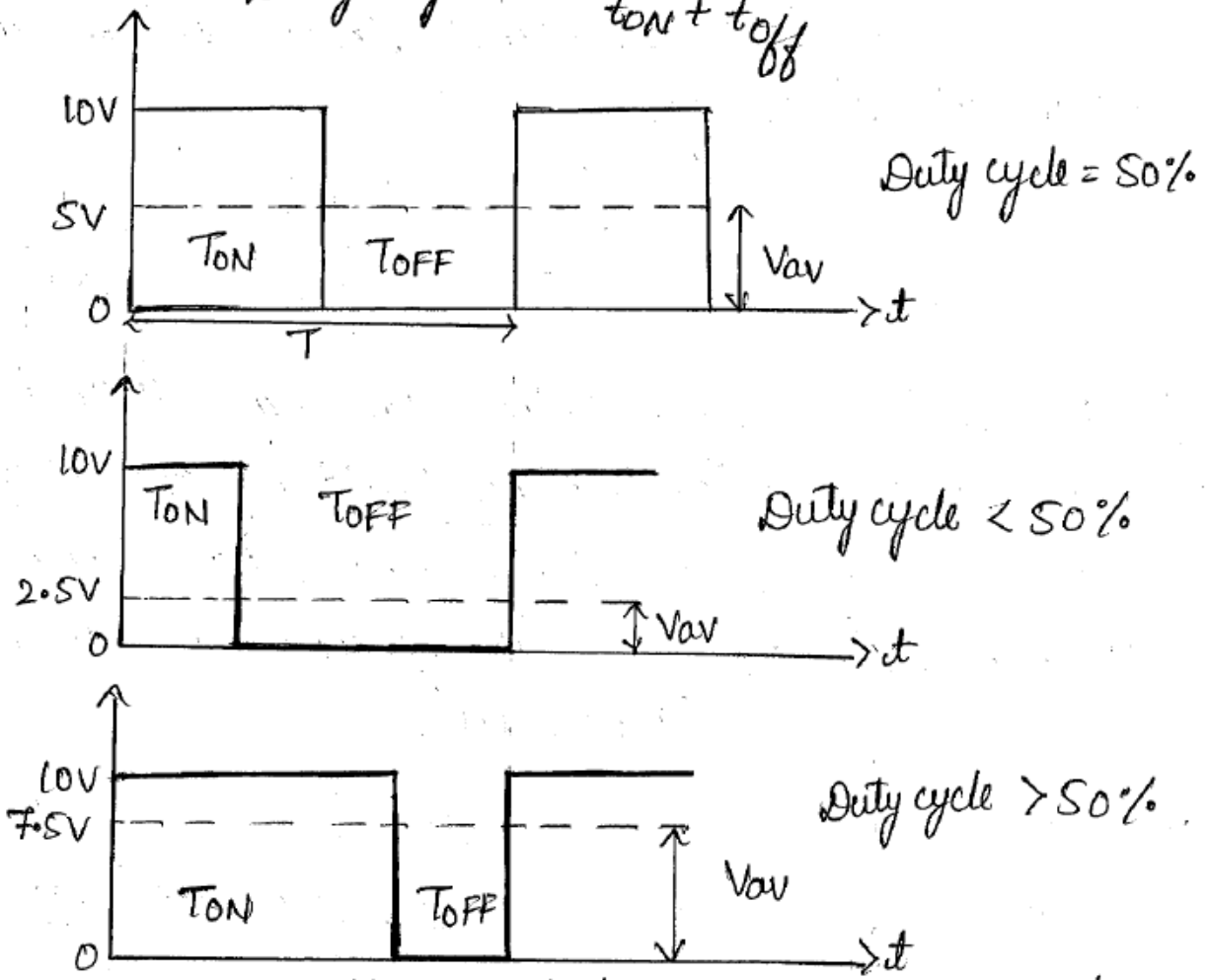

fig ①: Pulse width Modulation and average value

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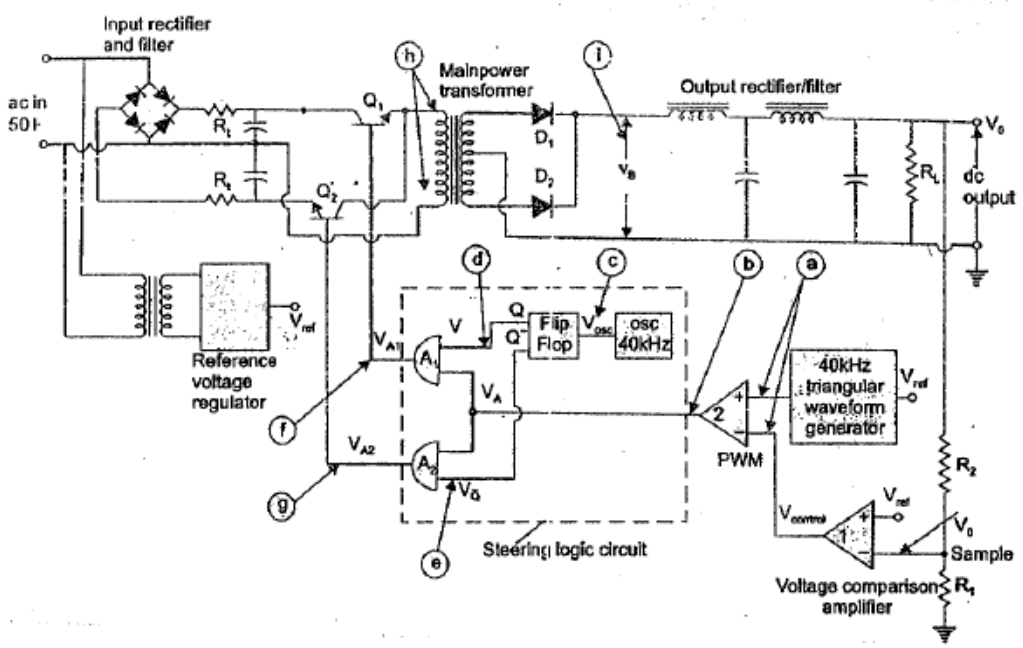

fig ① shows a switching power supply

* The bridge rectifier and capacitor filters are connected directly to the ac line to give unregulated dc input. The thermistor R_{th} limits the high initial capacitor charge current.
* Transistors Q_1 & Q_2 are alternatively switched OFF & ON at 20KHz. These transistors are either fully ON or cut-off, so they dissipate very little power.
* The transistors Q_1 & Q_2 drives the primary of the main transformer. The secondary is

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centre tapped & full wave rectification is achieved by diodes D_1 & D_2. This unidirectional square wave is next filtered through a two stage LC filter to produce o/p voltage V_o.

* The regulation of V_o is achieved by the feedback ckt consisting of a pulse width modulation & steering logic ckt.
The fraction of the o/p i.e; $\frac{R_2}{R_1+R_2} V_o$ is feedback to the INV input of the comparator 1 & is compared with a fixed reference voltage V_{ref} in comparator 1.

* The o/p of comparator 1 is called $V_{control}$ & is applied to the (−) input terminal of comparator 2 & a triangular waveform of frequency 40KHz is applied at the (+) input terminal.
(It may be noted that a high frequency triangular waveform is being used to reduce the ripple)

* The comparator 2 functions as a pulse width modulator & its o/p is a square wave V_A of period 'T'
The duty cycle of the square wave is $\frac{T_{ON}}{T_{ON}+T_{OFF}}$
and varies with $V_{control}$ which inturn varies with

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the variation of o/p V_o.

* The o/p V_A drives a steering logic ckt shown in dashed blocks.

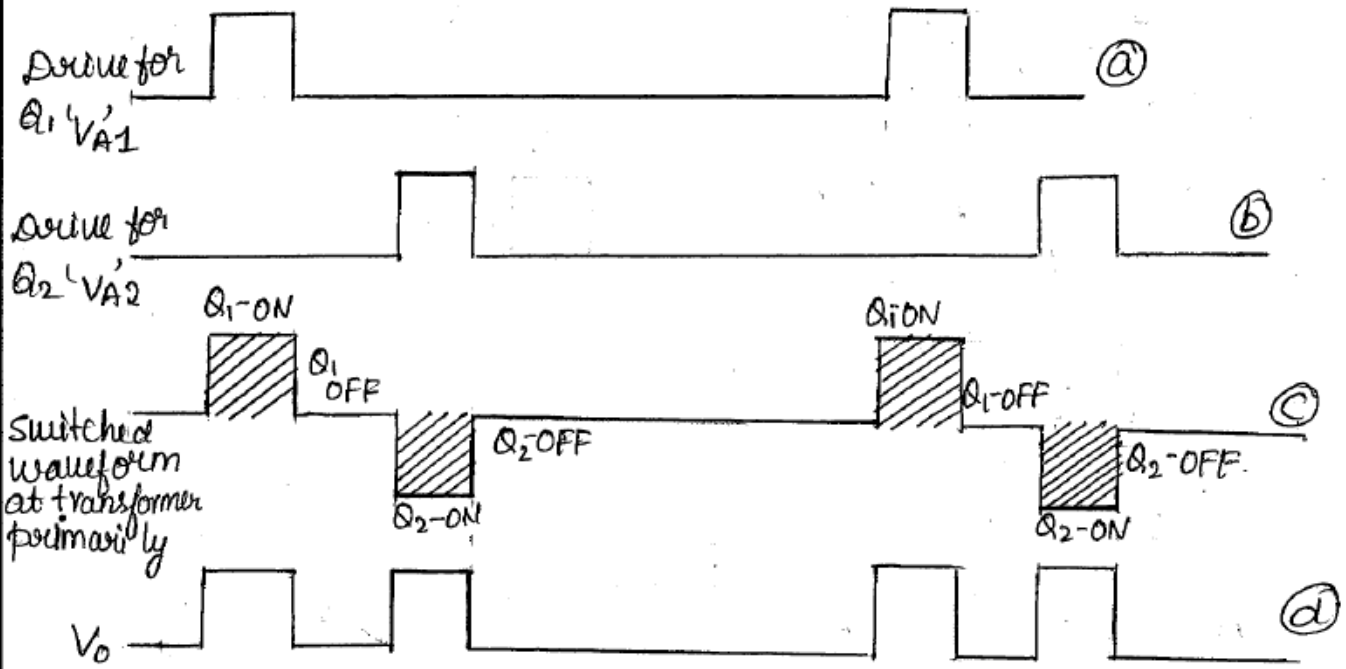

fig ③ : switching power supply wave form

* The o/p V_{A1} & V_{A2} of AND gates A_1 & A_2 are shown if fig ③ – @ & ⑥.

These waveforms are applied at the base of transistor Q_1 & Q_2. Depending upon whether Q_1 or Q_2 is ON, the waveform at the i/p of the transformer will be a square wave as shown in fig ©

The rectified o/p V_B is shown in fig ⓓ

* By using switch [transistor] with low losses and a filter with high quality factor, the conversion efficiency can easily exceed 90%.

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* If there is a rise in dc o/p voltage V_o, the voltage control $V_{control}$ of the comparator 1 also rises. Now time period T_1 decreases. This inturn decreases the pulse width of the waveform driving the main power transformer.
Reduction in pulse width lowers the average value of the dc o/p voltage V_o. Thus the initial rise in the dc o/p voltage V_o has been nullified.

Advantages:

1) Efficiency is high [70% to 90%]
2) Decrease in size and cost.
3) The high operating frequency used for the switching transistor allows the use of smaller transformer.
4) The power dissipation of pass transistor is very small.
5) Small o/p filters.

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Disadvantages:

1) Design is complex.
2) Ripple voltage is higher compared to linear regulator.
3) The response to load variations in not fast as compared to linear regulators.
4) Electromagnetic & radio frequency interference occurs.
5) A Switch mode power supply requires external components like inductors & transformers.

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Comparison of Linear regulators & Switching regulators :-

Sl No	Linear regulator	Switching regulator (SMPS)
1)	Efficieney is low	Efficieney is high
2)	cost is low	cost is high
3)	Design is simple	Design is complex
4)	Ripples are less at o/p.	Ripples are more at the o/p
5)	Power handling capacity is low	Power handling Capacity is high
6)	No switching losses	switching losses are high
7)	Response to load variation is fast	Response to load variation is slow.
8)	weight is high	It is light in weight.
9)	Due to low line frequency large filter capacitors are required.	High switching frequency allows small values of choke & capacitor
10)	Power transmitted across a transistor is in linear fashion	Power transmitted across a transistor is in the form of discrete pulse.
11)	series pass transistor does not act as a switch	series pass transistor acts as a switch.

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Other Linear IC Applications

555 Timer:

* The IC 555 timer is one of the most versatile linear IC used for generating accurate time delay or oscillation.
* IC555 timer is available in two packages
  i] 8-Pin Circular Style &
  ii] 8-Pin DIP type.

Features of IC 555 timer:

1) It operates on +5V to +18V.
2) It has adjustable duty cycle.
3) High temperature stability.
4) High current output. [200mA Sink or Source]
5) Low cost.
6) Operated in two modes:
   i) Monostable Multivibrator mode and
   ii) Astable or free running mode.

Applications of 555 timer:

1) Monostable and Astable multivibrator.
2) Oscillator
3) Ramp and Square wave generator.
4) Pulse generator.
5) Burglar alarm.

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6> Traffic light Control and
7> Voltage Monitor etc.

Functional Digram or Block Digram of 555 timer:

* Draw and Explain the functional diagram of 555 timer.

June-10, 6M

* Explain the functional diagram of IC 555 with a neat Sketch

Jan-10, 10M

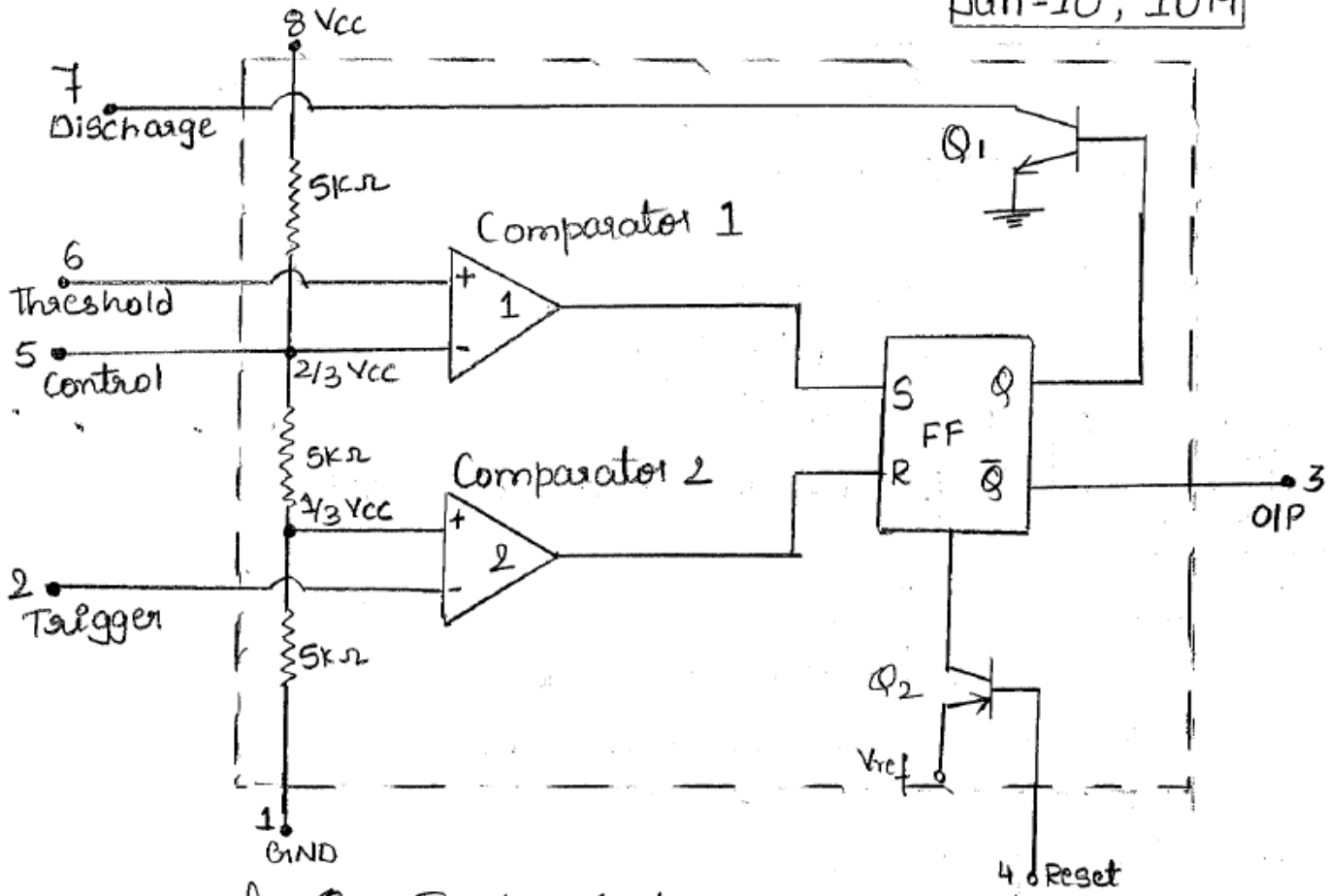

fig ①: Functional diagram of 555 timer.

fig ① Shows the functional diagram for 555 IC timer. It Consists of two op-amp voltage Comparators, resistive voltage divider network, SR Flip-Flop and a discharging transistor.

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Pin 1 : Ground :-

All the voltages are measured with respect to this terminal.

Pin 2 : Trigger :-

Due to voltage divider network, the voltage of Non-INV terminal of Comparator 2 is fixed at $V_{cc}/3$. The INV I/P of Comparator 2 which is compared with $V_{cc}/3$. When the trigger I/P is slightly less than $V_{cc}/3$ the Comparator 2 O/P goes high. This O/P is given to reset I/P of R-S flipflop. Thus $Q=0$ & $\bar{Q}=1$. [$\bar{Q}$ is connected to O/P] ∴ O/P of the timer is high.

Pin 3 : Output :-

* The $\bar{Q}$ of the flip-flop goes to pin 3 which is the O/P. The load can be connected in two ways:
i] Between Pin 3 and ground is called Normally-off load.
ii] Between Pin 3 and Vcc is called Normally-ON load.

Pin 4 : RESET :-

The 555 timer can be reset by applying a negative pulse to this pin. This pin is connected to Vcc to avoid false triggering when the timer is not in use.

Pin 5 : Control Voltage :-

An external voltage applied to this terminal changes the threshold as well as the triggering voltage [$2/3 V_{cc}$]

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By applying a voltage on this pin, the pulse width [duty cycle] of the o/p waveform can be varied.

Pin 6 : Threshold :-

This is a Non-INV I/p of Comparator 1. The voltage at this pin compare with the $\frac{2}{3}$ Vcc at the INV terminal of Comparator 1.

When the voltage at this pin is greater than threshold voltage 2/3 Vcc, the o/p of the Comparator 1 goes high, The flip-flop then resets switching the o/p to the timer to become low.

Pin 7 : Discharge :-

This pin is connected to the collector of the discharge transistor Q_1.

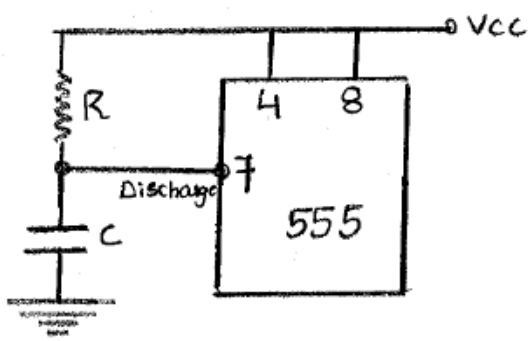
When the o/p is high [i.e. $\bar{Q}=1$ & $Q=0$], transistor Q_1 is OFF and acts as open ckt to the external capacitor.

Illy, When the o/p is low [i.e $\bar{Q}=0$ & $Q=1$], Q_1 is ON & acts as a short ckt, shorting out the external capacitor 'C' to ground.

Pin 8 : +Vcc :-

The IC 555 timer can work with an supply voltage between +15V to +18V.

Note :



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Monostable Multivibrator using IC-555 :

Jan-09, 5m

* 555 timer as monostable

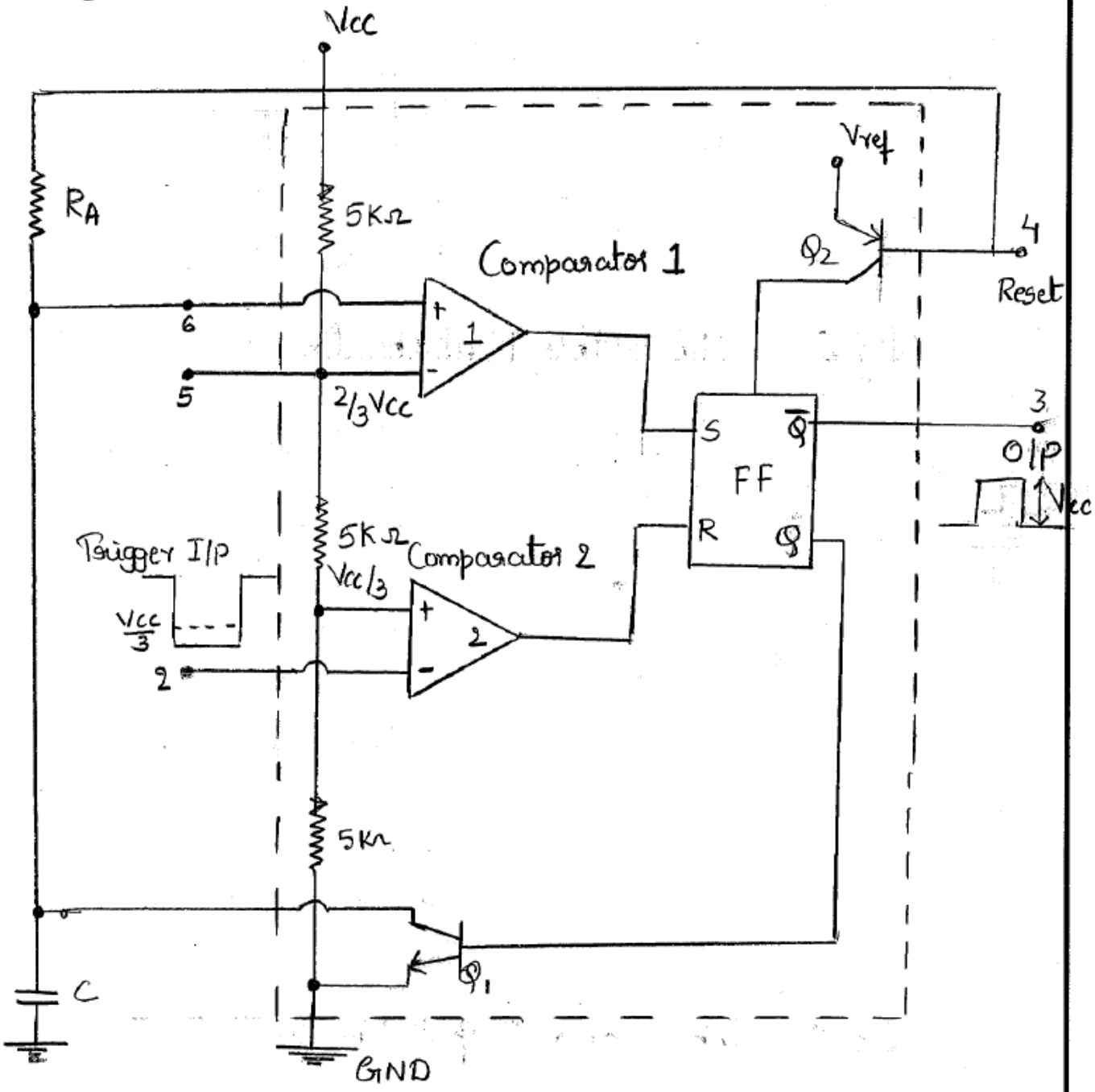

fig ①: 555 timer in Monostable operation with functional diagram.

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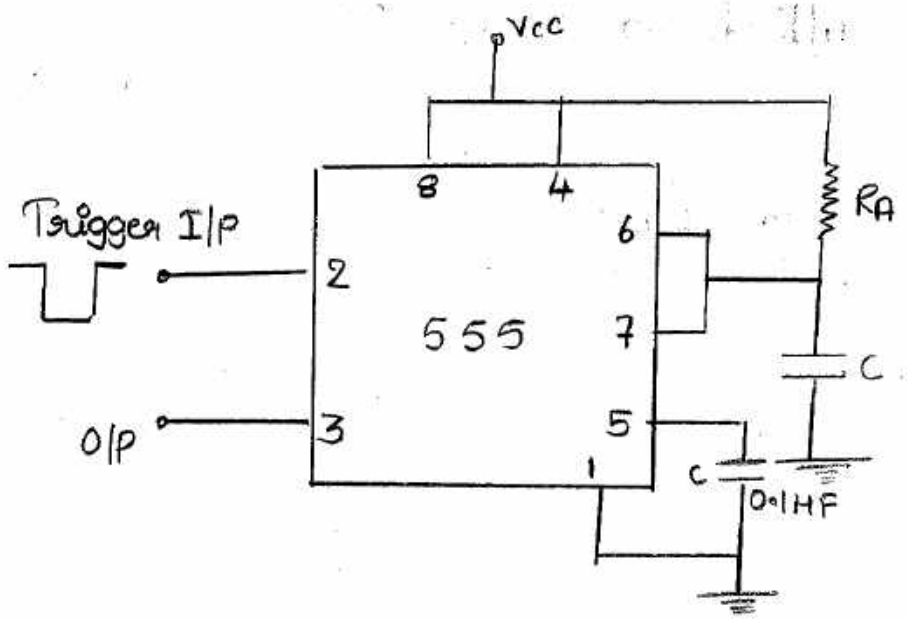

fig ② : Monostable Multivibrator.

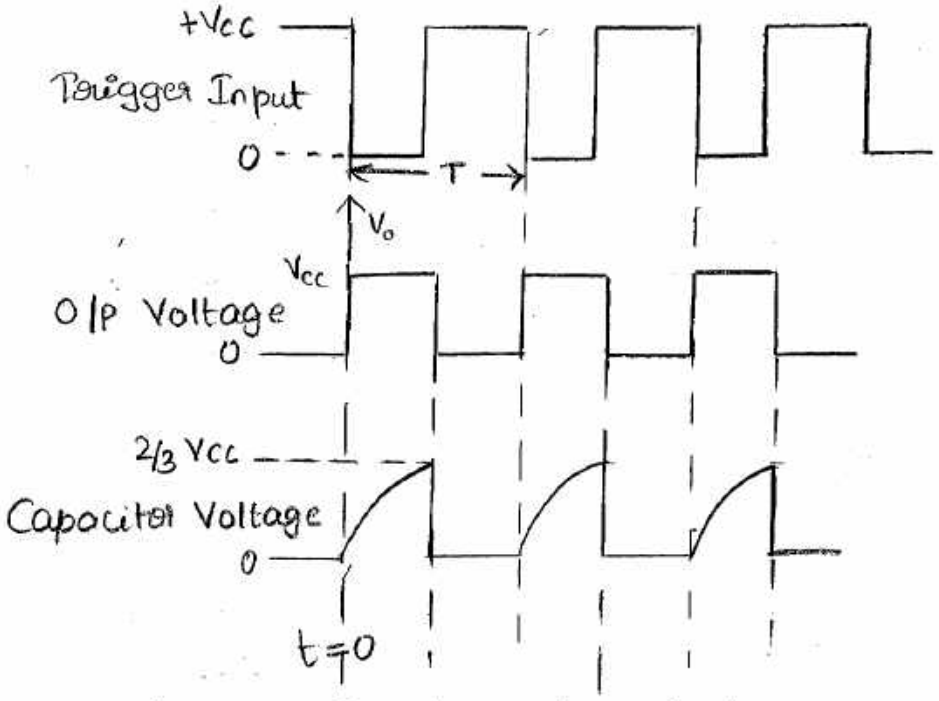

fig ③ : Input and Output Waveforms.

* Assume that the O/P of the 555 timer is initially low i.e. the circuit is in a stable state, transistor Q_1 is ON and Capacitor 'C' is shorted to ground.

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By the application of -ve trigger pulse to pin-2, transistor Q_1 is Turn-OFF, which releases the short ckt across the capacitor 'C' & drives the o/p to high. [i.e. $Q=0$ & $\bar{Q}=1$].

Now the capacitor 'C' starts charging towards Vcc through R_A. When the voltage across the capacitor 'C' equals 2/3 Vcc, the comparator 1 o/p goes to high, which intern drives [to] the o/p to low state [i.e $Q=1$ & $\bar{Q}=0$].

* Now transistor Q_1 is ON [$\because Q=1$] & hence capacitor 'C' discharges through the transistor Q_1.

The o/p of the monostable multivibrator remains low until a trigger pulse is again applied. Then the cycle repeats.

So a rectangular wave is produced at the o/p. The pulse width of this rectangular pulse is controlled by the charging time of capacitor & Resistor.

Thus R_AC Controls the pulse width.

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Derivation of Pulse width:-

The voltage across capacitor increases exponentially and is given by:

$$\boxed{V_c = V_{cc}\left[1 - e^{-t/R_AC}\right]} \rightarrow (1)$$

at $t = T$, $V_c = \frac{2}{3} V_{cc}$

Now eq (1) becomes

$$\frac{2}{3} V_{cc} = V_{cc}\left[1 - e^{-T/R_AC}\right]$$

$$\frac{2}{3} = 1 - e^{-T/R_AC}$$

$$\frac{2}{3} - 1 = - e^{-T/R_AC}$$

$$\frac{2-3}{3} = - e^{-T/R_AC}$$

$$+\frac{1}{3} = + e^{-T/R_AC}$$

$$e^{-T/R_AC} = \frac{1}{3}$$

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$$e^{-T/R_AC} = \frac{1}{3}$$

$$-\frac{T}{R_AC} = \ln\left[\frac{1}{3}\right]$$

$$+\frac{T}{R_AC} = +1.0996$$

$$\boxed{T = 1.0996\, R_AC}$$

$$\therefore \boxed{T \simeq 1.1\, R_AC} \longrightarrow (2)$$

Eq (2) indicates that the O/p voltages waveform depends on the values of R_A & C and it is independent of Vcc.

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Problems :

1] Design a monostable multivibrator using 555 timer to obtain a pulse width of 10msec **Jan-10, 6M**

Soln Given, $T = 10\text{msec}$.

WKT, $T = 1.1 R_A C$

$$R_A C = \frac{T}{1.1}$$

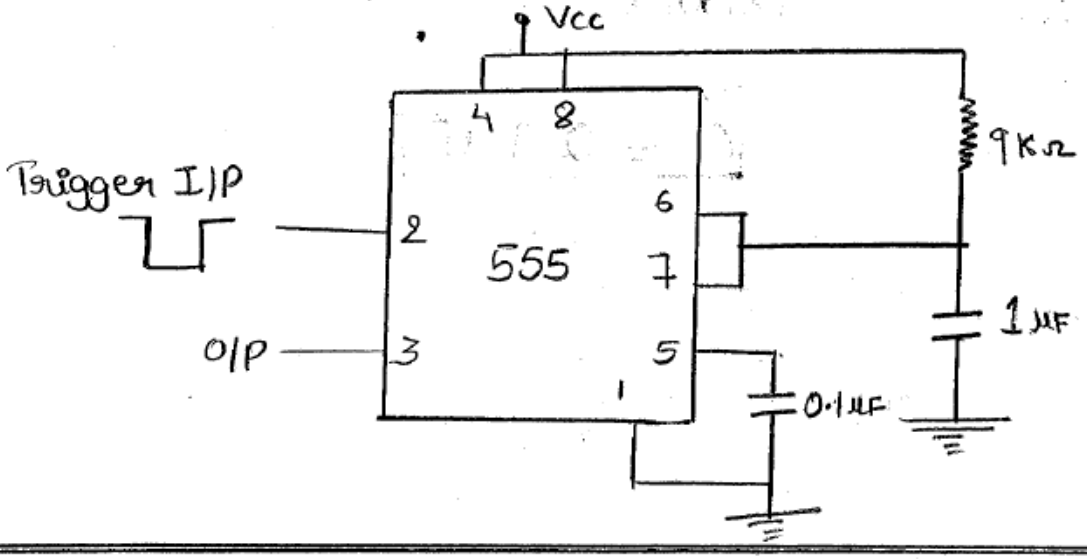
$$R_A C = \frac{10\text{msec}}{1.1}$$

$$R_A C = 9.09\text{msec} \leftarrow 1M$$

Assume $C = 1\mu F$ ← 1M

$$R_A = \frac{9.09\text{msec}}{1\mu F} = 9.09\text{K}\Omega$$

$\therefore$ $R_A = 9.9\text{K}\Omega$ ← 2M



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2] In the monostable multivibrator, the component values are $R_A = 5.6k\Omega$, $C = 0.068\mu F$. Find the pulse width T.

Sol: WKT, $T = 1.1 R_A C$

$= 1.1 \times 5.6k\Omega \times 0.068\mu F$

$\boxed{T = 0.42msec}$

3] In the monostable multivibrator, $R = 100k\Omega$ & the time delay $T = 100msec$. Calculate the value of C. Verify the value of C obtained.

Sol: WKT,

$T = 1.1 R_A C$

$T = 1.1 \times 100k\Omega \times C$

$\frac{100mSec}{1.1 \times 100k\Omega} = C$

$\boxed{C = 0.9\mu F}$

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Astable Multivibrator :-

* 555 timer as astable multivibrator.

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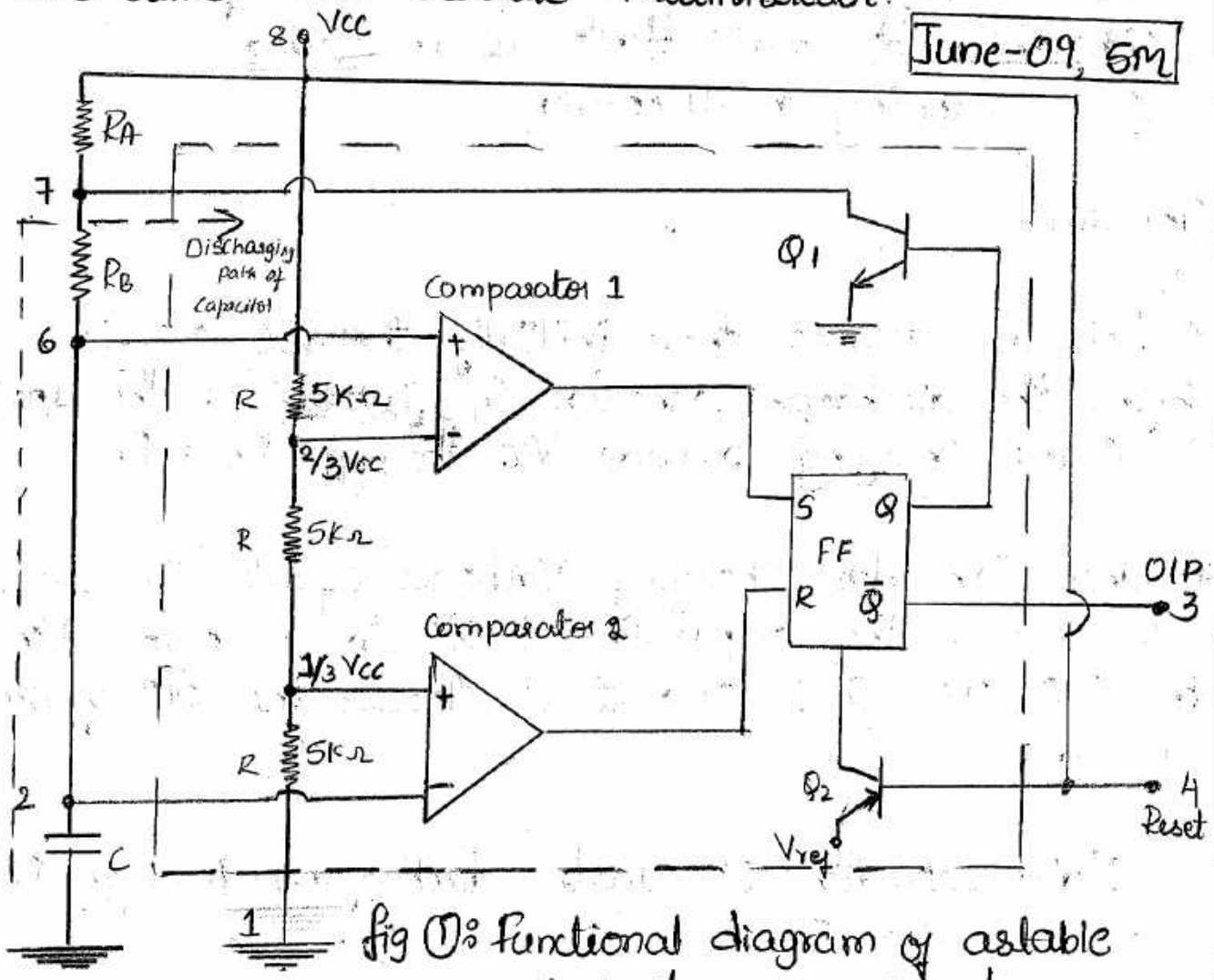

fig ①: Functional diagram of astable multivibrator using 555 timer.

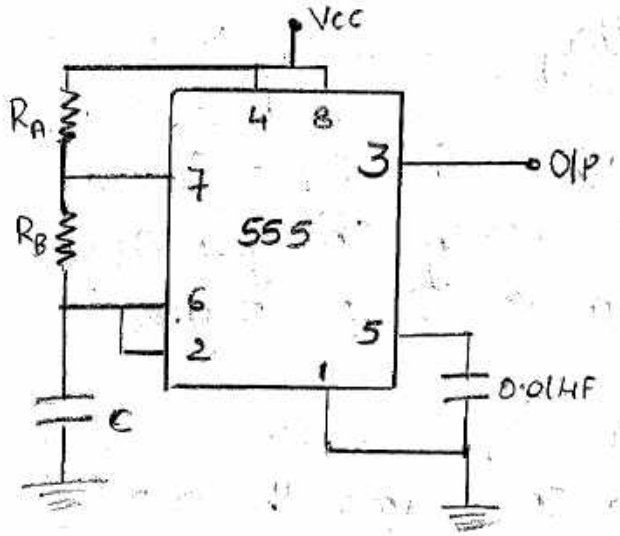

fig ② (a) : Astable Multivibrator Using 555 timer

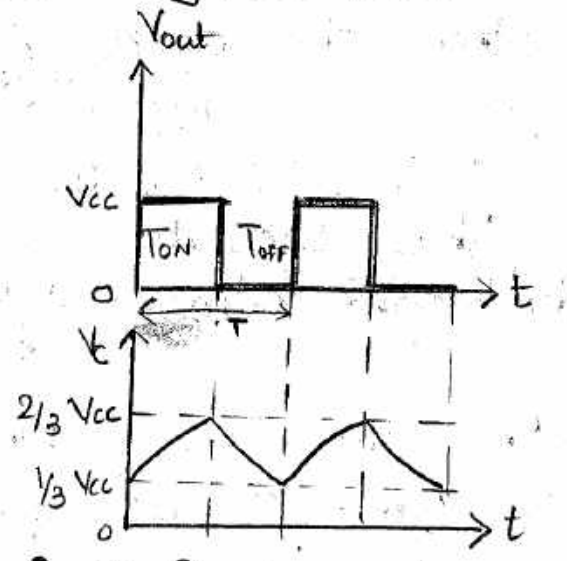

fig ② (b) O/P waveforms.

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* An Astable multivibrator is a rectangular wave generating circuit. This ckt does not require an external trigger to change the state of the o/p [either high or low]. Hence it is called free running multivibrator.

Operation :

* Let us assume that initially the 555 o/p is high, the discharge transistor Q_1 is OFF & the capacitor 'C' starts charging towards Vcc through R_A & R_B.

* When capacitor charging voltages equals to $\frac{2}{3}$ Vcc, it causes the comparator 1 o/p to go high. Hence the F/F o/p $Q=1$ and $\bar{Q}=0$. Thus, the o/p of timer is low.

Now capacitor 'C' starts discharging through R_B and transistor Q_1.

* When the discharging voltage across the capacitor 'C' equals $\frac{Vcc}{3}$, Comparator 2 o/p goes to high and hence it resets the F/F. Then the cycle repeat.

Thus capacitor is periodically charged and discharged between $\frac{2Vcc}{3}$ to $\frac{Vcc}{3}$ respectively.

* The time during which the capacitor charges from $\frac{Vcc}{3}$ to $\frac{2Vcc}{3}$ is equal to the time the o/p is high.

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IIIly The time during which the capacitor discharges from $\frac{2V_{cc}}{3}$ to $\frac{V_{cc}}{3}$ is equal to the time the o/p is high.

* The charging time for the capacitor is given by

$$T_C = 0.693 [R_A + R_B] C$$

* The discharging time for the capacitor is given by

$$T_d = 0.693 R_B C$$

* The time fore one cycle is

$$T = T_C + T_d = 0.693 [R_A + R_B] C + 0.693 R_B C$$

$$T = 0.693 R_A C + 0.693 R_B C + 0.693 R_B C$$

$$T = 0.693 [R_A + 2R_B] C$$

* Duty cycle $\%D = \frac{T_C}{T} \times 100$

$$\%D = \frac{0.693 [R_A + R_B] C}{0.693 [R_A + 2R_B] C} \times 100$$

$$\%D = \frac{(R_A + R_B)}{(R_A + 2R_B)} \times 100$$

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* Frequency of oscillation is given by,

$$f = \frac{1}{T}$$

$$f = \frac{1}{T} = \frac{1}{0.693[R_A + 2R_B]\,C}$$

$$f = \frac{1}{0.693} \times \frac{1}{C(R_A + 2R_B)}$$

$$f = \frac{1.44}{C[R_A + 2R_B]}$$

$$\therefore \boxed{f = \frac{1.44}{[R_A + 2R_B]C} \; Hz}$$

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* Derive an expression for Charging and discharging time for Astable Multivibrator. [T_C or T_{ON} & T_d or T_{OFF}]

→ The expression for capacitor charging is given by

$$V_C = V_{CC}\left[1 - e^{-t/RC}\right] \longrightarrow (1)$$

Eq (1) is valid only if the initial voltage on the capacitor is zero.

→ If there is a some initial voltage present then the charging equation gets modified as follows:

$$V_C = V_F + (V_i - V_F)\, e^{-t/RC} \longrightarrow (2)$$

where, V_F → Final Voltage
V_i → Initial Voltage

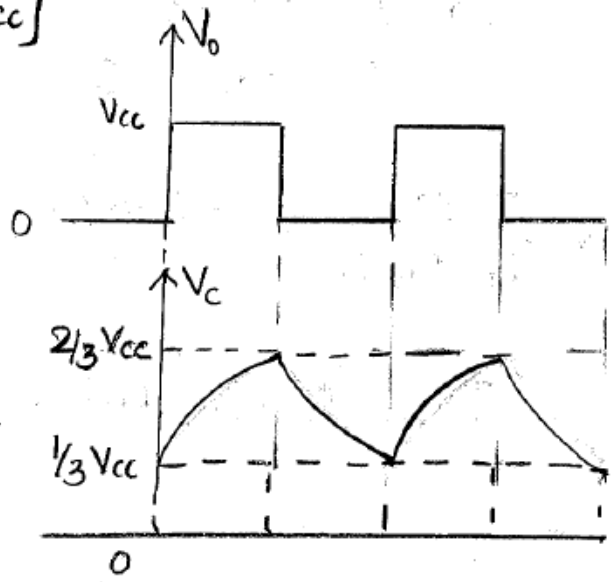
T_{ON} or T_C :- $\left[V_C = \frac{2}{3} V_{CC}\right]$

During charging period,

At, $t = T_C$,

$V_i = \frac{V_{CC}}{3}$, $V_F = V_{CC}$,

$R = R_A + R_B$



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Now Eq ② becomes,

$$\frac{2}{3}V_{cc} = V_{cc} + \left[\frac{V_{cc}}{3} - V_{cc}\right] e^{-T_c/(R_A+R_B)C}$$

$$\frac{2}{3}V_{cc} - V_{cc} = \left[\frac{V_{cc} - 3V_{cc}}{3}\right] e^{-T_c/(R_A+R_B)C}$$

$$\frac{2V_{cc} - 3V_{cc}}{3} = \left[-\frac{2V_{cc}}{3}\right] e^{-T_c/(R_A+R_B)C}$$

$$+\frac{V_{cc}}{3} = +\frac{2V_{cc}}{3} e^{-T_c/(R_A+R_B)C}$$

$$\frac{1}{2} = e^{-T_c/(R_A+R_B)C}$$

$$0.5 = e^{-T_c/(R_A+R_B)C}$$

$$\ln(0.5) = \frac{-T_c}{(R_A+R_B)C}$$

$$\frac{+T_c}{(R_A+R_B)C} = +0.693$$

$$\boxed{T_c = 0.693[R_A+R_B]C}$$

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T_{OFF} or T_d :

The capacitor discharges from $\frac{2V_{CC}}{3}$ to $\frac{V_{CC}}{3}$

$\therefore$ At $t = T_d$, $V_i = \frac{2V_{CC}}{3}$, $V_F = 0$, $R = R_B$

Now eq ② becomes,

$$\frac{V_{CC}}{3} = 0 + \left[\frac{2V_{CC}}{3} - 0\right] e^{-T_d/R_BC}$$

$$\frac{V_{CC}}{3} = \frac{2V_{CC}}{3} e^{-T_d/R_BC}$$

$$\frac{1}{2} = e^{-T_d/R_BC}$$

$$e^{-T_d/R_BC} = 0.5$$

$$-\frac{T_d}{R_BC} = \ln(0.5)$$

$$+\frac{T_d}{R_BC} = +0.693$$

$$\boxed{T_d = 0.693 R_BC}$$

→ Total time period is given by

$$T = T_C + T_d$$

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$$T = 0.693[R_A + R_B]C + 0.693 R_B C$$

$$\therefore \boxed{T = 0.693[R_A + 2R_B]C}$$

* The frequency of oscillation is given by

$$f = \frac{1}{T} = \frac{1}{0.693[R_A + 2R_B]C}$$

$$\boxed{f = \frac{1.44}{[R_A + 2R_B]C} \; Hz}$$

→ Duty Cycle :

$$\%D = \frac{T_c}{T} \times 100$$

$$= \frac{0.693[R_A + R_B]\cancel{C}}{0.693[R_A + 2R_B]\cancel{C}} \times 100$$

$$\boxed{\%D = \frac{[R_A + R_B]}{[R_A + 2R_B]} \times 100}$$

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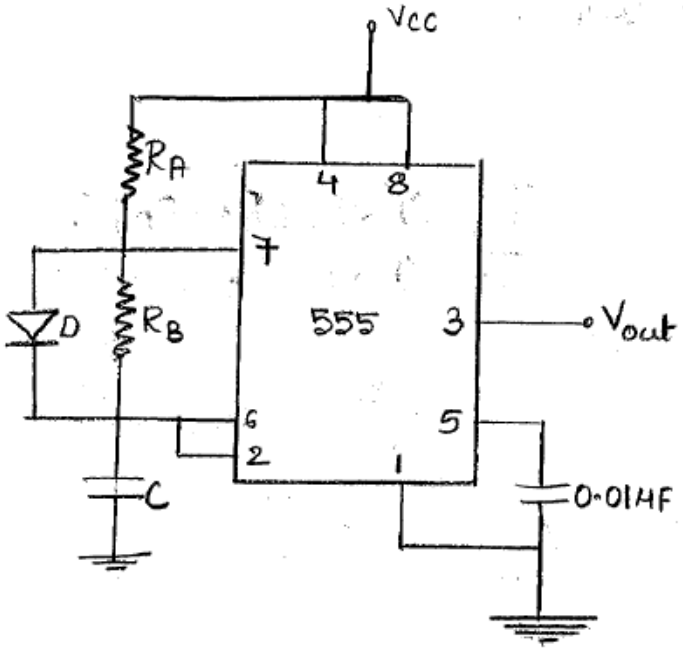
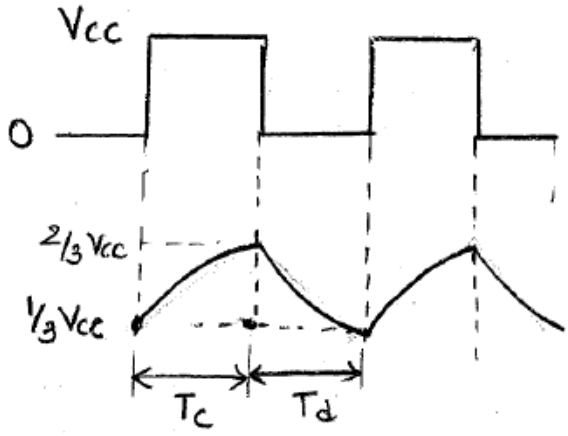
Astable Multivibrator to generate Square wave.

[Duty Cycle = 50·1·]



Fig①: Square wave generator



Fig②: Square wave.

* To get exactly 50·1· duty cycle i·e Square wave o/p it is necessary to modify the astable timer ckt.

In modified astable ckt, the capacitor 'C' charges through R_A and diode D & discharges through R_B.

∴ $T_C = 0.693 R_A C$ & $T_d = 0.693 R_B C$

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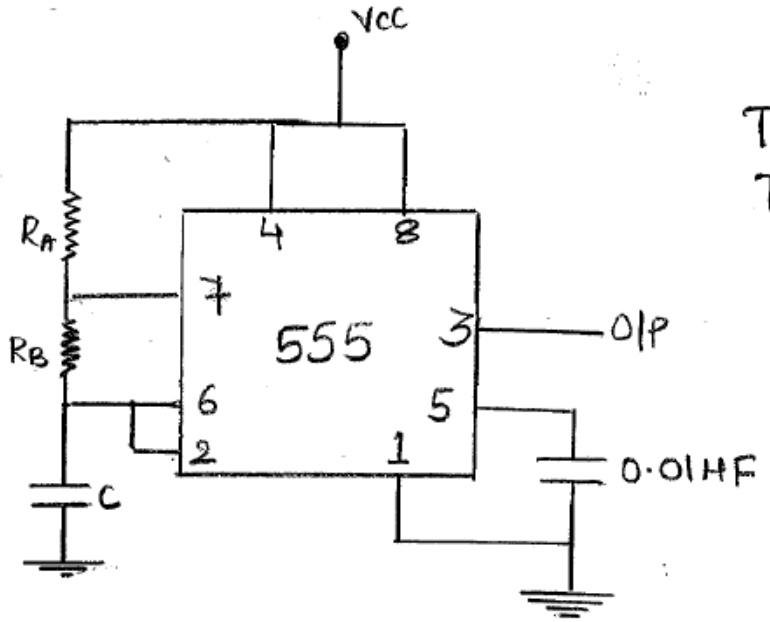
NOTE:

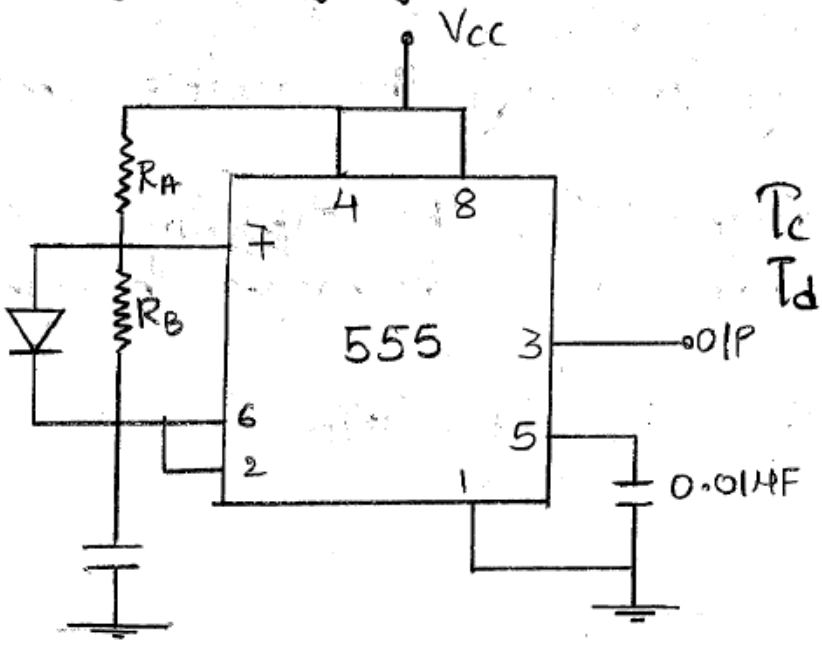
1] To get Duty Cycle 'D' > 50·1·



$T_c = 0.693 [R_A + R_B] C$

$T_d = 0.693 R_B C$

2] To get Duty Cycle 'D' ≤ 50·1·



$T_c = 0.693 R_A C$

$T_d = 0.693 R_B C$

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Problems :

1] For the astable multivibrator, $R_A = 4.7K\Omega$, $R_B = 1K\Omega$ and $C = 1\mu F$. Determine

i] The positive pulse width 'T_c'
ii] The negative pulse width 'T_d'
iii] Free - running frequency 'f'
iv] Duty Cycle

Sol:

i] $T_c = 0.693\,[R_A + R_B]\,C$

$= 0.693\,[4.7K + 1k] \times 1\mu$

$\boxed{T_c = 3.933 m sec}$

ii] $T_d = 0.693\, R_B\, C$

$= 0.693 \times 1K \times 1 \times 10^{-6}$

$\boxed{T_d = 0.69 m sec}$

iii] $f = \frac{1}{T}$

$T = T_c + T_d = 3.933\,m + 0.69m = 4.623 m sec$

$f = \frac{1}{4.62 m sec}$

$\boxed{f = 216.31\ Hz}$

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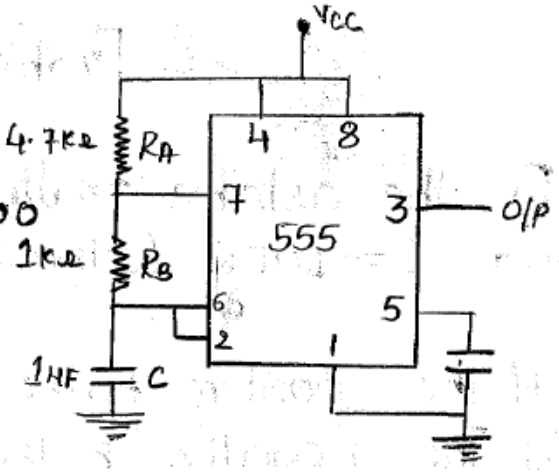
iv] Duty cycle $= \frac{T_c}{T} \times 100 \cdot 1\cdot$

$= \frac{3.983 \times 10^{-3}}{4.623 \times 10^{-3}} \times 100$

Duty Cycle = 85.07 1·



2] Design an Astable multivibrator using 555 Timer to generate an O/P waveform of 2KHz with a duty cycle of 50·1·

Sol⁹ Given,

$D = 50 \cdot 1\cdot$, $f = 2Hz \times 10^{+3} = 2KHz$

$T = \frac{1}{f} = \frac{1}{2KHz}$

T = 0.5 msec

WKT, In 50·1· duty cycle $T_{ON} = T_{OFF}$ i.e. $T_c = T_d$

* $T_c = 0.693 R_A C$

Assuming **C = 0.01 HF**

$R_A = \frac{T_c}{0.693 C} = \frac{0.5 msec}{0.693 \times 0.01 \times HF}$

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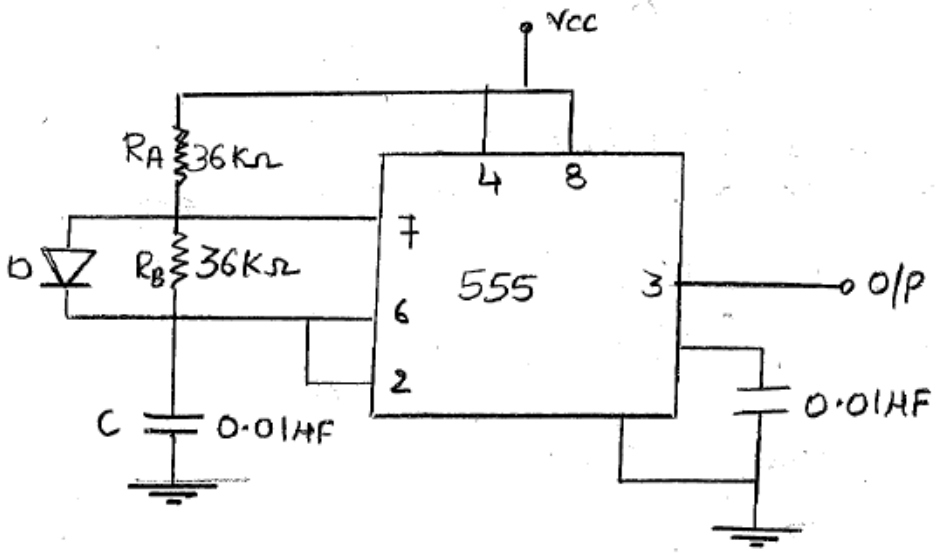
$R_A = 36.07K\Omega$

$\therefore R_A = R_B = 36.07K\Omega$



3] Design a 555 astable multivibrator to operate at 5kHz with a duty cycle of 40%.

Sol⇒ $f = 5kHz$,

$D = 0.4$

$$T = \frac{1}{f} = \frac{1}{5kHz} = 0.2msec$$

$$D = \frac{T_C}{T}$$

$$T_C = D \times T$$

$$T_C = 0.4 \times 2msec$$

$$\boxed{T_C = 0.08msec}$$

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WKT, $T = T_C + T_d$

$$T_d = T - T_C = 0.2\,msec - 0.08\,msec$$

$$\boxed{T_d = 0.12\,msec}$$

WKT, $T_C = 0.693 R_A C$

$$R_A = \frac{T_C}{0.693\,C}$$

Assume $\boxed{C = 0.01\mu F}$

$$R_A = \frac{0.08 \times 10^{-3}}{0.693 \times 0.01\mu F}$$

$$\boxed{R_A = 11.54\,K\Omega}$$

WKT, $T_d = 0.693\, R_B C$

$$R_B = \frac{T_d}{0.693\,C}$$

$$= \frac{0.12 \times 10^{-3}}{0.693 \times 0.01 \times 10^{-6}}$$

$$\boxed{R_B = 17.31\,K\Omega}$$

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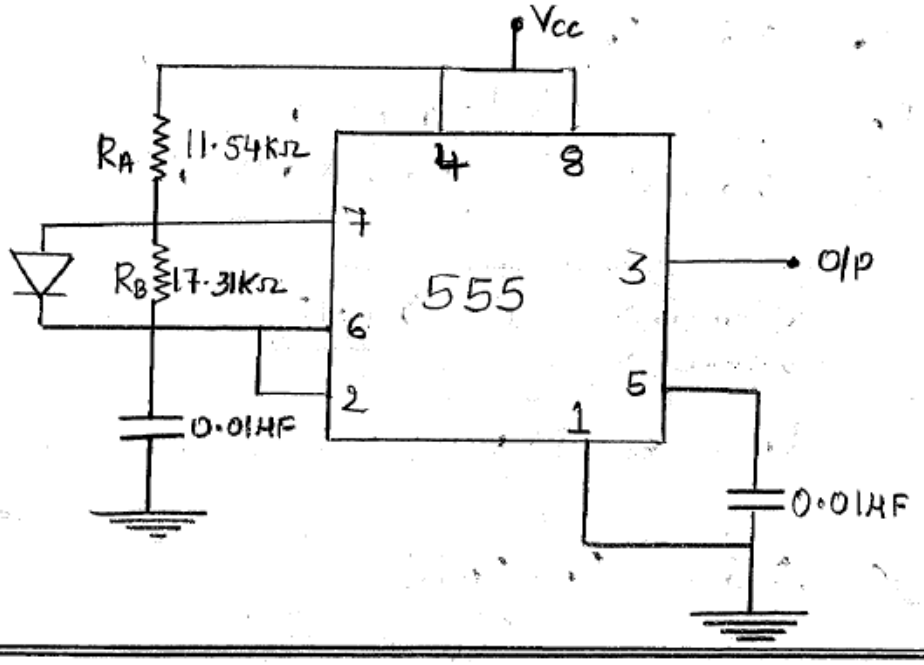

4] Design a 555 astable multivibrator for an o/p frequency of 1KHz & duty cycle 60%.

Sol:

$f = 1KHz$, $D = 0.6$

* $T = \frac{1}{f} = \frac{1}{1KHz} = 1msec$

* $D = \frac{T_c}{T}$

$0.6 = \frac{T_c}{1msec}$

$$\boxed{T_c = 0.6 \times 1msec = 0.6msec}$$

* WKT, $T = T_c + T_d$

$T_d = T - T_c = 1msec - 0.6msec$

$$\boxed{T_d = 0.4msec}$$

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* WKT, $T_d = 0.693 R_B C$

$$R_B = \frac{T_d}{0.693 C} = \frac{0.4 \times 10^{-3}}{0.693 \times 0.1 \times 10^{-6}}$$

Assuming $\boxed{C = 0.1\,\mu F}$

$$\boxed{R_B = 5.77\,K\Omega}$$

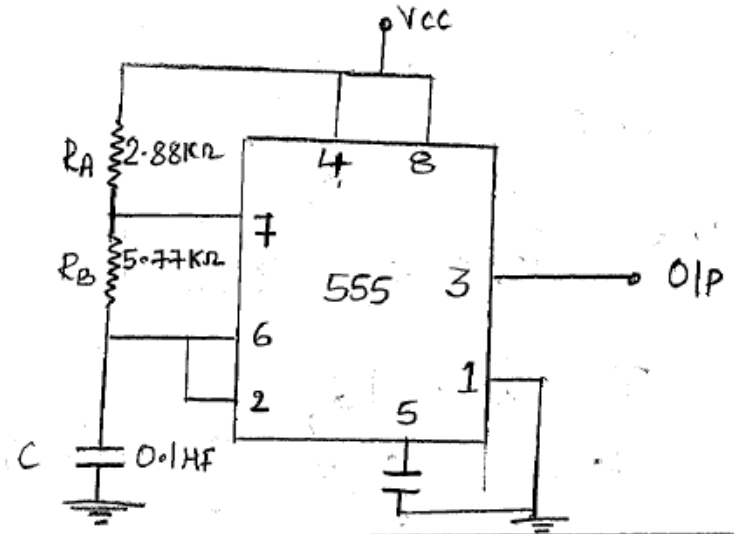
* WKT, $T_C = 0.693 [R_A + R_B] C$

$$R_A + R_B = \frac{T_C}{0.693 C}$$

$$R_A = \frac{T_C}{0.693 C} - R_B$$

$$R_A = \frac{0.6 \times 10^{-3}}{0.693 \times 0.1 \times 10^{-6}} - 5.77 \times 10^3$$

$$\boxed{R_A = 2.88\,K\Omega}$$



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5] A 555 Stable multivibrator has $R_A = 2.2K\Omega$ and $R_B = 6.8K\Omega$ and $C = 0.01\mu F$
Calculate, i] t_{high} ii] t_{low} iii] free-running frequency and iv] Duty Cycle.
Draw the Connection diagram. **June-08, 7M**

Sol:→

i] t_{high}

$$T_C = 0.693[R_A + R_B]\,C = 0.693\,[2.2K\Omega + 6.8K\Omega]\,0.01\mu F$$

$$\boxed{T_C = 0.062\,msec} \leftarrow (1m)$$

ii] t_{low}

$$T_d = 0.693\,R_B C = 0.693 \times 6.8K\Omega \times 0.01\mu F$$

$$\boxed{T_d = 0.047\,msec} \leftarrow (1m)$$

iii] free-running frequency

$$T = T_C + T_d = 0.062 \times 10^{-3} + 0.047 \times 10^{-3}$$

$$\boxed{T = 0.109\,msec}$$

$$f = \frac{1}{T} = \frac{1}{0.109m} = 9.14KHz$$

$$\boxed{f = 9.14KHz} \leftarrow (2M)$$

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(01)

$$f = \frac{1.14}{(R_A + 2R_B)C} = \frac{1.14}{(2.2k + 2\times 6.8K)\times 0.01\mu F}$$

$$\boxed{f = 9.14 kHz}$$ ← (2M)

iv] Duty cycle

$$D = \frac{T_C}{T}$$ (01) $$D = \frac{R_A + R_B}{R_A + 2R_B} \times 100$$

$$= \frac{0.062 msec}{0.109 msec}$$

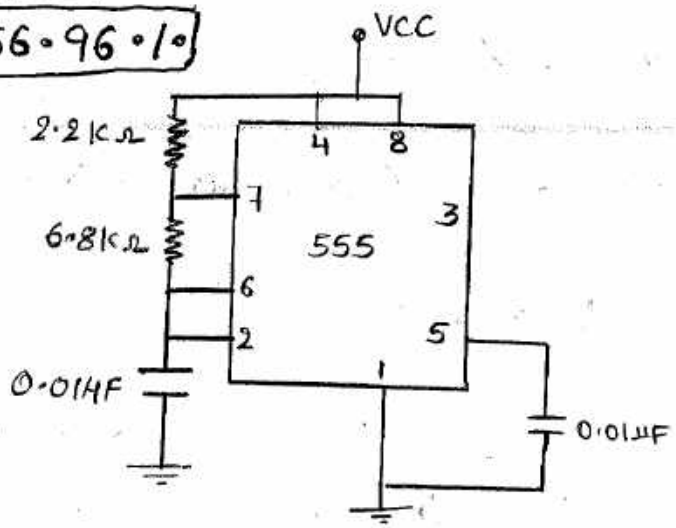
$$D = \frac{(2.2K + 6.8K)}{(2.2K + 2\times 6.8K)} \times 100$$

$$D = 0.56$$

$$\boxed{\%D = 56.1\%}$$

$$\boxed{\%D = 56.1\%}$$ ← (2M)

$$\boxed{\%D = 56.96\%}$$



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Schmitt Trigger :

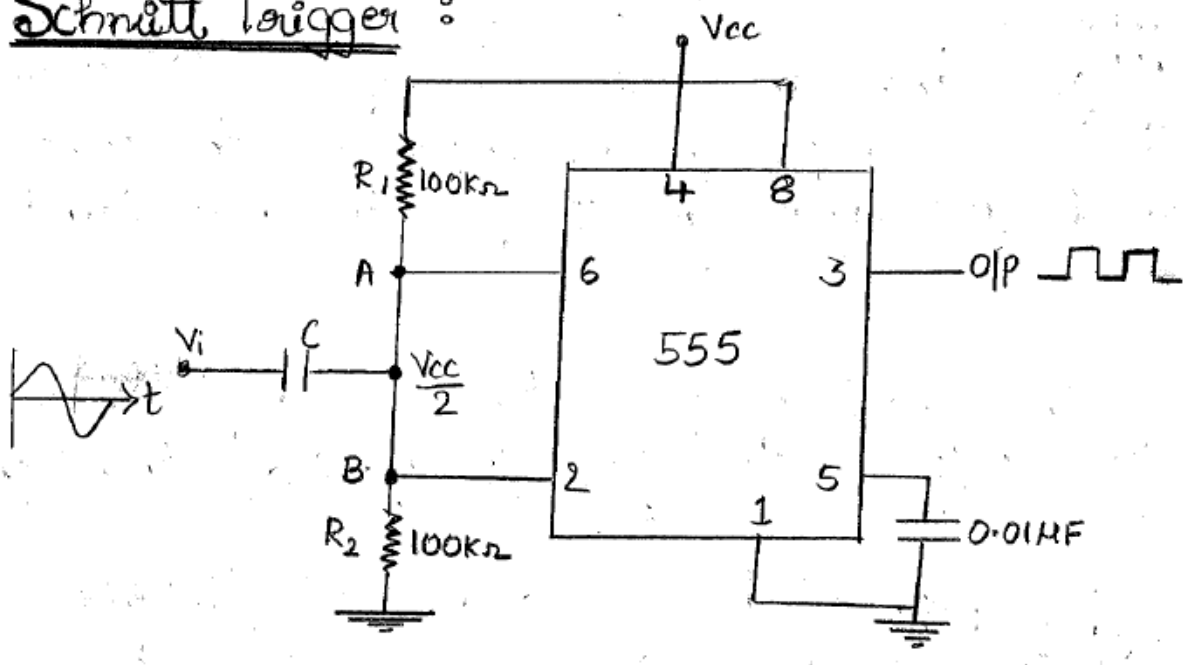

Fig ① : 555 timer Connected as Schmitt trigger Ckt

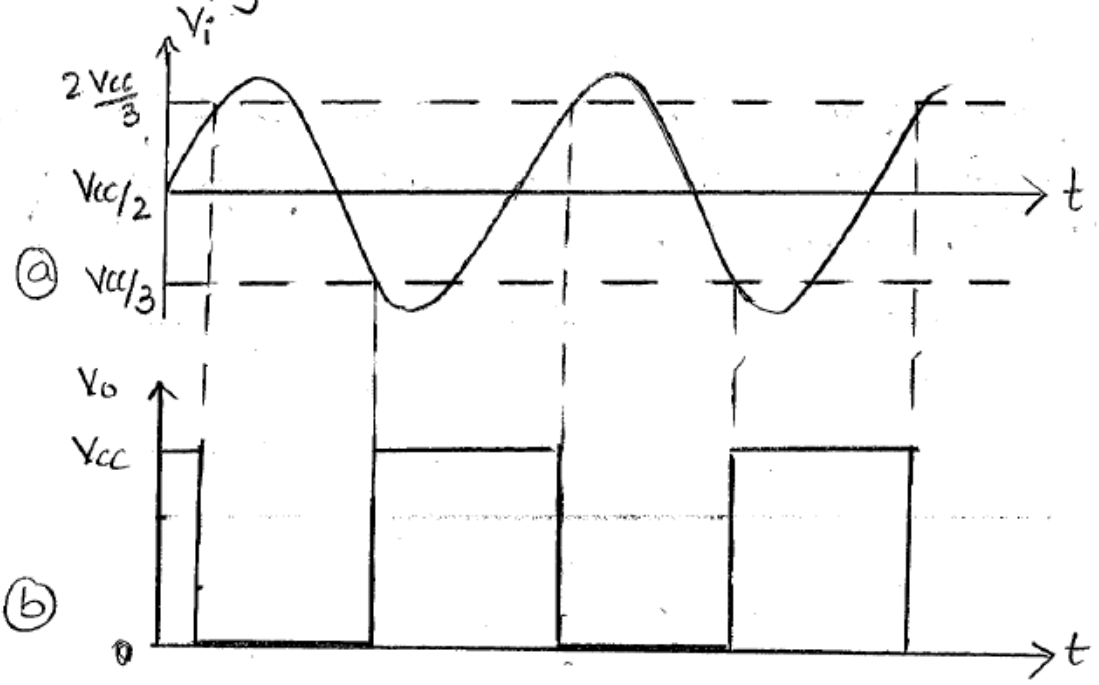

Fig ② : ⓐ Input Voltage Waveform, ⓑ Output Voltage Waveform.

Fig ① shows a schmitt trigger circuit using a 555 timer. Here the two internal comparators are tied together [Pin 2 & 6] and externally biased at Vcc/2 through R_1 and R_2.

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* The upper comparator will Set when the voltage at point A goes above the bias value of $\frac{Vcc}{2}$ to $\frac{2}{3}Vcc$. and the lower comparator will Set when the voltage at point B goes down to $\frac{Vcc}{3}$ from the bias value of $\frac{Vcc}{2}$.

* If a Sine wave of ~~peak to peak~~ amplitude greater than $\frac{Vcc}{6}$ $\left[\because \frac{Vcc}{6} = \frac{2Vcc}{3} - \frac{Vcc}{2}\right]$ is applied, then the internal flip-flop will be Set and reset alternately thus producing a Square wave at the o/p pin 3.

* The frequency of the Square wave obtained from the Schmitt trigger is same as the frequency of the I/p Sinusoidal Signal.

i.e. I/p Signal Frequency = o/p Signal Frequency.

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Phase Locked Loop [PLL] :

* Phase locked loop as automatic frequency controller.

Jan-09, 5M

* Write Explanatory note on PLL

Jan-10, 5M

* With the block diagram, explain the operation of phase locked loop:

Jan-09, 6M [CBE]

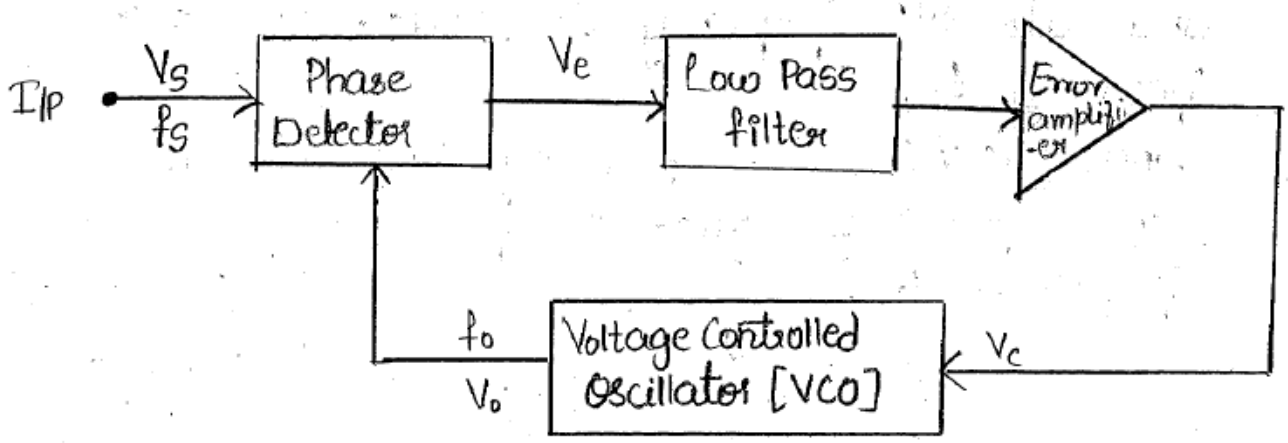

fig ①: Block diagram of PLL

Fig ① shows the block diagram of PLL.

PLL is a feedback System Consists of:

1] Phase detector
2] Low-Pass filter
3] Error amplifier
4] Voltage Controlled Oscillator [VCO].

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* The VCO is a free running multivibrator which operates at a frequency 'f_o' [determined by an external timing resistor an a external capacitor] called <u>free running frequency</u>.

*

* A VCO is an oscillator ckt in which the O/P frequency 'f_o' can be controlled by an externally applied voltage. The VCO provides the linear relationship between the applied voltage and the oscillator frequency. The applied voltage is called <u>Control Voltage 'V_c'</u>.

{ When $V_c = 0$, VCO is in free-running mode and its O/P frequency is called as Center frequency 'f_o'.
When $V_c \neq 0$, VCO frequency will shift to some other frequency called 'f' from a free running frequency 'f_o'. }

* Let an input signal of amplitude 'V_s' & frequency 'f_s' be applied to the PLL. The phase detector compares the phase and frequency of the incoming signal to that of the O/P 'V_o' of the VCO.

* If there is a difference in either the frequency or in phase or in both, then phase detector generates an error voltage V_e.
The phase detector produces the sum $[f_s + f_o]$ and differences $[f_s - f_o]$ components at its O/P. The high

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frequency Component (fs+fo) is removed by the loco pass filter and the difference frequency Component is amplified and then applied as Control Voltage 'V_c' at VCO.

* The Signal Vc shifts the VCO frequency in a direction to reduce the frequency difference between fs & fo. As Soon as this happens, then PLL is said to be in Capture range.

* The VCO Continues to change frequency till its OIP frequency becomes equal to the I/P Signal frequency The Ckt is said to be locked.

Once the PLL is locked, the OIP frequency of VCO i.e. fo is identical to fs except for a finite phase difference ϕ.

* After achieving locking, the PLL then tracks the frequency changes in the input Signal.

Thus, a PLL goes through three Stages:

i] free running ii] Capture and iii] Locked or tracking

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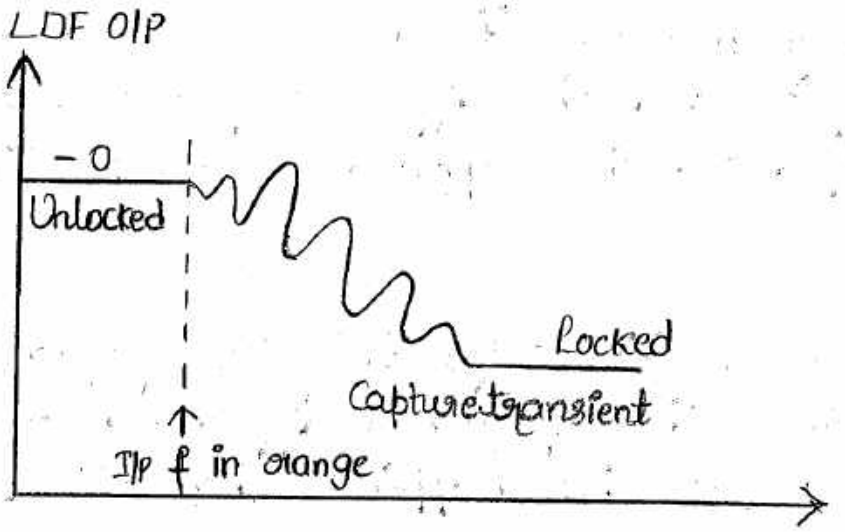

fig ② : The capture transient.

Figure ② shows the capture transient. As capture starts, a small sine wave appears. This is due to the frequency difference between the VCO and the I/P signal.

Each successive cycle causes the VCO frequency to more closer to the I/P signal frequency.

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Important definitions related to PLL :-

* Explain the following for a PLL

i] Lock-in range ii] Capture range
iii] Pull-in time

June-08, 6M

* Define lock-in range and capture range with reference to PLL.

Jan-11, 2M

i] Lock-in Range (or) Tracking range :-

The range of frequencies over which the PLL can maintain lock with the incoming signal is called the Lock-in range (or) Tracking range.

The lock range is usually expressed as a percentage of fo (VCO frequency).

ii] Capture range :-

The range of frequencies over which the PLL can acquire lock with an i/p signal is called the capture range.

Capture range is also expressed as a percentage of fo.

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iii] Pull-in time :-

The total time taken by the PLL to establish lock is called Pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

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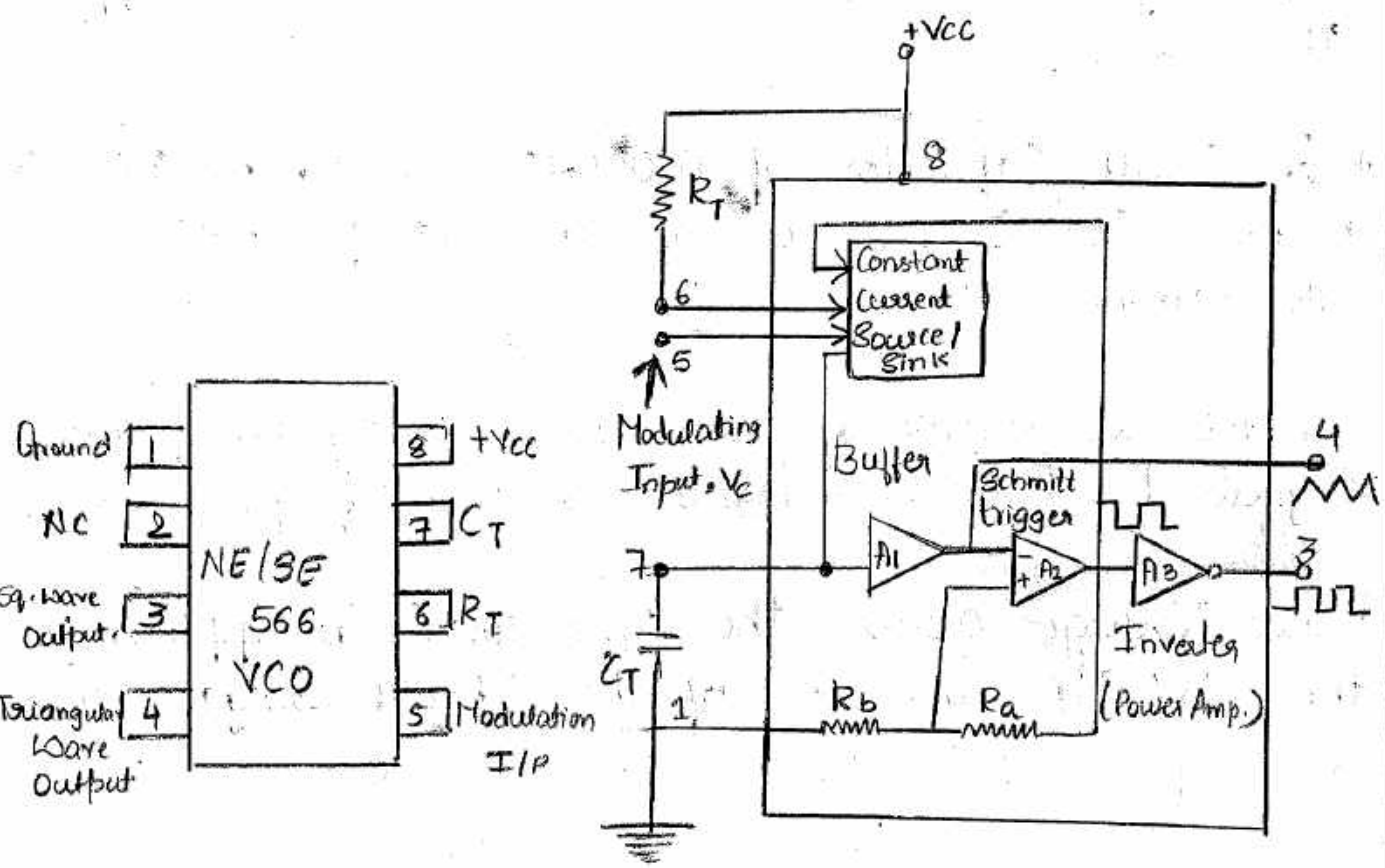
Voltage Controlled Oscillator [VCO] :-

* 566 Voltage Controlled Oscillator — June-09, 5M



(a) (b)

fig 1 : Voltage Controlled Oscillator.
a] Pin Configuration.
b] Block Diagram.

VCO is available in the IC form manufactured by Signetics with brand name NE/SE 566.

* In fig 1 (b), a timing capacitor C_T is linearly charged & discharged by a constant current Source/Sink.

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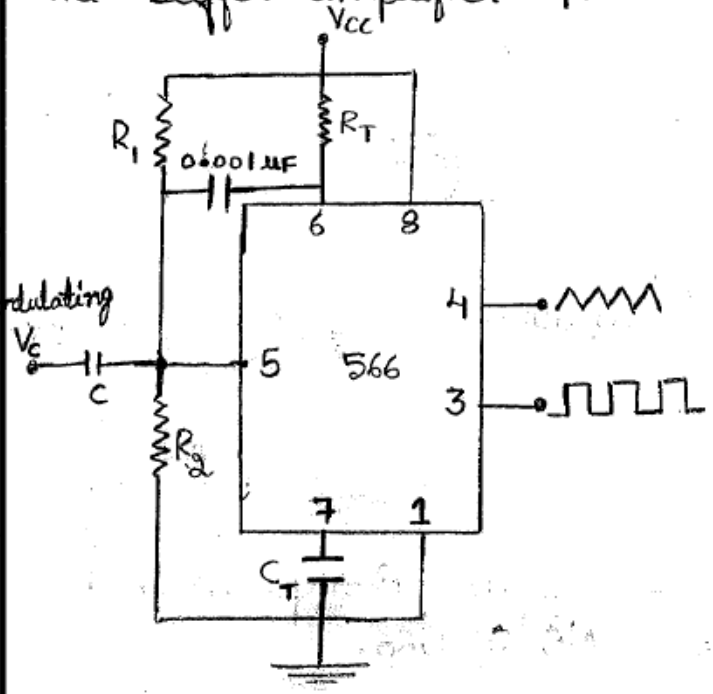
The amount of current can be controlled by changing the voltage Vc applied at the modulating input [Pin5] or by changing the timer resistor R_T external to IC chip. The voltage at Pin 6 is held at the same voltage as Pin 5.

* A small capacitor of 0.001 μF should be connected between Pin 5 and 6 to eliminate possible oscillations.

A VCO is commonly used in converting low frequency signals [such as EEGs] into an audio frequency range.

* The voltage across the capacitor C_T is applied to the INV I/P terminal of the Schmitt trigger A_2 via buffer amplifier A_1.



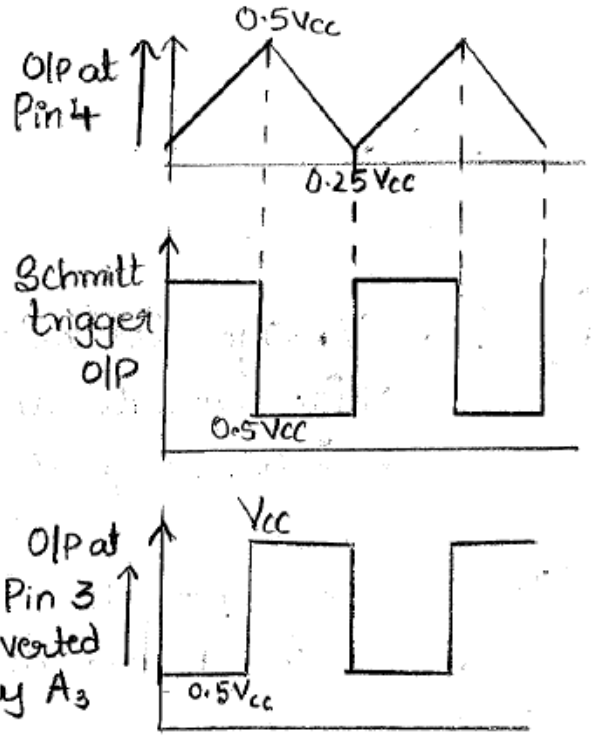


fig ②: ⓐ Typical connection diagram, ⓑ O/P waveform

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* The O/P Voltage Swing of the Schmitt trigger is designed to Vcc and 0.5Vcc. If Ra = Rb, the Voltages at the Non-INV terminal of A_2 Swings from 0.5Vcc to 0.25Vcc.

In fig 2(b), When the voltage on the capacitor C_T exceeds 0.5Vcc during Charging, the O/P of the Schmitt trigger goes LOW [i.e 0.5Vcc]. The capacitor now discharges and when it is at 0.25Vcc, the O/P of Schmitt trigger goes High (Vcc).

* The capacitor Charges and discharges for the same amount of time. This gives a triangular Voltage Waveform across C_T which is also available at Pin 4.

* The Square Wave O/P of the Schmitt trigger is Inverted by Inverter A_3 and is available at Pin 3.

* The O/P frequency of the VCO is given by:

$$f_o = \frac{2(V_{cc} - V_c)}{C_T R_T V_{cc}} \longrightarrow (1)$$

The O/P frequency of the VCO can be changed either by,

i] R_T ii] C_T iii] V_c.

* With no modulating input signal, if the Voltage at Pin 5 is biased at $\frac{2}{3}$ Vcc, Eq(1) gives the VCO

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O/P frequency as,

$$f_0 = \frac{2(V_{CC} - 7/8\, V_{CC})}{C_T R_T V_{CC}} = \frac{2\left(8V_{CC} - \frac{7V_{CC}}{8}\right)}{C_T R_T V_{CC}}$$

$$f_0 = \frac{2V_{CC}}{8 C_T R_T V_{CC}}$$

$$f_0 = \frac{1}{4 C_T R_T}$$

$$\boxed{f_0 = \frac{0.25}{R_T C_T}}$$

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Basic DAC Techniques :

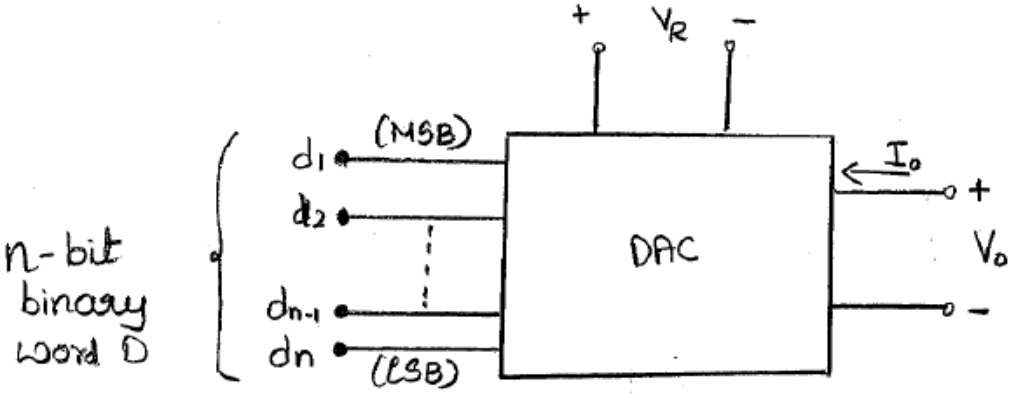

fig ① : Schematic of a DAC

* The input to the DAC is a n-bit binary word D whose digits are d_1, d_2, d_3, d_4 [i.e. $D = d_1, d_2 \cdots d_n$] and is combined with a reference voltage V_R to give an analog o/p signal.

The o/p of a DAC can be either a voltage (or) current. The analog o/p voltage is expressed as :

$$V_o = K V_{FS} (d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + - - - + d_n 2^{-n})$$

where, K = Scaling factor usually adjusted to unity
V_{FS} = full scale o/p voltage.
d_1 = Most significant bit [MSB] with a weight of $V_{FS}/2$
d_n = Least significant bit [LSB] with a weight of $V_{FS}/2^n$

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Weighted Resistor DAC (or) Binary Weighted Resistor DAC :-

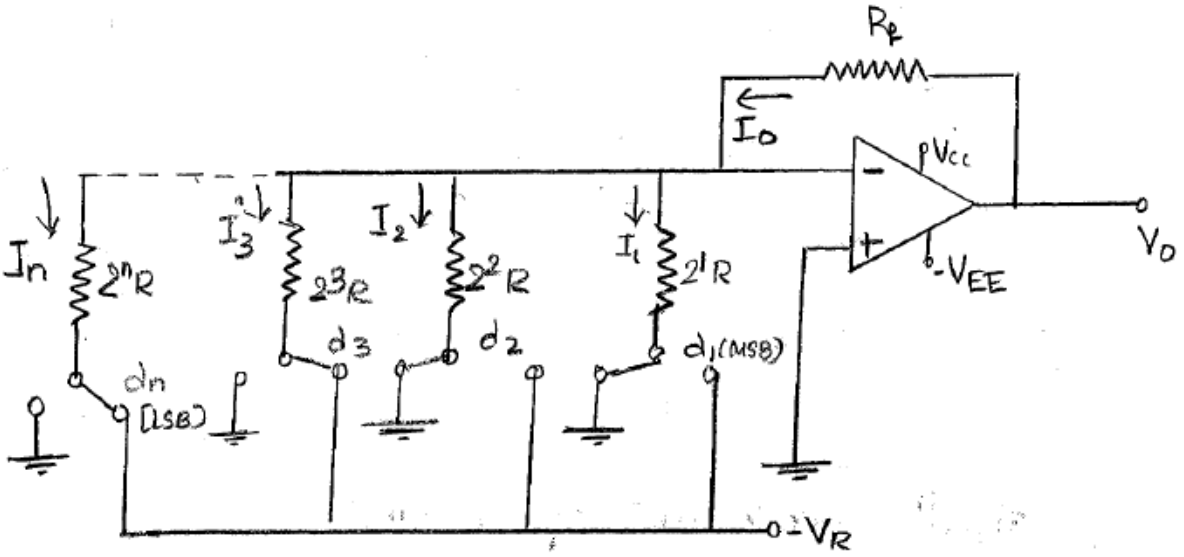

fig : A Simple weighted resistor DAC

* The DAC uses an summing op-amp with a binary weighted resistor 2^1R, 2^2R, 2^3R, ----, 2^nR as shown in fig (a)

* It has n-electronic switches d_1, d_2, ----, d_n controlled by the binary I/P word. These switches are single pole double throw [SPDT] type.

* If the binary input to a particular switch is 1, it connects the resistance to the reference voltage (-ve).

* If the input bit is 0, the switch connects the resistor to the ground.

From fig (a), the o/p current I_o for an ideal op-amp can be written as

$$I_o = I_1 + I_2 + I_3 + ---- + I_n$$

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$$I_0 = \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \frac{V_R}{2^3 R} d_3 + \cdots + \frac{V_R}{2^n R} d_n$$

Where $d_1, d_2, d_3, \ldots, d_n$ may be either 0 or 1 depending on the binary input word.

$$I_0 = \frac{V_R}{R}\left[d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n}\right] \longrightarrow (1)$$

* The O/P voltage

$$V_0 = I_0 R_f \longrightarrow (2)$$

Sub Eq (1) in Eq (2)

$$V_0 = V_R\left[\frac{R_f}{R}\right]\left[d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n}\right]$$

Let $R_f = R$

$$V_0 = V_R\left[d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n}\right]$$

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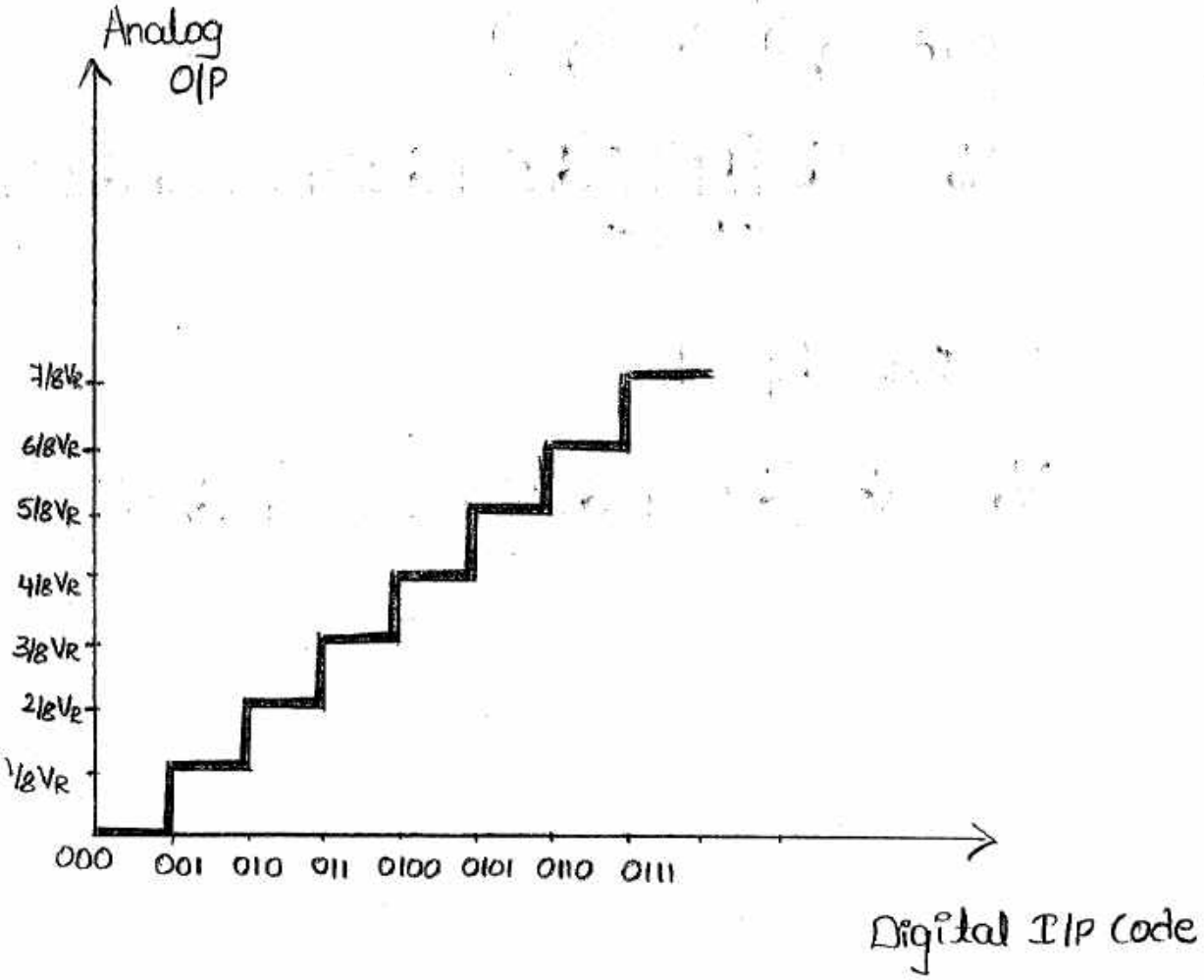
Eg: for 3-bit DAC

Digital I/P d_1 d_2 d_3	Analog O/P V_o
0 0 0	0
0 0 1	$V_R/8$
0 1 0	$2/8\ V_R$
0 1 1	$3/8\ V_R$
1 0 0	$4/8\ V_R$
1 0 1	$5/8\ V_R$
1 1 0	$6/8\ V_R$
1 1 1	$7/8\ V_R$



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* Briefly explain the working of a 4-bit binary weighted resistor DAC.

Jan-11, 6M

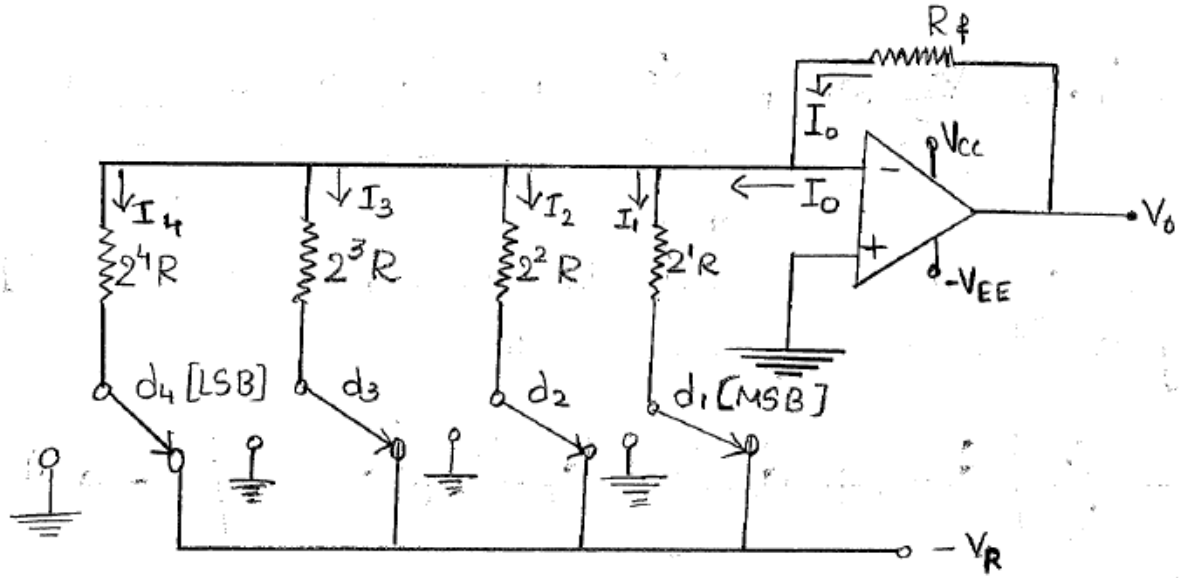

fig @

→ The DAC uses an summing op-amp with a binary weighted resistor 2^1R, 2^2R, 2^3R & 2^4R as shown in fig @.

→ It has 4 electronic switches d_1, d_2, d_3 & d_4 controlled by the binary I/P word. These switches are single pole double throw [SPDT] type.

→ If the binary input to a particular switch is 1 it connects the resistance to the reference voltage ($-V_R$)

If the input bit is 0, the switch connects the resistor to the ground.

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From fig (a), the O/P current I_o for an [ideal] ideal op-amp can be written as

$$I_o = I_1 + I_2 + I_3 + I_4$$

$$I_o = \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \frac{V_R}{2^3 R} d_3 + \frac{V_R}{2^4 R} d_4$$

Where d_1, d_2, d_3 and d_4 may be either 0 or 1 depending on the binary input word.

$$I_o = \frac{V_R}{R}\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + d_4 2^{-4}\right] \rightarrow (1)$$

→ The O/P voltage

$$\boxed{V_o = I_o R_f} \rightarrow (2)$$

Sub eq (1) in eq (2), we get

$$V_o = \frac{V_R}{R} R_f \left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + d_4 2^{-4}\right]$$

Let $R_f = R$.

$$\boxed{V_o = V_R\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + d_4 2^{-4}\right]} \leftarrow (2m)$$

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Note :

Digital IIP				Analog OIP
d_1	d_2	d_3	d_4	V_0
0	0	0	0	0
0	0	0	1	$1/16\ V_R$
0	0	1	0	$2/16\ V_R$
0	0	1	1	$3/16\ V_R$
0	1	0	0	$4/16\ V_R$
0	1	0	1	$5/16\ V_R$
0	1	1	0	$6/16\ V_R$
0	1	1	1	$7/16\ V_R$
1	0	0	0	$8/16\ V_R$
1	0	0	1	$9/16\ V_R$
1	0	1	0	$10/16\ V_R$
1	0	1	1	$11/16\ V_R$
1	1	0	0	$12/16\ V_R$
1	1	0	1	$13/16\ V_R$
1	1	1	0	$14/16\ V_R$
1	1	1	1	$15/16\ V_R$

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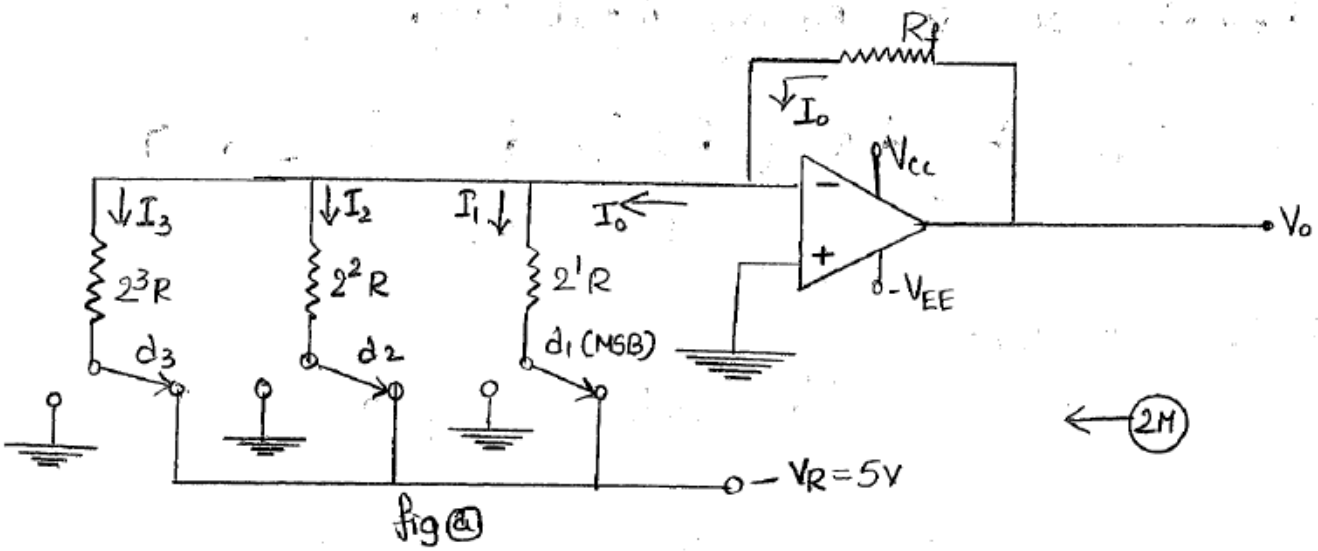
* 8-bit DAC with $V_{out(max)} = 5$ volts.

Jan-09, 5m

Explain about 3-bit DAC and substitute $V_R = 5V$.



fig@

* The DAC uses an summing op-amp with a binary weighted resistor 2^1R, 2^2R & 2^3R as shown in fig@.

* It has 3 electronic switches d_1, d_2 & d_3 controlled by the binary I/P word. These switches are single pole double throw [SPDT] type.

* If the binary input to a particular switch is 1, it connects the resistance to the reference voltage ($-V_R$).

* If the binary input bit is 0, the switch connects the resistor to the ground.

From fig@, the O/P current I_o for an ideal op-amp can be written as,

$$I_o = I_1 + I_2 + I_3$$

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$$I_0 = \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \frac{V_R}{2^3 R} d_3$$

Where d_1, d_2 & d_3 may be either 0 or 1 depending on the binary input word.

$$I_0 = \frac{V_R}{R} \left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} \right] \longrightarrow (1)$$

* The O/P voltage,

$$\boxed{V_0 = I_0 R_f} \longrightarrow (2)$$

Sub Eq(1) in Eq(2), we get

$$V_0 = V_R \left(\frac{R_f}{R}\right) \left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} \right]$$

Let $R_f = R$

$$\boxed{V_0 = V_R \left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} \right]} \leftarrow (2m)$$

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R-2R Ladder DAC :

* With a sketch, explain the working of R-2R ladder DAC.

June-10, 8m

* R-2R ladder DAC

June-09, 5m

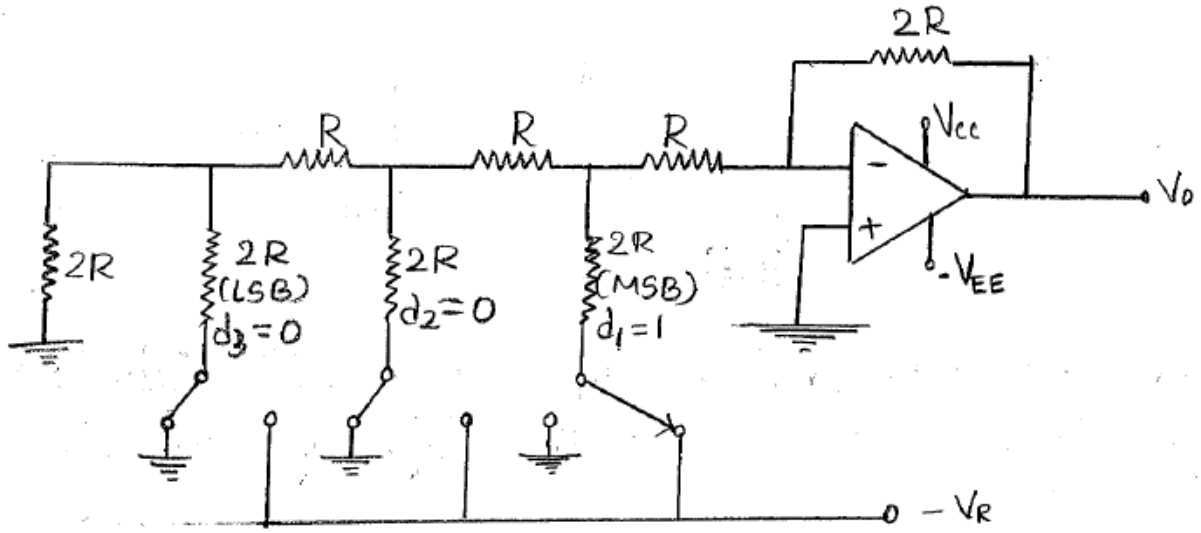

fig @ : R-2R ladder DAC

* R-2R ladder DAC uses only two values of resistor and hence it is easy to fabricate all resistors on a chip [IC].

The typical value of R ranges from 2.25kΩ to 10kΩ

* The resistors [R-2R] are so arranged as to form a ladder network as shown in fig @.

For simplicity, consider a 3-bit DAC as shown in fig @. Let the digital input be a 3-bit binary word given as D = 100.

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$\therefore d_1 = 1,\ d_2 = 0$ and $d_3 = 0$

The switch positions are as shown in fig ⓐ and the ckt is redrawn below.

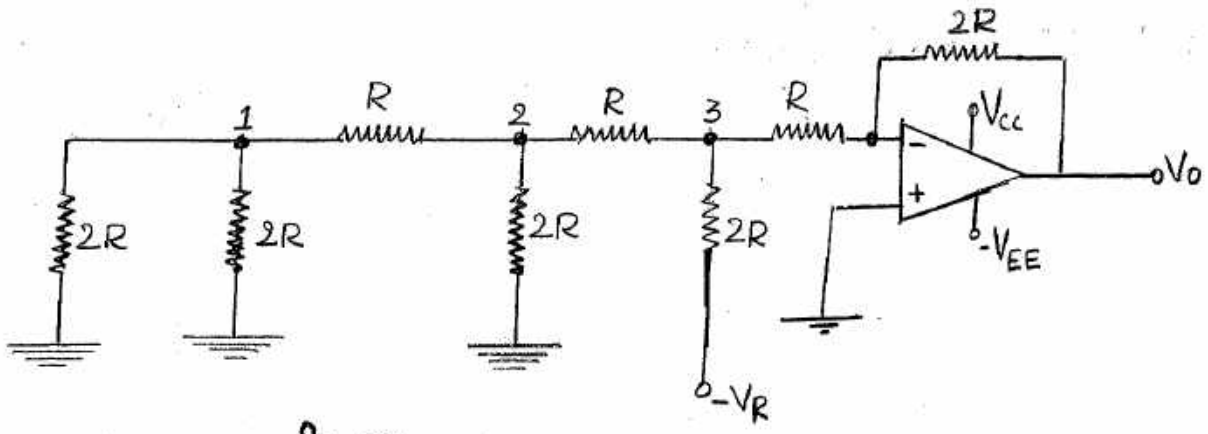
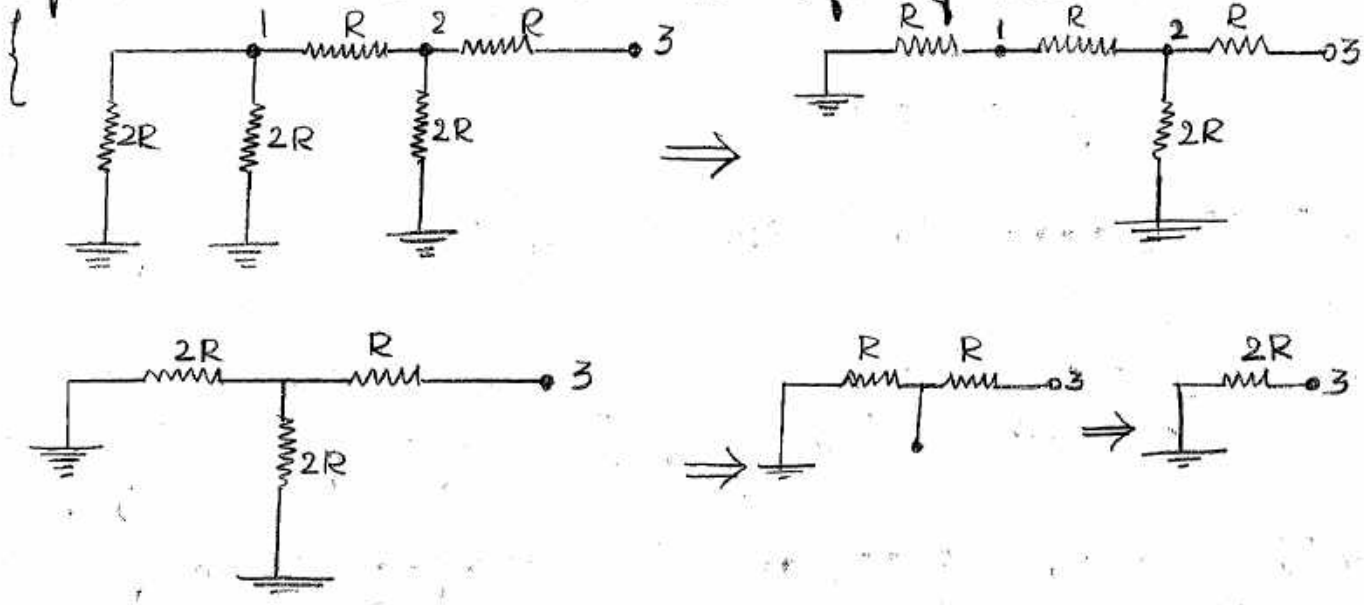


fig ⓑ

* To calculate Voltage at node 3 (V_3), Calculate the equivalent resistance to the left of node 3.



i.e, i] $2R \| 2R = R$

ii] $R + R = 2R$

iii] $2R \| 2R = R$

iv] $R + R = 2R$

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∴ Equivalent resistance to the left of node 3 is 2R.

The modified ckt is as shown in fig ©.

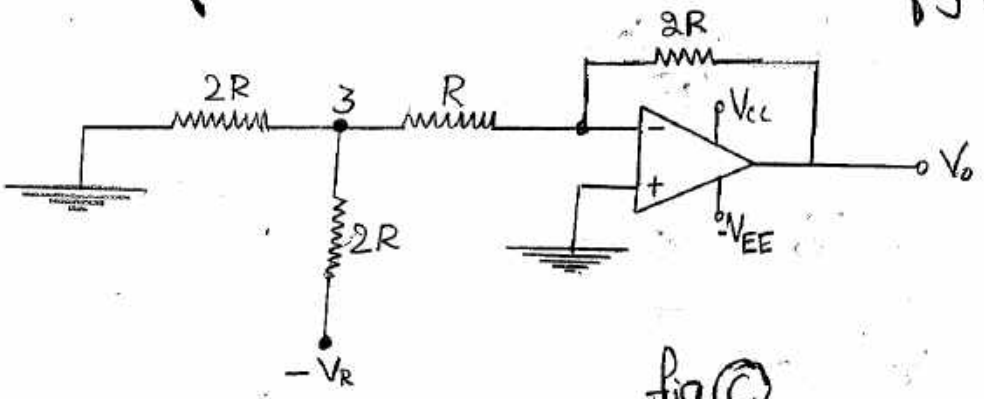

fig ©

* The voltage at node 3 is given by

$$V_3 = IR$$

$$= \frac{-V_R R}{2R+2R}$$

$$= \frac{-V_R R}{4R}$$

$$= \frac{-V_R}{4}$$

$$\boxed{V_3 = -\frac{V_R}{4}}$$

* Fig© is redrawn as below.

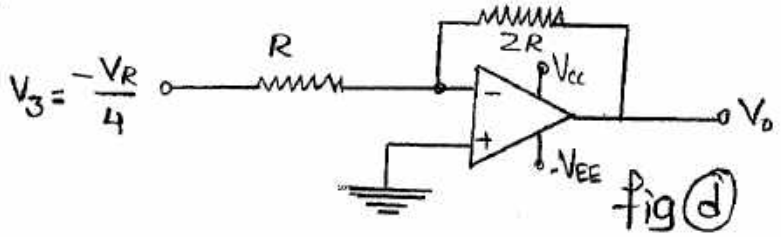

fig ⓓ

* Fig ⓓ is INV amplifier and its O/P voltage is given by

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$$V_o = -\left(\frac{2R}{R}\right)\left(\frac{-V_R}{4}\right) \quad \left\{\because V_o = -\left(\frac{R_f}{R_1}\right)V_i\right\}$$

$$V_o = \frac{2RV_R}{4R}$$

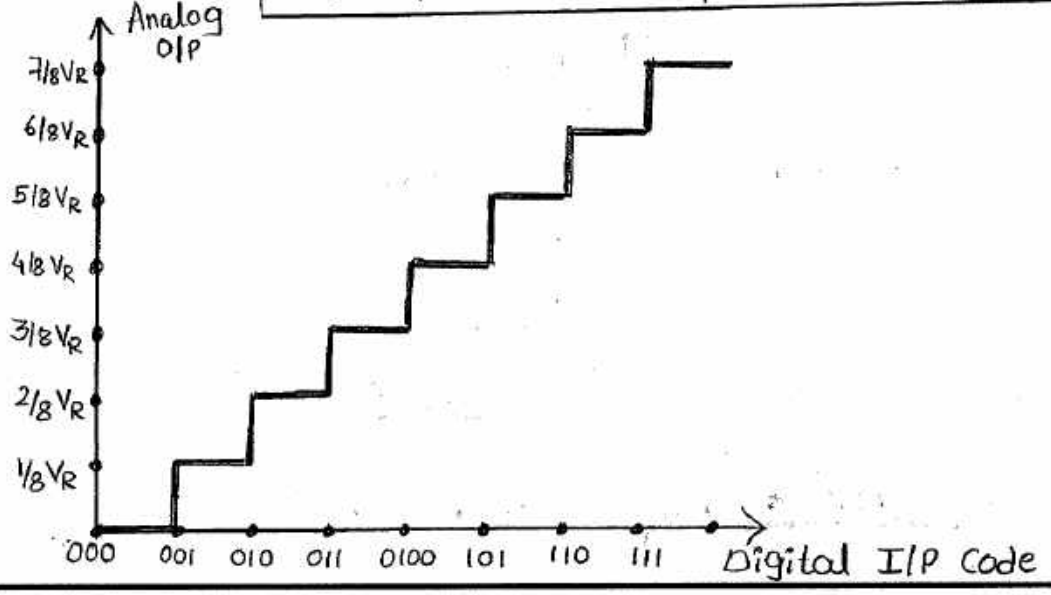
$$\boxed{V_o = \frac{V_R}{2}}$$

Since, $V_R = V_{FS}$

$$\therefore \boxed{V_o = \frac{V_{FS}}{2}} \quad [V_{FS} = \text{full scale O/P Vtg}]$$

* In general,

Digital I/P d_1 d_2 d_3	Analog O/P V_o
0 0 0	0
0 0 1	1/8 V_R
0 1 0	2/8 V_R
0 1 1	3/8 V_R
1 0 0	4/8 V_R
1 0 1	5/8 V_R
1 1 0	6/8 V_R
1 1 1	7/8 V_R



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Performance parameters of DAC :

The various performance parameters of DAC are :

1) Resolution
2) Accuracy
3) Monotonicity
4) Conversion time
5) Settling time
6) Stability

1) Resolution :

Resolution is defined in two ways :

i] Resolution is the number of different analog O/P values that can be ~~performed~~ provided by a DAC. For an n-bit DAC.

$$\text{Resolution} = 2^n$$

ii] Resolution is also defined as the ratio of a change in O/P voltage resulting from a change of 1LSB at the digital inputs.

$$\text{Resolution} = \frac{V_{OFS}}{2^n - 1}$$

2] Accuracy :

It is a comparision of actual o/p voltage with expected O/P. It is expressed in percentage. Ideally, the accuracy of DAC should be at

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Vout, $\pm 1/2$ of its LSB.

$$\text{Accuracy} = \frac{V_{OFS}}{(2^n - 1)2}$$

3] Monotonicity :

A converter is said to have good monotonicity if it does not miss any step backward when stepped through its entire range by a counter.

4] Conversion time :

It is a time required for conversion of analog signal into its digital equivalent or vice versa. It is also called setting time.

5> Settling time :

This is the time required for the O/P of the DAC to settle to within $\pm 1/2$ LSB of the final value for a given digital I/P [i-e zero to full scale.]

6] Stability :

The performance of converter changes with temperature, age and power supply variation. So all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges. These parameters represent the stability of the converter.

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FORMULAE

* Resolution of DAC

i] Resolution $= 2^n$

Where n is the number of bits in DAC

ii] Resolution $= \frac{V_{OFS}}{2^n - 1}$ V / LSB

Where V_{OFS} = Full Scale O/P Voltage.

* O/P Voltage V_o = Resolution × D

For Ex:

$D = (1000)_2 = 8$

$D = (0100)_2 = 4$

* V_{OFS} = Step Size × $(2^n - 1)$

Where n is the no of bits in DAC

* For 8-bit DAC

* $LSB = \frac{1}{2^8} = \frac{1}{256}$

* $MSB = \frac{1}{2^1} = \frac{1}{2}$

* For 4-bit DAC

$$LSB = \frac{\text{Voltage range}}{2^4} = \frac{\text{Voltage range}}{16}$$

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$$MSB = \frac{\text{Voltage range}}{2^1} = \frac{\text{Voltage range}}{2}$$

* Full Scale O/P = [Full Scale Voltage − LSB]

* For n-bit DAC, O/P Voltage is given by

$$V_o = V_R \left[d_1 \cdot \frac{1}{2^1} + d_2 \cdot \frac{1}{2^2} + d_3 \cdot \frac{1}{2^3} + \cdots + d_n \cdot \frac{1}{2^n} \right]$$

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Problems

1) What O/P voltage would be produced by a D/A Converter whose O/P range is 0 to 10V and whose input binary number is

i) 10 [for a 2-bit DAC]

ii) 0110 [for a 4-bit DAC]

iii) 10111100 [for a 8-bit DAC]

Sol⇒ $V_R = 10V$

i) $(10)_2$

$$V_o = V_R \left[d_1 2^{-1} + d_2 2^{-2}\right]$$

$$= 10 \left[1 \times 2^{-1} + 0 \times 2^{-2}\right]$$

$$\boxed{V_o = 5V}$$

ii) 0110

$$V_o = 10 \left[0 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3} + 0 \times 2^{-4}\right]$$

$$\boxed{V_o = 3.75V}$$

iii) 10111100

$$V_o = 10 \left[1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3} + 1 \times 2^{-4} + 1 \times 2^{-5} + 1 \times 2^{-6} + 0 \times 2^{-7} + 0 \times 2^{-8}\right]$$

$$\boxed{V_o = 7.34V}$$

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2) Calculate the values of the LSB, MSB and full scale O/P for an 8-bit DAC for the 0 to 10V range.

Sol:

* LSB for 10V range.

$$LSB = \frac{10V}{2^8}$$

$$\boxed{LSB = 39mV}$$

* MSB for 10V range

$$MSB = \frac{10V}{2^1}$$

$$\boxed{MSB = 5V}$$

* Full Scale O/P = [Full Scale Voltage − LSB]

= [10V − 39mV]

$$\boxed{\text{Full Scale O/P} = 9.961V}$$

3] An 8-bit DAC has an O/P Voltage range of 0-255V. [0-2.55V] Define its resolution in two ways.

Sol:

i] Resolution = $2^n = 2^8 = 256$

ii] Resolution = $\frac{V_{FS}}{2^n - 1} = \frac{2.55}{2^8 - 1}$

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$$\text{Resolution} = \frac{2.55}{2^8 - 1}$$

$$\boxed{\text{Resolution} = 10\text{mV/LSB}}$$

---

4) The digital I/P for a 4-bit DAC is 0110. Calculate its final O/P voltage. Given $V_{OFS} = 15V$.

Sol) $$\text{Resolution} = \frac{V_{OFS}}{2^n - 1} = \frac{15V}{2^4 - 1}$$

$$\boxed{\text{Resolution} = 1V/\text{LSB}}$$

* $V_o = \text{Resolution} \times D$

$$D = (0110)_2 = [0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0]$$

$$\boxed{D = 6}$$

$$V_o = 1V/\text{LSB} \times 6$$

$$\boxed{V_o = 6V}$$

---

5) An 8-bit DAC has resolution of 20mV/LSB. Find V_{OFS} and V_o if the input is $(10000000)_2$

Sol) $$\text{Resolution} = \frac{V_{OFS}}{2^n - 1}$$

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$$20mV = \frac{V_{OFS}}{2^8 - 1}$$

$$\boxed{V_{OFS} = 5.1\ V}$$

$$D = (10000000)_2 = 128$$

$$V_o = \text{Resolution} \times D = 20mV \times 128$$

$$\boxed{V_o = 2.56\ V}$$

---

6) Find out stepsize and analog O/P for 4-bit R-2R ladder DAC when I/P is 1000 and 1111. Assume $V_{ref} = +5V$

Sol:

$$\text{Resolution} = \frac{V_{OFS}}{2^n - 1} = \frac{5V}{2^4 - 1}$$

$$\boxed{\text{Resolution} = 0.33\ V/LSB}$$

* For $D = (1000)_2 = 8$

$$O/P\ V_o = \text{Resolution} \times D = 0.33 \times 8$$

$$\boxed{V_o = 2.6667\ V}$$

* For $D = (1111)_2 = 15$

$$O/P\ V_o = \text{Resolution} \times D = 0.33 \times 15$$

$$\boxed{V_o = 5V}$$

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7) A 12-bit DAC has a stepsize of 8mV. Determine the full scale o/p voltage. Also find the O/P voltage for the I/P of 010101101101

Sol:

Given, $n = 12$

Step size = 8mV

* $V_{OFS} = \text{Step Size} \times (2^n - 1)$

$= 8mV \times (2^{12} - 1)$

$\boxed{V_{OFS} = 32.76\ V}$

$\{ D = (010101101101)_2 = (1389)_{10}$

* The O/P voltage,

$V_o = \text{Resolution} \times D$

$= 8mV \times 1389$

$\boxed{V_o = 11.112\ V}$

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Analog to digital Convertors [ADC] :

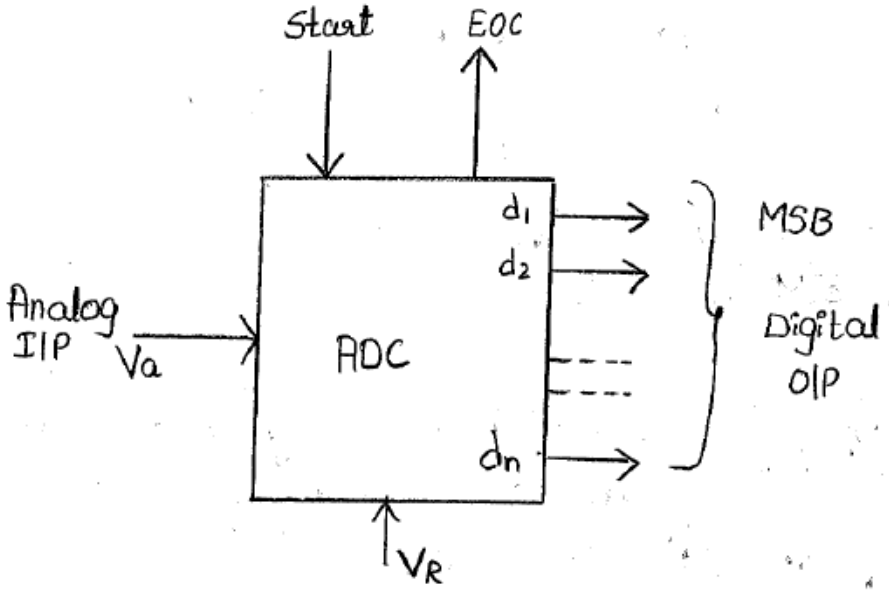

fig ① : Functional diagram of ADC.

Fig ① shows the block schematic of ADC. It accepts an analog input Voltage Va and produces an OIP binary word $d_1, d_2, ----, d_n$ so that,

$$D = d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + ---- + d_n 2^{-n}$$

where d_1 is the most significant bit [MSB] and d_n is the least significant bit [LSB].

* An ADC has two additional control lines :
i] The START input to tell the ADC when to start the conversion and
ii] The EOC [End of Conversion] O/P announces when the Conversion is Complete.

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Classification of ADC's :

* ADC's are classified broadly into two groups according to their conversion technique.

1) Direct type ADC's &
2) Integrating type ADC's.

* Direct type ADC's Compare a given analog signal with the internally generated equivalent signal. Some of the direct type ADC's are :

1] Flash type Converter @ parallel Comparator ADC.
2] Counter type Converter.
3] Tracking or Servo Converter.
4] Successive approximation type converter etc.

* Integrating type ADC's, the analog input signal is first converted into a linear function of frequency & time, and this is subsequently Converted into a digital Code.

The two most widely used integrating type Converters are :

1) Charge balancing ADC
2) Dual Slope ADC.

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Flash ADC or parallel Comparator ADC:

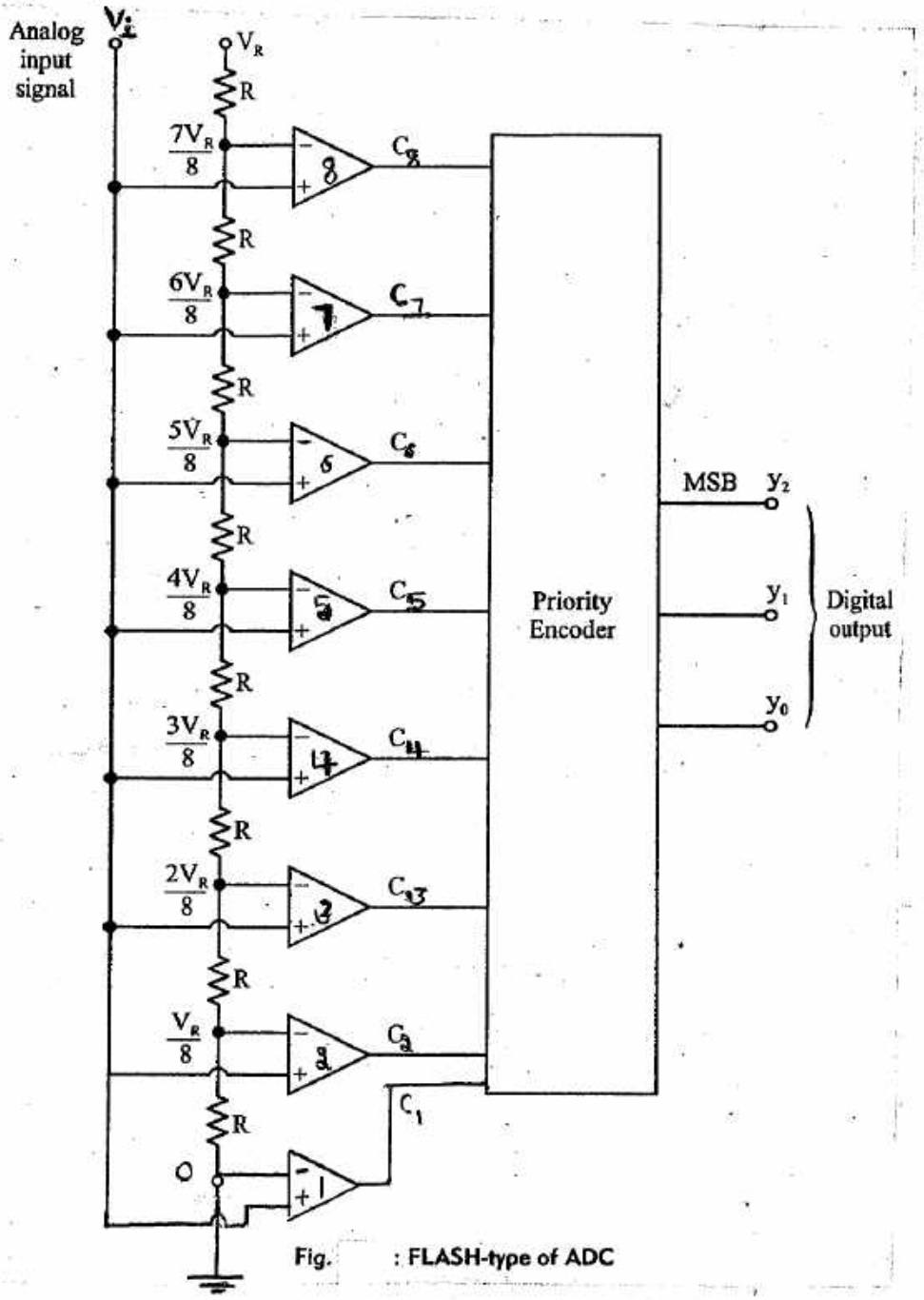

Fig. : FLASH-type of ADC

Voltage input	Logic output X
$V_a > V_d$	$X = 1$
$V_a < V_d$	$X = 0$
$V_a = V_d$	Previous value

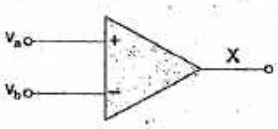

Fig. (b) Comparator and its truth table

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Table Digital output data according to analog input

Input voltage V_i	Outputs of comparators								Digital outputs		
	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	y_2	y_1	y_0
0 to $\frac{V_R}{8}$	0	0	0	0	0	0	0	1	0	0	0
$\frac{V_R}{8}$ to $\frac{2V_R}{8}$	0	0	0	0	0	0	1	1	0	0	1
$\frac{2V_R}{8}$ to $\frac{3V_R}{8}$	0	0	0	0	0	1	1	1	0	1	0
$\frac{3V_R}{8}$ to $\frac{4V_R}{8}$	0	0	0	0	1	1	1	1	0	1	1
$\frac{4V_R}{8}$ to $\frac{5V_R}{8}$	0	0	0	1	1	1	1	1	1	0	0
$\frac{5V_R}{8}$ to $\frac{6V_R}{8}$	0	0	1	1	1	1	1	1	1	0	1
$\frac{6V_R}{8}$ to $\frac{7V_R}{8}$	0	1	1	1	1	1	1	1	1	1	0
$\frac{7V_R}{8}$ to V_R	1	1	1	1	1	1	1	1	1	1	1

→ Fig shows a 3-bit A/D Converter. The Ckt Consists of a resistive divider network, 8 op-amp Comparator and a 8-line to 3-line encoder [3-bit priority encoder].

* The analog input 'V_i' & the INV I/p terminals are Connected to various level of the reference voltage V_R produced by the resistive divider network as shown in figure. The reference voltage V_R is equal to the full Scale input Signal voltage.

* All resistors are of equal magnitude, the voltage levels at the nodes are equally divided between the reference voltage V_R and the ground.

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* The main purpose of building the circuit in the fashion shown in figure is to compare the I/p analog circuit V_i with each of the node voltages.

* The comparators give o/p of 1 or 0 depending upon whether the I/p signal level is greater or less than the reference voltage level.

  i.e. if $V_i > V_d$, then o/p $X = 1$

  $V_i < V_d$, then o/p $X = 0$

  $V_i = V_d$, then o/p X = previous value

* The number of comparators required for n-bit resolution is 2^n & Quantization error is $\pm \frac{1}{2}$ LSB.

* The maximum frequency for a sinusoidal I/p voltage to be digitized within an accuracy of $\pm \frac{1}{2}$ LSB is

$$f_{max} = \frac{1}{2\pi T_c 2^n}$$

Where $T_c \rightarrow$ Conversion time &

$n \rightarrow$ number of bits.

Advantages :-

1) Conversion is very fast (High Speed)

Disadvantages :-

1) It requires a large number of comparators i.e. number of comparators required almost doubles for each added bit.

2) Expensive

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* If the conversion time of a 8-bit Flash ADC is 10 μsec, Find the maximum frequency of a Sinusoidal voltage that can be digitised.

Given :- $n = 8$ and $T_c = 10\ \mu sec$

Sol :- WKT $f_{max} = \frac{1}{2\pi T_c 2^n} = \frac{1}{2\pi \times (10 \times 10^{-6}) \times 2^8}$

$$\boxed{f_{max} = 62.17\ Hz}$$

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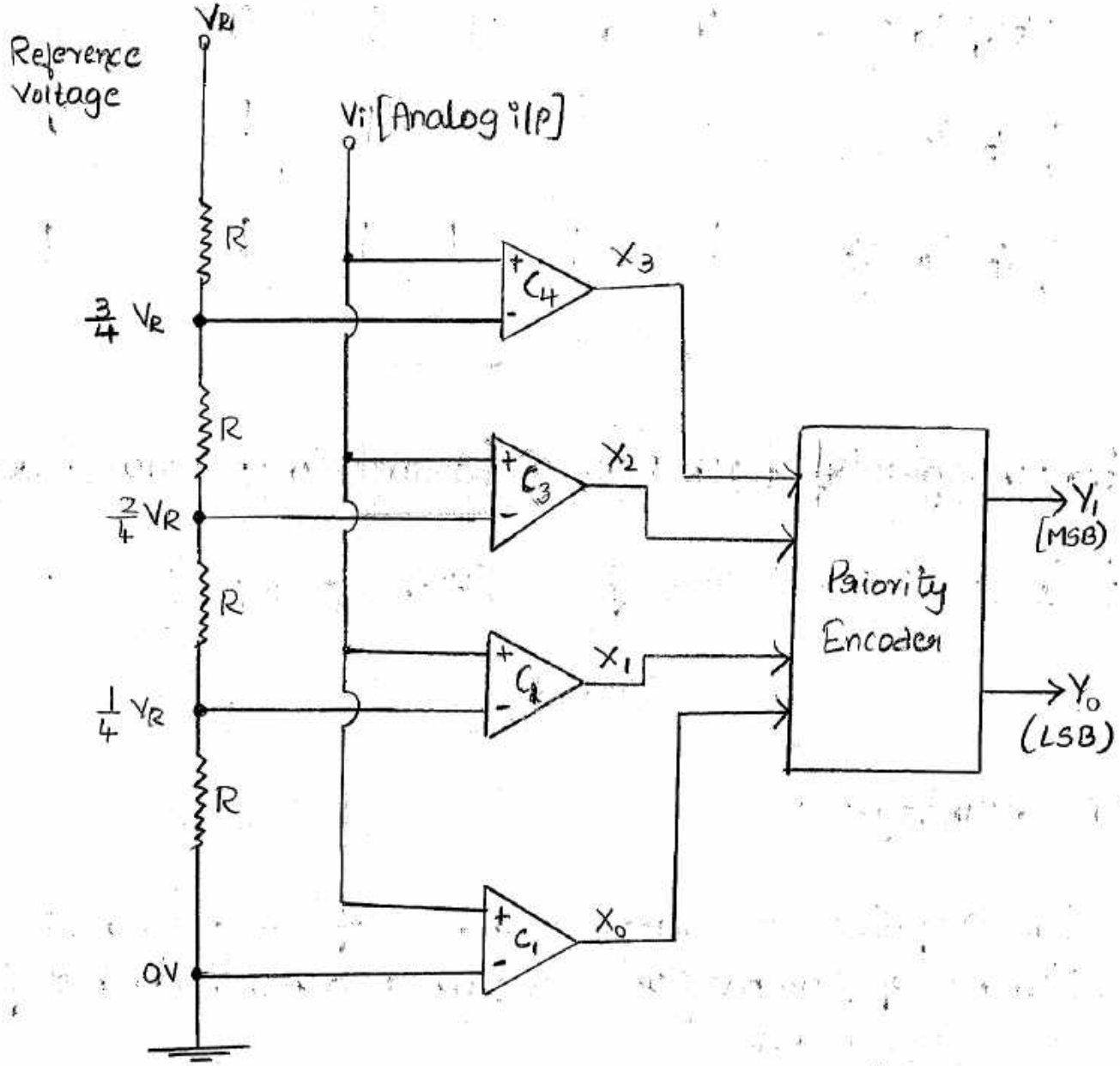
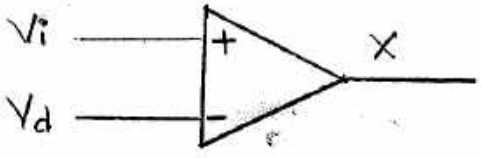
* Design a 2-bit Flash ADC

Sol:- Number of Comparator = $2^n = 2^2 = \underline{4}$

Where $n = 2$





I/P Voltage	O/P Logic 'X'
$V_i > V_d$	$X = 1$
$V_i < V_d$	$X = 0$
$V_i = V_d$	Previous Value

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Analog i/p Voltage (Vi)	O/p of Comparators				Digital O/p's	
	X_3	X_2	X_1	X_0	Y_1	Y_0
0 to $V_R/4$	0	0	0	1	0	0
$V_R/4$ to $\frac{2}{4} V_R$	0	0	1	1	0	1
$\frac{2}{4} V_R$ to $\frac{3}{4} V_R$	0	1	1	1	1	0
$\frac{3}{4} V_R$ to V_R	1	1	1	1	1	1

Advantages of flash ADC @ Parallel Comparator ADC:

1) Conversion is very fast [High Speed]

Disadvantages:

1) It requires a large number of comparators i.e. Number of comparators required almost doubles for each added bit.

Ex: 1) For 3-bit ADC

No of Comparators is $2^n = 2^3 = 8$

2) For 4-bit ADC

No of Comparators is $2^n = 2^4 = 16$

2) Expensive.

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Successive approximation ADC :

* Explain the operation of a successive approximation ADC using a simplified block diagram. Jan-11, 6M

* 4-bit ADC with $V_{in(max)} = 2$ volts. Jan-09, 5m

[Explain any one ADC.]

* What is the main disadvantage of Flash ADC? With the help of a neat diagram explain the operation of a successive approximation type ADC. June-08, 7m

* A/D Converters Jan-10, 5m

Sol:

Explain Disadvantage of Flash type ADC ← 1m

→ A Successive approximation A to D Converter is based on a very efficient code searching strategy called binary search.

→ The searching process is very fast, a n-bit conversion being completed in only n-clock periods.

P.T.O

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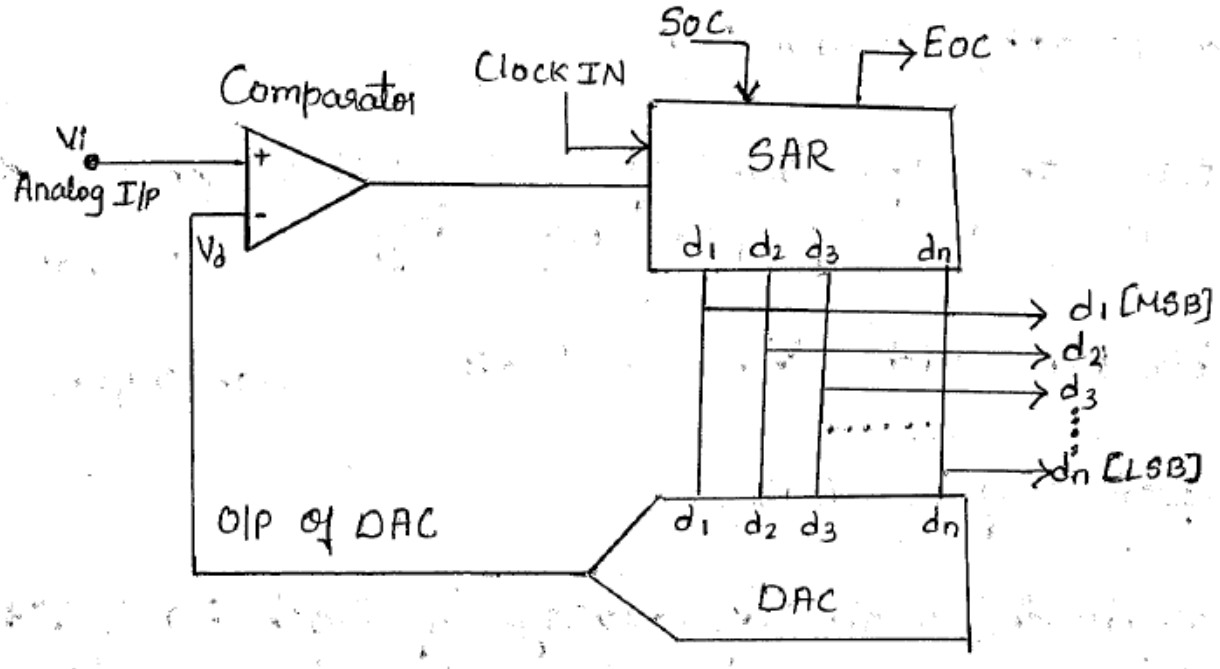

fig ①: Block diagram of Successive approximation A/D Converter

Fig① Shows the block diagram of Successive approximation ADC.

It consists of i] DAC
ii] Comparator &
iii] Successive Approximation Register (SAR)

→ The external clock I/P sets the internal timing parameters. The SOC signal starts the process of conversion and the activated EOC signal announces the end of Conversion process.

Operation:

The SOC signal initiates the process of signal search. The SAR sets the MSB $d_1 = 1$, as soon as the START signal arrives, and all other bits are set to 0, of the Converter is a 8-bit Converter, the

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Initial setting would be 10000000.

The O/P V_A of the DAC for this trial code is compared with the analog I/P V_i. If the analog I/P V_i is greater than the DAC O/P V_A [i.e, $V_i > V_A$], it implies that the trial code 10000000 is less than the correct digital representation of V_i. The MSB d_1 is left at 1 and the next lower significant bit is set at 1, and the process is repeated.

→ On the other hand, if the I/P V_i is less that the DAC O/P V_A, it implies that the trial code 10000000 is greater than the correct digital representation of V_i. In such an event, the MSB is set to '0' and the next lower significant bit is set to '1', and the process is repeated. [i.e 01000000

→ The above process of comparision is repeated for all subsequent bits, one at a time, untill all bit position have been tested.

→ The Comparator changes the state whenever the DAC O/P crosses V_i, and this activates the EOC command.

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Correct digital Representation	SAR OIP VA at different Stages	Comparator OIP
10110010	10000000	1
	11000000	0
	10100000	1
	10110000	1
	10111000	0
	10110100	0
	10110010	1
	10110011	0

→ Comparator OIP after Comparing all 8-bits = 10110010 = Digital representation of analog IIP.

In practice, however, an additional pulse is needed to load the OIP register and reinitialize the Ckt.

→ The time required for one Conversion from analog to digital depends on both the ckts clock period 'T' and the number of bits 'n'.

$$T_c = T(n+1)$$

Where Tc denotes the Conversion time.

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* Dual Slope DAC (or) Integrator type DAC :

June-09, 5M

→ The dual slope DAC is an integrator type D to A converter. Its accuracy is quite high, even though the speed of operation is quite low.

{ In dual slope DAC, the analog input voltage and a reference voltage are both converted into time periods by means of an integrator, and are then measured by means of a Counter }

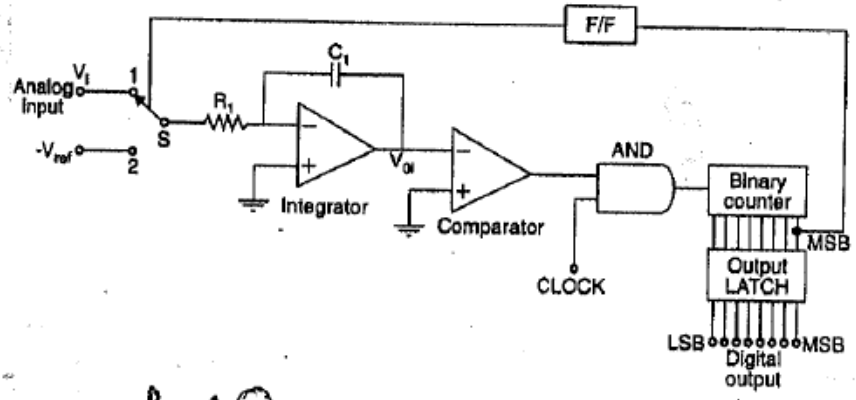

Fig 1(a)

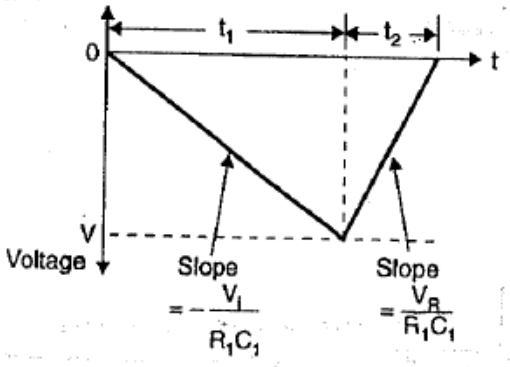

Fig 1(b)

Fig (1)(a) Shows the block diagram of Dual Slope DAC.

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→ The integrator is a ramp generator. There is a switch arrangement 'S' by which the integrator input can be switched between the analog input voltage V_i and a negative reference voltage $-V_{ref}$. The switch is controlled by the MSB of the binary counter.

→ When the MSB is a logic 0, the switch closes on terminal 1 at which the input voltage is applied.

→ When the MSB is a logic 1, the switch closes on terminal 2 at which the input voltage is applied.

→ Operation :

→ Let the switch close on terminal 1 at $t=0$. The analog input voltage V_i gets applied at the INV terminal of the integrator.

The integrator O/P voltage is given as

$$V_{oi} = \frac{-i}{R_1C_1}\int_0^{t_1} V_i\,dt = -\frac{1}{RC}V_i\int_0^{t_1} 1.dt$$

$$\boxed{V_{oi} = -\frac{V_i t_1}{R_1C_1}}$$

→ The integrator O/P voltage is applied to the comparator. The comparator O/P goes high. It enables the AND gate and the clock pulses reach the counter.

→ At the end of 2^n clock periods, the MSB of the

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Counter goes high. This causes the O/P of the flip-flop to go high with the result that the analog switch 'S' Switches from position 1 to position 2, and Connects the reference Voltage to the integrator INV terminal.

Simultaneously the binary counter gets reset. The negative reference Voltage $-V_R$ which now forms the I/P to the integrator makes the O/P of the integrator increases as a positive linear ramp.

When it reaches Zero level, the Comparator O/P goes low, and this disables the AND gates, and the result of it is the clock pulses cease to reach the Counter.

The Counter stops at a Count Corresponding a time interval t_2.

→ Charge Voltage = Discharge Voltage.

$$\frac{V_i t_1}{R_1 C_1} = \frac{V_R t_2}{R_1 C_1}$$

$$\boxed{t_2 = \frac{V_i}{V_R} t_1}$$

In above equation V_R & t_1 are fixed. Hence

$$\boxed{t_2 \propto V_i}$$

i.e. t_2 is directly proportional to the analog input Voltage and hence is a measure of it. The O/P

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of the counter is also proportional to the analog I/P.

$\therefore$ **Digital O/P of the Counter = [Counts/sec] $t_1 \frac{V_i}{V_R}$**

Advantages:

1) It possesses a high degree of accuracy.
2] It is cheap and
3] Its performance is not adversely affected by change of temperature.

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Problems :

1) The reference voltage for a dual slope ADC is 100mV of $t_1 = 50ms$, find t_2 if the input voltage is 150mV.

Sol:- Given,

$V_R = 100mV$

$t_1 = 50msec$

$V_i = 150mV$

$t_2 = ?$

W.K.T, $t_2 = t_1 \cdot \frac{V_i}{V_R}$

$= \frac{50msec \times 150mV}{100mV}$

$\boxed{t_2 = 75msec}$

---

2) For a dual slope ADC, $V_R = 100mV$, $t_1 = 50msec$ and the clock frequency is 12KHz. Find the digital o/p for an input voltage of 200mV.

Sol:- Given, $V_R = 100mV$, $V_i = 200mV$, $t_1 = 50msec$.

Given clock frequency = 12KHz

= 12000 Counts/sec

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WKT, Digital o/p = (Counter/sec) $\frac{t_i V_i}{V_R}$

$$= \frac{12000 \times 50\times10^{-3} \times 900\times10^{-3}}{100\,mV}$$

Digital o/p = 1200 Counts.

---

3) An 8-bit ADC o/p's all 1's when $V_i = 2.55V$, find its,
i] Resolution in mV/LSB and
ii] Digital o/p when $V_i = 1.28V$ **June-10, 6m**

Sol:) i] Resolution $= 2^n = 2^8 = 256$ ✓

$$\text{Resolution} = \frac{V_{FS}}{2^n - 1} = \frac{2.55V}{2^8 - 1}$$

Resolution = 10mV/LSB ← (3m)

ii] Digital o/p $= \frac{1.28V}{10mV/LSB}$

Digital o/p = 128 LSB

Digital o/p code = Binary Equivalent of LSB = 128LSB
$= 10000000$ ← (3m)

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